Capacitances in Compact 7-Parameter Model for Analog Design in Nanoscale Process

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***Abstract*—Lately efforts have been made to have compact models for nanoscale processes with a small number of parameters. These models consider one to four extra parameters in addition to the three basic parameters of the long-channel transistor compact models, which are the slope factor, the equilibrium threshold voltage and the normalization current. An acceptable accuracy of the dc characteristics and the small-signal parameters is obtained through these models. This work analyzes whether it is possible to obtain an adequate model of the intrinsic part of the capacitances by means of these models and parameters, while proposing a simple method to account for the extrinsic part of the capacitances. The proposed method, together with the model, is tested for minimum-length transistors in an FD-SOI 28 nm process and applied to the design of a low-voltage LC oscillator. The results obtained by these means are compared with the results of a look-up table approach and with simulation results, showing a reasonable agreement.**

***Index Terms*—Analog design methodology, MOS capacitance model, nanoscale process, low-voltage design, compact model**

I. INTRODUCTION

The capability of exploiting all inversion regions of MOS transistors, and in particular the moderate inversion region, is well recognized as a need for optimizing the performance of analog circuits. This poses the challenge of correctly modeling the transistor characteristics in a way that is suitable for design calculations. Different approaches have been applied for this. The gm/ID design methodology [1] was originally conceived in part to address this issue. One popular way to apply this methodology is to condensate the information required in a few curves or Look-Up Tables (LUTs) that can be extracted from simulation or measurements. This approach is widely used [2].

On the other hand, efforts towards all-inversion-region, charge-based compact models led to models as EKV [3] and ACM [4]. These models in their initial embodiments targeted long-channel transistors without including second-order effects, and in this case only three parameters are required. Nevertheless, second-order, short-channel effects are a must to model current nanoscale processes. Detailed consideration of all second-order effects, as done in the models applied in simulators (such as BSIM, PSP or UTSOI), lead to deal with tens or even a few hundred parameters.

A key question that arises is whether in advanced processes it is possible to keep the advantage of a simple analytical model, with few parameters, of making analytical derivations on the main circuit performance while achieving a reasonable modeling accuracy. Efforts have been made in this direction, seeking to complement the three basic parameters of the long channel EKV or ACM model with one to four additional key parameters, depending on the intended analysis [5], [6]. In all cases the value of the parameters depends on the transistor channel length. In [7] it is even explored whether the combination of the 3 parameters basic ACM model plus a LUT approach for modeling the output conductance could provide good enough modeling for an advanced 28 nm FD-SOI process. In [7] it is shown that this is the case for operation in weak and moderate inversion regions, except for the modeling of the transistor parasitic capacitances.

The prior works that augment the basic models up to 7 parameters [5], [6] focus on the dc modeling, small-signal parameters and higher-order derivatives for distortion analysis, but, as far as we know, these do not assess the modeling of parasitic capacitances. A question to answer is whether this dc-guided parameter fitting is also useful to provide accurate modeling of capacitances.

This work uses the 7-parameter fitting done on a 28 nm FD-SOI process in [6] to assess how to extend it to model the parasitic capacitances and to evaluate how accurate the results are and suitable for prediction of circuit performance. The study case is the determination of the minimum supply voltage for a 2.45 GHz LC oscillator, previously analyzed using a LUT approach [8].

The paper is organized as follows. Section II summarizes the model that this work is based on. In Section III the methods for deriving the intrinsic capacitances and for dealing with the extrinsic capacitances, which are very significant in short-channel transistors, are presented. The application of the results obtained is shown in Section IV and Section V summarizes the main conclusions of the paper.

II. OVERVIEW OF 7-PARAMETER COMPACT MODEL

In this work, we use the 7-parameter model presented in [6] to obtain the intrinsic capacitances of a MOS transistor. The 7-parameter model is based on the 3-parameter ACM model [9]. These three parameters are the slope factor n, the equilibrium threshold voltage V_{T0}, and the normalization current I_{S0} defined as [4]

$$I_{S0} = \frac{1}{2} n \mu C'_{ox} \phi_t^2 \frac{W}{L}, \tag{1}$$

where μ is the mobility, n is the slope factor, C'_{ox} is the oxide capacitance per unit area, ϕ_t is the thermal voltage and W/L is the aspect ratio of the transistor.

The drain current I_D of a long-channel transistor is expressed as the sum of two currents, namely, the forward and reverse currents [4] (I_F and I_R respectively), as follows

$$I_D = I_F - I_R = I_{S0}\left(i_f - i_r\right), \tag{2}$$

where i_f and i_r are the forward and reverse normalized currents, respectively.

The normalized inversion charge density at source (drain) $q'_{S(D)}$ is the inversion charge per unit area at source (drain) $Q'_{S(D)}$ normalized by the pinch-off charge per unit area $Q'_P = -nC'_{ox}\phi_t$.

The forward (reverse) normalized current $i_{f(r)}$ is related to the normalized inversion charge density at source (drain) $q'_{S(D)}$ in the following way:

$$i_{f(r)} = q'_{S(D)}\left(q'_{S(D)} + 2\right). \tag{3}$$

The relationship between the terminal voltages V_G, V_S, V_D (all referred to the bulk) and the normalized inversion charge densities is [4]

$$V_P - V_{S(D)} = \phi_t\left[q'_{S(D)} - 1 + \ln\left(q'_{S(D)}\right)\right], \tag{4}$$

where the pinch-off voltage V_P can be approximated by $V_P \cong (V_G - V_{T0})/n$.

The 7-parameter model [6] adds 4 extra parameters to account for second-order effects that can be significant, especially for short-channel transistors. These 4 parameters are the carrier mobility reduction factor θ, the Drain-Induced Barrier Lowering (DIBL) factor σ, the carrier velocity saturation factor ζ and the Channel Length Modulation (CLM) factor V_E.

The DIBL effect can be seen as a correction of the gate voltage [6]

$$V_G^* = V_G + \sigma\left(V_D + V_S\right). \tag{5}$$

The carrier mobility reduction and carrier velocity saturation effects can be seen as a correction of the drain voltage. The corrected drain voltage can be obtained as [6]

$$V'_D = V'_{DS} + V_S = \frac{V_{DS}}{\sqrt[4]{1 + \left(\frac{V_{DS}}{V_{DSsat}}\right)^4}} + V_S, \tag{6}$$

where V_{DSsat} is the drain to source saturation voltage and is expressed as

$$\frac{V_{DSsat}}{\phi_t} = q'_S - q'_{Dsat} + \ln\left(\frac{q'_S}{q'_{Dsat}}\right), \tag{7}$$

with q'_{Dsat} such that

$$q'_S = \tfrac{\theta}{2\zeta}q'_{Dsat} - 1 + \sqrt{1 + q'_{Dsat}\left(2 + \tfrac{2}{\zeta} - \tfrac{\theta}{\zeta}\right) + q'^2_{Dsat}\left(1 + \tfrac{\theta}{\zeta} + \tfrac{\theta^2}{4\zeta^2}\right)}. \tag{8}$$

The CLM effect can be seen as a correction of the normalization current I_{S0}, giving [6]

$$I^*_{S0} = I_{S0}\left(1 + \frac{V_{DS} - V'_{DS}}{V_E}\right). \tag{9}$$

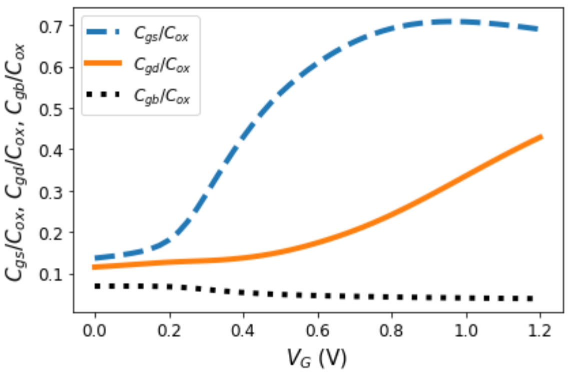

Fig. 1. Simulation results of the normalized total capacitive terms, C_{gs}/C_{ox}, C_{gd}/C_{ox} and C_{gb}/C_{ox}, for a transistor with $L = 30\,\mathrm{nm}$, $W = 1\,\mu\mathrm{m}$, $V_D = 0.3\,\mathrm{V}$ and $V_S = 0\,\mathrm{V}$.

Finally, we use the classic ACM model [4], but with the corrected gate voltage due to DIBL, drain voltage due to carrier mobility reduction and carrier velocity saturation, and the corrected normalization current due to CLM, to find the normalized inversion charge density at source (drain) $q'_{S(D)}$.

III. PARASITIC CAPACITANCES IN 7-PARAMETER MODEL

The parasitic capacitances of the transistors determine the achievable frequency performance of integrated circuits. Therefore, is key to be able to easily estimate them during the design process.

The parasitic capacitances of transistors can be broadly classified in extrinsic and intrinsic [10]. Extrinsic capacitances are very significant since they usually dominate in minimum-length transistors in nanoscale processes [11]. They are also complex to model in these cases.

Figure 1 shows the simulation of the normalized total capacitive terms C_{gs}/C_{ox}, C_{gd}/C_{ox} and C_{gb}/C_{ox} for a minimum-length transistor ($L = 30\,\mathrm{nm}$) in a 28 nm FD-SOI process, with $W = 1\,\mu\mathrm{m}$ and $V_D = 0.3\,\mathrm{V}$. The particular examples shown in this section will refer to this case and the 7 parameters used are those in [6] ($n = 1.377$, $I_{S0} = 5.9\,\mu\mathrm{A}$, $V_{T0} = 384.9\,\mathrm{mV}$, $\sigma = 0.093$, $\theta = 0.115$, $\zeta = 0.035$, $V_E = 5\,\mathrm{V}$). The $V_D = 0.3\,\mathrm{V}$ operating point is selected because the study is aimed at low-voltage designs.

In Fig. 1, particularly in the case of C_{gs} and C_{gd}, it is noticeable that there is a component of the capacitance that varies with the V_G bias point and a constant baseline. The intrinsic part of C_{gs} and C_{gd} ideally would tend to 0 when V_G tends to 0 and there is no significant inversion channel [4]. On the other hand, the intrinsic part of C_{gs} and C_{gd} is expected to vary with V_G. Therefore, the value of C_{gs} and C_{gd} at V_G equal to 0 can be identified to be approximately the extrinsic part of these capacitive terms. In the case of the capacitances of the example transistor shown in Fig. 1, the approximation of the extrinsic components obtained in this way results in $C_{gs_{ext}}/C_{ox} = 0.137\,\mathrm{F/F}$ and $C_{gd_{ext}}/C_{ox} = 0.115\,\mathrm{F/F}$. In this work we will approximate the extrinsic component of C_{gs} and C_{gd} by the value of C_{gs} and C_{gd} at V_G equal to 0 given by the simulation model and parameters provided by the foundry.

An additional issue to be considered is that the 7-parameter model is a bulk CMOS model and we are considering an FD-SOI CMOS process. This is not a major issue for many characteristics that can be well followed provided a suitable parameter set, and in particular the n parameter value, is selected. Nevertheless, this difference in the underlying physical structure of the transistor is noticeable in particular points, such as the substrate charge dependence with V_G and the C_{gb} intrinsic capacitance. In Fig. 1 it can be seen that C_{gb} is almost constant with V_G, which is consistent with a constant charge in the fully depleted body of the FD-SOI transistor instead of the expected substrate charge variation in a bulk transistor. Thus, we consider C_{gb} to be constant, obtained through simulations with $V_G = V_D = 0.3\,\mathrm{V}$, resulting in $C_{gb}/C_{ox} = 0.043\,\mathrm{F/F}$.

Let us now consider how the 7-parameter model described in Section II can be applied to extract the intrinsic capacitance component of C_{gs} and C_{gd} and the results of doing so.

The intrinsic capacitive term $C_{gs(d)}$ is defined as

$$C_{gs(d)} = -\frac{\partial Q_G}{\partial V_{S(D)}}. \tag{10}$$

According to [4], the total gate charge is

$$Q_G = -\frac{Q_I}{n} - Q'_{Ba} W L - Q_O, \tag{11}$$

where Q'_{Ba} is the depletion charge density deep in weak inversion and Q_O is the fixed oxide charge, which are constant, then

$$dQ_G = -\frac{dQ_I}{n}. \tag{12}$$

As a result, $C_{gs(d)}$ can be expressed as

$$C_{gs(d)} = \left(\frac{1}{n}\right) \frac{\partial Q_I}{\partial V_{S(D)}}, \tag{13}$$

where Q_I is the total inversion charge and is such that [4]

$$Q_I = \frac{2}{3}\left(\frac{1+\alpha+\alpha^2}{1+\alpha}\right)(q'_S + 1) - 1, \tag{14}$$

where $\alpha = (q'_D + 1) \,/\, (q'_S + 1)$.

In (14) q'_S can be obtained from (8) considering the 7-parameter model and q'_D is derived using (4-6).

Finally, C_{gs} and C_{gd} are obtained by means of the numerical derivative of Q_I with respect to V_S and V_D, respectively. This approach is taken in order to have an initial assessment of the results of the intrinsic capacitances derived from the 7-parameter model. As future work it would be valuable to have analytical expressions that gives (or approximates) the intrinsic capacitances, so that the advantage of using the 7-parameter analytical model is fully preserved.

The channel length modulation, which affects mainly in strong inversion, does not modify the charges according to the model used, since its effect is modeled directly in the current (9). As a consequence, this effect does not modify the capacitances either.

The results of applying the previous approaches are shown in Figs. 2 and 3 where the results of the intrinsic capacitances derived from the 7-parameter model are compared with the results of the basic 3-parameter model and the simulation results with the model and parameters provided by the foundry. In the right-side y-axis it is shown the relative error with respect to the simulation results of the total (extrinsic plus intrinsic) capacitance of the 7-parameter model with the approach taken here for the extrinsic capacitances.

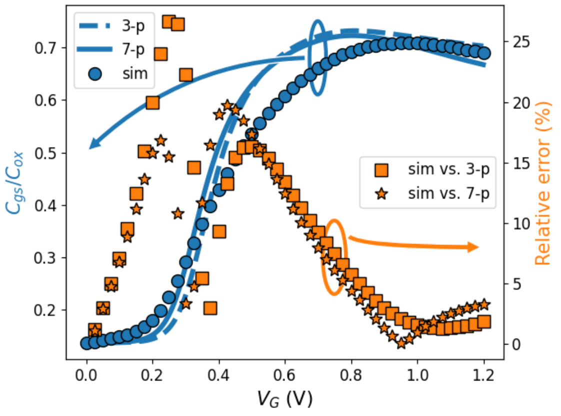

Fig. 2. Normalized intrinsic capacitance C_{gs}/C_{ox} obtained with the 3-parameter model, the 7-parameter model and the simulations and the relative error with respect to the simulation results of the total (extrinsic plus intrinsic) capacitance.

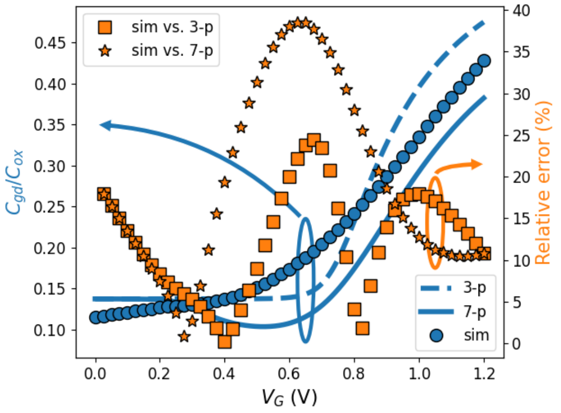

Fig. 3. Normalized intrinsic capacitance C_{gd}/C_{ox} obtained with the 3-parameter model, the 7-parameter model and the simulations and the relative error with respect to the simulation results of the total (extrinsic plus intrinsic) capacitance.

It is noticeable that while a decrease in the error is achieved in C_{gs}, this is not the case for C_{gd}. Nevertheless, in the range of interest for the considered application (up to V_G of 0.4 V), the error remains below 20% in both cases. This provides good results in the considered application, as shown in the next section.

IV. APPLICATION: MINIMUM SUPPLY VOLTAGE OF LC OSCILLATOR

Figure 4 shows the circuit schematic of an LC cross-coupled oscillator. The design is carried out following the procedure

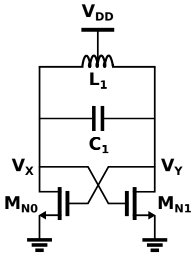

Fig. 4. Circuit schematic of an LC cross-coupled oscillator.

presented in [8] with the same target frequency, 2.45 GHz, and aiming at low voltage and low power. However, this procedure relies strongly on look-up tables (LUTs), which must be filled in advance by means of dc simulations of a unitary transistor at all of the dc operating points $V_{GS} = V_{DS} = V_{DD}$ that may be taken into consideration for the design. Here, the 7-parameter model is used instead of LUTs.

Following [8], the Barkhausen condition simplifies to

$$I_D \geq \frac{\frac{2}{R_P}}{\frac{g_m}{I_D} - \frac{g_d}{I_D}}, \tag{15}$$

where R_P is the equivalent parallel resistor of the inductor and g_m/I_D and g_d/I_D of the transistors are looked up in a table. Here, g_m/I_D and g_d/I_D are obtained using the 7-parameter model with the 7 parameters extracted for a transistor sized $W_u/L_u = 1\,\mu\text{m}/30\,\text{nm}$ presented in [6]. Then, the transistors are implemented with N fingers, each sized W_u/L_u.

Having the same frequency specification and low-power target as [8], allow us to choose the same inductor from the technology library, this is $L_{nom} = 7.76\,\text{nH}$, which has $R_P = 1.6\,\text{k}\Omega$ and $L_1 = 9.63\,\text{nH}$ equivalent inductance at the oscillation frequency. As a result, the total capacitance must be

$$C_{tot} = \frac{1}{(2\pi f_{osc})^2 L_1}, \tag{16}$$

which is composed of C_1 and the parasitic capacitances of the transistors. It was verified through simulations that C_{sd} and C_{bd} are negligible in low-voltage operation with respect to the other parasitic capacitances involved, resulting from [8] in

$$C_1 = C_{tot} - N\left(\frac{C_{gs} + C_{gb}}{2} + 2C_{gd}\right), \tag{17}$$

where C_{gs}, C_{gd} and C_{gb} are the capacitances of the transistors, which are obtained through the 7-parameter model as discussed in Section III.

Figure 5 shows the capacitor C_1 needed to tune the oscillation frequency to 2.45 GHz. The values of C_1 found through (17) and the 7-parameter model applied to the calculations of g_m, g_d and the capacitances, as discussed in Section III, are compared to the simulation results of the oscillator and to the LUT approach presented in [8]. Evidently the results are in more agreement with the results obtained using the LUT approach, since it is based on simulations to load the tables. Nevertheless, the approach presented here still is in good agreement with the simulation results of the oscillator, proving to be an excellent tool for the design as it only requires the extraction of the 7 parameters and 3 extra parameters modeling extrinsic component of C_{gs} and C_{gd} and FD-SOI C_{gb} component, as presented in Section III.

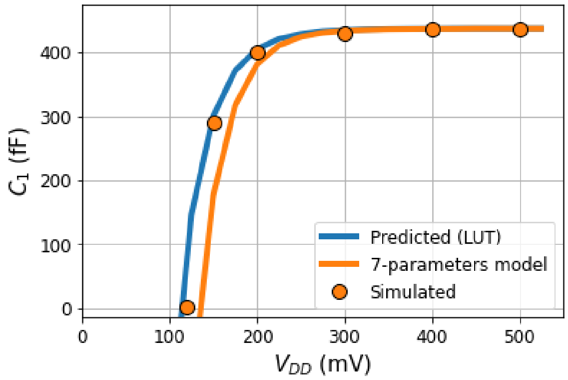

Fig. 5. Simulated necessary capacitor C_1 for oscillation at 2.45 GHz as a function of V_{DD}, compared to the prediction by means of the 7-parameter model and the prediction using the LUT approach in [8].

The capacitor $C_1 = 0\,\text{F}$ for $V_{DD} = 120\,\text{mV}$ represents the operating point with minimum supply possible and no extra capacitance added, as the oscillator only requires the parasitic capacitances to start at the target frequency.

However, a design based solely on parasitic capacitances would not reliable. For $V_{DD} \geq 0.25\,\text{V}$, C_1 is independent of V_{DD}. Thus, it is chosen $V_{DD} = 0.3\,\text{V}$ as a trade-off between robustness and low voltage. Each transistor should have $N = 9$ fingers to obtain a differential output voltage amplitude of 0.3 V.

V. CONCLUSION

This paper has explored whether a 7-parameter compact model fitted to match the dc current characteristics could also be suitable for overall ac characteristics modeling, including capacitive components in a minimum-length transistor of a nanoscale process. First, a simple method is proposed to obtain an approximation of the extrinsic part of C_{gs} and C_{gd}, which are very significant in these transistors. It is described how to calculate the intrinsic part of C_{gs} and C_{gd} using the 7-parameter model. It is discussed how to take into account the fact that an FD-SOI device is being modeled with a bulk MOS model, in the C_{gb} calculation. The analysis shows that the capacitance fitting has a noticeable error, which remains, anyway, below approximately 20% for low voltage operation (below 0.4 V). The model is applied to the design of a low voltage 2.45 GHz LC oscillator, showing good agreement with the LUT approach and the simulation results. This is in part due to the extrinsic capacitances being a significant part of the total capacitance, hence attenuating the impact of the error in the intrinsic part.

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