Dynamic Model of a Six-Transistor Schmitt Trigger in Weak Inversion

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***Abstract*—This paper presents a dynamic model for the six-transistor Schmitt trigger in the weak inversion region. It captures key parameters—capacitances, transition frequency, hysteresis thresholds, output current, and time constants—with good agreement to circuit-level simulations. Complementing existing models, it provides fast and reliable estimates for transistor sizing and reduces the need for extensive simulations, offering a practical tool for the design and analysis of ultra-low-voltage circuits.**

***Index Terms*—Schmitt trigger, weak inversion operation, Dynamic model, Ultra-low-voltage circuits, Hysteresis**

I. Introduction

Wireless sensor nodes and other IoT devices face very tight power budgets, as they rely on small batteries, energy harvesters, or both. To extend battery life or enable operation solely from harvesters, power consumption must be minimized, making the limited power budget a significant challenge [1]. Many harvesters, such as thermoelectric generators, indoor photovoltaics, and bio-potentials, deliver voltages well below 1 V, sometimes under 100 mV [2]–[6]. CMOS circuits can still operate at these levels [7], [8], but careful design and modeling are required to ensure proper dynamic performance, especially for circuits with long standby times [8], [9].

Among circuits suited for ultra-low-voltage design, the Schmitt Trigger (ST) stands out as a versatile building block. The classic six-transistor topology [10], depicted in Fig. 1, was largely overlooked until its recent use in ultra-low-power logic [7]. In low-voltage scenarios, transistors operate in weak inversion, strongly affecting circuit dynamics. To date, no complete dynamic model of the six-transistor ST in weak inversion has been reported. Existing work provides valuable insights—static hysteresis thresholds [11], strong-inversion hysteresis-only models [12], [13], and delay-cell designs with qualitative predictions [14]—but leaves key dynamic parameters uncharacterized. Similarly, metastability has been analyzed for STs at standard supply voltages (0.9 V) [15] and for latches modeled as STs [16], yet transient behavior during dynamic operation with hysteresis remains unexplored.

Weak inversion models have partially addressed ST operation as an amplifier, deriving small-signal transconductances [17], but without considering transition frequency or capacitive coefficients, which are essential for a full understanding of dynamics. Extensions focusing on hysteresis thresholds [18] also omit other dynamic parameters.

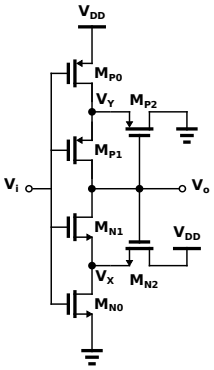

Fig. 1. Six transistor Schmitt trigger circuit schematic.

In this work, transistor capacitive coefficients are calculated and an equivalent-input/output capacitance model is proposed, from which the transition frequency is derived to complete the ST dynamic model in amplifier operation. Key parameters for hysteresis, including thresholds and step response, are also estimated. The model is validated through simulations, showing excellent agreement with predictions.

The paper is organized as follows. Section II presents the ST operation in weak inversion and the dynamic model for amplifier and hysteresis modes. Section III shows simulation results, and Section IV concludes.

II. Operation of the Schmitt trigger in WI

In ultra low voltage operation, both nMOS and pMOS are in the weak inversion region (WI). The nMOS transistor drain current in WI is given by [19], [20]

$$I_{D\,N} = I_N\, e^{\frac{V_{GB}}{n_N \phi_t}} \left(e^{-\frac{V_{SB}}{\phi_t}} - e^{-\frac{V_{DB}}{\phi_t}} \right), \tag{1}$$

where I_N, represents the transistor current strength, given by

$$I_N = \frac{W}{L}\, I_{SQ\,N} = \frac{W}{L}\, n_N \mu_N C'_{ox} \phi_t^2\, e^{1-\frac{V_{T0\,N}}{n_N \phi_t}}, \tag{2}$$

with n_N the slope factor, $V_{T0\,N}$ the equilibrium threshold voltage, ϕ_t the thermal voltage, μ_N the electron mobility, C'_{ox} the oxide capacitance per unit area and W/L the transistor aspect ratio.

The pMOS current is obtained from (1) by replacing V_{SB} with V_{BS}, V_{DB} with V_{BD}, and V_{GB} with V_{BG}, with the current strength from (2) using pMOS parameters.

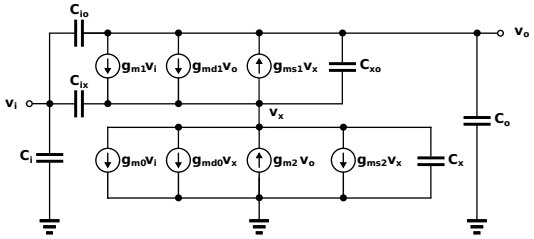

Fig. 2. nMOS network of the six transistor Schmitt Trigger circuit. High-frequency small-signal equivalent model for $V_I = V_O = V_{DD}/2$, accounting for parasitic capacitances.

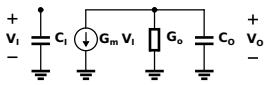

Fig. 3. Circuit schematic of the dynamic model of a Schmitt trigger as an amplifier.

All transistors of the Schmitt trigger (ST) in Fig. 1 are composed of parallel arrangements of nMOS or pMOS unit transistors, achieving the same V_{T0}, I_{SQ}, and n [21], simplifying calculations. The number of parallel units is chosen to ensure symmetry, i.e., $I_{N0} = I_{P0} = I_0$, $I_{N1} = I_{P1} = I_1$, $I_{N2} = I_{P2} = I_2$, and $n_N = n_P = n$.

From (1), the dc equations for nodes V_X and V_Y are [11]

$$e^{\frac{V_X}{\phi_t}} = \frac{I_0 + I_1 + I_2 e^{\frac{V_O - V_I}{\phi_t}}}{I_0 + I_1 e^{-\frac{V_0}{\phi_t}} + I_2 e^{\frac{V_O - V_I}{\phi_t}} e^{-\frac{V_{DD}}{\phi_t}}}, \tag{3}$$

and

$$e^{\frac{V_Y}{\phi_t}} = \frac{I_0\, e^{\frac{V_{DD}}{\phi_t}} + I_1\, e^{\frac{V_O}{\phi_t}} + I_2\, e^{\frac{V_I - V_O}{\phi_t}}}{I_0 + I_1 + I_2\, e^{\frac{V_I - V_O}{\phi_t}}}, \tag{4}$$

where $n = 1$ for simplicity. The dc equation for node V_O is given by

$$e^{\frac{V_I - V_X}{\phi_t}} - e^{\frac{V_I - V_O}{\phi_t}} = e^{\frac{V_Y - V_I}{\phi_t}} - e^{\frac{V_O - V_I}{\phi_t}}. \tag{5}$$

Finally, from (3), (4) and (5), V_O can be expressed as a function of V_I, V_{DD} and the current strengths.

A. The Schmitt trigger as an amplifier

The high-frequency small-signal model of the ST's nMOS network is shown in Fig. 2 and, by symmetry, can be extended to the full ST. A simplified model (Fig. 3) is obtained by expressing G_m, G_o, C_I, and C_O in terms of the components of Fig. 2, whose expressions are derived in the following sections.

1) Transconductances: The transconductances are defined as follows

$$g_{mk} = \left.\frac{\partial I_{D\,N}}{\partial V_{GB}}\right|_{V_I = V_O = V_{DD}/2}, \tag{6a}$$

$$g_{mdk} = \left.\frac{\partial I_{D\,N}}{\partial V_{DB}}\right|_{V_I = V_O = V_{DD}/2}, \tag{6b}$$

$$g_{msk} = -\left.\frac{\partial I_{D\,N}}{\partial V_{SB}}\right|_{V_I = V_O = V_{DD}/2}, \tag{6c}$$

TABLE I
TRANSCONDUCTANCES OF THE SCHMITT TRIGGER

	g_m	g_{ms}	g_{md}
M_{N0}, M_{P0}	$\frac{I_0}{n\phi_t}\left[\frac{1 - e^{-\frac{V_{X0}}{\phi_t}}}{e^{-\frac{V_{DD}}{2n\phi_t}}}\right]$		$\frac{I_0}{\phi_t}\left[\frac{e^{\frac{V_{DD}}{2n\phi_t}}}{e^{\frac{V_{X0}}{\phi_t}}}\right]$
M_{N1}, M_{P1}	$\frac{I_1}{n\phi_t}\left[\frac{e^{-\frac{V_{X0}}{\phi_t}} - e^{-\frac{V_{DD}}{2\phi_t}}}{e^{-\frac{V_{DD}}{2n\phi_t}}}\right]$	$\frac{I_1}{\phi_t}\left[\frac{e^{\frac{V_{DD}}{2n\phi_t}}}{e^{\frac{V_{X0}}{\phi_t}}}\right]$	$\frac{I_1}{\phi_t}\left[\frac{e^{\frac{V_{DD}}{2n\phi_t}}}{e^{\frac{V_{DD}}{2\phi_t}}}\right]$
M_{N2}, M_{P2}	$\frac{I_2}{n\phi_t}\left[\frac{e^{-\frac{V_{X0}}{\phi_t}} - e^{-\frac{V_{DD}}{\phi_t}}}{e^{-\frac{V_{DD}}{2n\phi_t}}}\right]$	$\frac{I_2}{\phi_t}\left[\frac{e^{\frac{V_{DD}}{2n\phi_t}}}{e^{\frac{V_{X0}}{\phi_t}}}\right]$	

where g_{mk}, g_{mdk} and g_{msk}, are the gate, drain and source transconductances of transistor k, respectively. The values are summarized in Table I.

The equivalent G_m and G_o in Fig. 3 can be expressed in terms of the transconductances in Table I as [17]

$$G_m = -2 \times \frac{g_{m1}(g_{ms2} + g_{md0}) + g_{ms1} g_{m0}}{g_{ms1} + g_{ms2} + g_{md0}}, \tag{7}$$

$$G_o = -2 \times \frac{g_{md1}(g_{ms2} + g_{md0}) - g_{ms1} g_{m2}}{g_{ms1} + g_{ms2} + g_{md0}}. \tag{8}$$

2) Capacitive coefficients: In WI the intrinsic capacitances, other than the gate-bulk capacitance C_{gb}, are negligible. This can be verified by deriving the expressions in WI for the intrinsic capacitances [19]. Thus, the gate to bulk intrinsic capacitance of transistor k is given by

$$C_{gbk} = \left(\frac{n-1}{n}\right) W_k L_k C'_{ox}, \tag{9}$$

where W_k and L_k are the width and length of transistor M_{Nk}, respectively.

On the other hand, the overlap and junction extrinsic capacitances are taken into consideration. Each of the parasitic capacitance contributes to one of the equivalent capacitances in Fig. 2, giving

$$C_i = C_{s0\,ov} + C_{gb0} + C_{gb1}, \tag{10a}$$

$$C_x = C_{J0} + C_{J1} + C_{J2}, \tag{10b}$$

$$C_{ix} = C_{d0\,ov} + C_{s1\,ov}, \tag{10c}$$

$$C_o = C_{d2\,ov} + C_{gb2} + C_{J1}, \tag{10d}$$

$$C_{io} = C_{d1\,ov}, \tag{10e}$$

$$C_{xo} = C_{s2\,ov}, \tag{10f}$$

where $C_{pk\,ov}$ is the overlap capacitance at node p of transistor k and C_{Jk} is the extrinsic capacitance within the drain or source to bulk junction.

The extrinsic overlap capacitances of transistor k are expressed as

$$C_{sk\,ov} = C_{dk\,ov} = C'_{ox} W_k LD, \tag{11}$$

being LD the overlapping distance.

For the sake of simplicity, the extrinsic junction capacitances are considered to be independent of any voltage

variations, hence, $C_{Jk} = C'_J \times A_{Sk}$, where C'_J and A_{Sk} are the junction capacitance per unit area and the drain or source diffusion area of transistor k, respectively.

The equivalent input and output capacitances, C_I and C_O in Fig. 3, can be expressed taking into consideration the Miller effect [22] as

$$C_I = C_i + C_{io}\left(1 + |A_{io}|\right) + C_{ix}\left(1 + |A_{ix}|\right), \tag{12}$$

$$C_O = C_o + C_{io}\left(1 + \frac{1}{|A_{io}|}\right) + C_{xo}\left(1 + \frac{|A_{ix}|}{|A_{io}|}\right), \tag{13}$$

where A_{io} and A_{ix} are the low frequency voltage gain , at $V_I = V_O = V_{DD}/2$, between v_o and v_i and v_x and v_i, respectively, given by

$$A_{io} = \frac{g_{m1}(g_{ms2} + g_{md0}) + g_{ms1}g_{m0}}{g_{md1}(g_{ms2} + g_{md0}) - g_{ms1}g_{m2}}, \tag{14}$$

$$A_{ix} = \frac{g_{m1} - g_{m0}}{g_{ms1} + g_{md0} + g_{ms2} - g_{m2}}. \tag{15}$$

Due to the symmetry of the ST circuit, each pMOS capacitance is modeled in parallel with its nMOS counterpart, so the total capacitances are given by the nMOS values times $(1 + W_{pMOS}/W_{nMOS})$, assuming equal channel lengths.

3) Intrinsic transition frequency: The transition frequency of the ST is defined analogously to a single transistor [23]. The short-circuit current gain magnitude a_i is the ratio of the small-signal output to input currents, hence,

$$a_i = \frac{i_{out}}{i_{in}} = \frac{G_m}{2\pi f C_{IT}}, \tag{16}$$

where G_m is the equivalent transconductance of the ST (7) and C_{IT} the total input capacitance, i.e., the sum of all input-node capacitances, given by

$$C_{IT} = C_i + C_{io} + C_{ix}. \tag{17}$$

Unlike the voltage gain used for C_I and C_O (12, 13), a_i is a current gain. The intrinsic transition frequency f_T is the frequency at which $a_i = 1$, yielding

$$f_T = \frac{G_m}{2\pi C_{IT}}. \tag{18}$$

B. Schmitt trigger with hysteresis

The minimum supply voltage to obtain hysteresis in an ST with symmetric pMOS and nMOS networks is given by [11]

$$V_{DDH} \approx 2\phi_t \, ln\left[n\left(1 + \frac{I_0}{I_2}\right)\left(1 + \frac{I_1}{I_0} + \frac{I_2}{I_0}\right) - \frac{I_1}{I_0}\right]. \tag{19}$$

The hysteresis width is approximated by [17]

$$V_L \approx \frac{(V_{DD} - 2V_{X0})\left(1 - e^{V_{DDH} - V_{DD}}\right)}{2 + \frac{I_0}{I_2} + \frac{I_1}{I_2}}, \tag{20}$$

where V_{X0} is V_X at $V_I = V_O = V_{DD}/2$, and provided that the transistors are in WI region. Owing to the symmetry of the circuit, the input value of the upper and lower thresholds of the hysteresis loop are

$$V_{TH\pm} = \frac{V_{DD}}{2} \pm \frac{V_L}{2}. \tag{21}$$

TABLE II
TRANSISTOR DIMENSIONS OF THE SCHMITT TRIGGER CIRCUIT.

$L_{N,P}$ [μm]	W_{N0} [μm]	W_{P0} [μm]	W_{N1} [μm]	W_{P1} [μm]	W_{N2} [μm]	W_{P2} [μm]
1.08	8×5.1	8×53	2×5.1	2×53	4×5.1	4×53

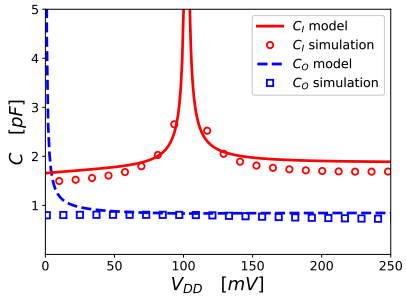

Fig. 4. Equivalent input and output capacitances as functions of the supply voltage, V_{DD}. The analytic curves follow (12) and (13) and are contrasted to simulation results.

In the region with hysteresis, the response to a step from V_{DD} to zero is given by

$$v_o(t) = V_{DD}\left(1 - e^{-t/\tau}\right), \tag{22}$$

with the time constant

$$\tau = R_O \, C_O \tag{23}$$

and the output resistance

$$R_O = \left.\frac{V_O}{I_O}\right|_{V_I = 0}, \tag{24}$$

where the output current I_O is calculated as the difference between the drain currents of transistors M_{N1} and M_{P1}, at $V_I = 0$ V. The drain currents are I_{DN1} and I_{DP1}, respectively, and follow (1).

III. SIMULATION RESULTS

Simulations were carried out on the ST circuit with transistor sizes listed in Table II. Figure 4 compares the simulation results with the analytical predictions. The input capacitance C_I shows a singularity at the supply voltage V_{DD}, where hysteresis occurs, since the gain A_{io} in (17) becomes infinite. In general, the model slightly overestimates C_I due to conservative assumptions. The output capacitance C_O predicted by the model diverges as V_{DD} approaches zero, whereas in simulations it remains nearly constant. This discrepancy is explained by the fact that the linear model does not account for the saturation of parasitic capacitances at very low voltages.

The model accurately predicts the circuit behavior both in the amplifier region ($V_{DD} < V_{DDH}$) and in the hysteresis region ($V_{DD} > V_{DDH}$), as ac simulations are consistent with the linear model. Capacitive extractions using steady state simulations confirm the model predictions, with minor differences arising from feedback resistances in the nonlinear model. Transition frequency f_T is extracted considering the

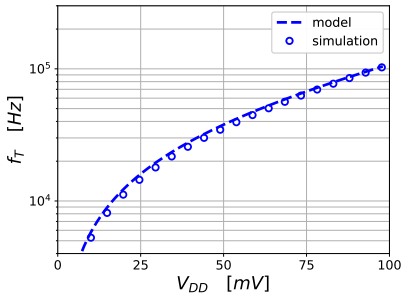

Fig. 5. Transition frequency as a function of the supply voltage, V_{DD}, estimated analytically and contrasted to simulation results.

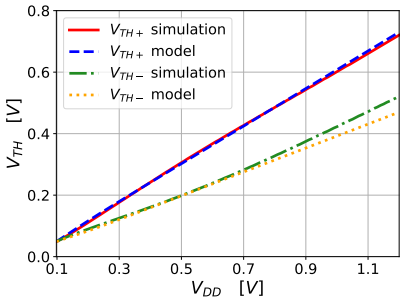

Fig. 6. Thresholds of the hysteresis as a function of the supply voltage, V_{DD}, estimated analytically and contrasted to simulation results.

differential gain and hysteresis thresholds, providing results consistent with the linear model across the supply range.

Figure 5 shows the simulated and analytical transition frequency in (18), demonstrating good agreement. Figure 6 presents the simulated and modeled hysteresis thresholds $V_{TH,+}$ and $V_{TH,-}$ as a function of V_{DD}, showing agreement for weak inversion operation.

The main parameters of the ST with hysteresis are modeled and verified. In particular, the output current I_O predicted by the model is shown in Fig. 7, illustrating its strong dependence on V_O. For each V_{DD}, an average I_O is used to estimate an equivalent output resistance R_O and the time constant τ. Figure 8 shows transient step responses for various V_{DD} values, from which τ is extracted (10–90% rise time). As expected, rise time decreases with increasing supply voltage. Figure 9 compares the time constant τ calculated from (23) with simulations. The model accurately predicts τ at low supply voltages, while deviations grow for $V_{DD} > 0.2$ V as the linear approximation loses validity and nonlinear effects in the transistors operation become significant. Despite these deviations, the model captures the overall dynamic trends and provides a reliable tool for design estimation in the weak inversion regime.

The simulations show that the model accurately captures device trends, with deviations reflecting its simplifying assumptions. It thus provides a useful tool for sizing transistors and quickly estimating key dynamic parameters, reducing reliance on extensive ac or transient simulations in early design stages.

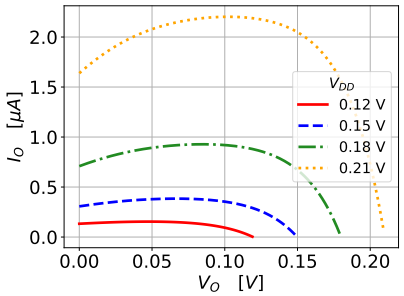

Fig. 7. Model results of the output current of the Schmitt trigger, I_O, at $V_I = 0$ V, as a function of the output voltage V_O and for several values of supply voltage V_{DD}.

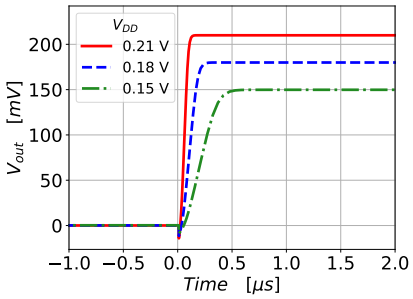

Fig. 8. Transient simulation results of the step response of the Schmitt trigger with hysteresis for several values of supply voltage V_{DD}.

IV. Conclusion

This work contributes a compact model that provides fast and reliable estimates of key dynamic parameters. While the model relies on simplifying assumptions that introduce small deviations, it still enables efficient transistor sizing and reduces reliance on extensive simulations, offering a practical and versatile tool for early-stage circuit design.

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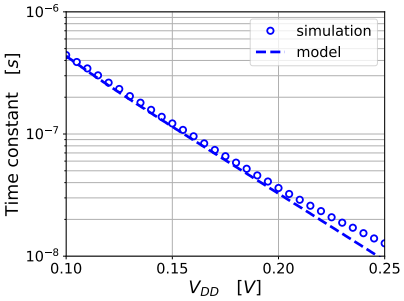

Fig. 9. Time constant τ as a function of the supply voltage, V_{DD}, estimated analytically and contrasted to simulation results.

REFERENCES

[1] D. Yoon, T. Jang, D. Sylvester, and D. Blaauw, "A 5.58 nW crystal oscillator using pulsed driver for real-time clocks," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 2, pp. 509–522, Feb 2016.

[2] H. Bottner, J. Nurnus, A. Gavrikov, G. Kuhner, M. Jagle, C. Kunzel, D. Eberhard, G. Plescher, A. Schubert, and K. Schlereth, "New thermoelectric components using microsystem technologies," *Journal of Microelectromechanical Systems*, vol. 13, no. 3, pp. 414–420, June 2004.

[3] Alta devices: Single junction gallium arsenide photovoltaic product. [Online]. Available: https://www.altadevices.com/wp-content/uploads/2018/04/Single-Junction-Tech-Brief.pdf

[4] C. J. Love, S. Zhang, and A. Mershin, "Source of sustained voltage difference between the xylem of a potted ficus benjamina tree and its soil," *PLoS ONE*, vol. 3, no. 8, e2963, 2008.

[5] P. Weng, H. Tang, P. Ku, and L. Lu, "50 mV-input batteryless boost converter for thermal energy harvesting," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 4, pp. 1031–1041, April 2013.

[6] S. Bandyopadhyay, P. P. Mercier, A. C. Lysaght, K. M. Stankovic, and A. P. Chandrakasan, "A 1.1 nW energy-harvesting system with 544 pW quiescent power for next-generation implants," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 12, pp. 2812–2824, Dec 2014.

[7] N. Lotze and Y. Manoli, "A 62 mV 0.13μm CMOS standard-cell-based design technique using Schmitt-trigger logic," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 1, pp. 47–60, Jan 2012.

[8] ——, "Ultra-sub-threshold operation of always-on digital circuits for IoT applications by use of Schmitt trigger gates," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 11, pp. 2920–2933, Nov 2017.

[9] R. G. Dreslinski, M. Wieckowski, D. Blaauw, D. Sylvester, and T. Mudge, "Near-threshold computing: Reclaiming Moore's law through energy efficient integrated circuits," *Proceedings of the IEEE*, vol. 98, no. 2, pp. 253–266, Feb 2010.

[10] "CMOS Schmitt trigger: A uniquely versatile design component," Fairchild Semiconductor Corporation, Application Note AN-140, Jun. 1975, also circulated later under National Semiconductor branding. Fairchild was acquired by onsemi in 2016.

[11] L. A. P. Melek, A. L. da Silva, M. C. Schneider, and C. Galup-Montoro, "Analysis and design of the classical CMOS Schmitt trigger in subthreshold operation," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 4, pp. 869–878, 2017.

[12] M. R. Elmezayen, W. Hu, A. M. Maghraby, I. T. Abougindia, and S. U. Ay, "Accurate analysis and design of integrated single input Schmitt trigger circuits," *Journal of Low Power Electronics and Applications*, vol. 10, no. 3, p. 21, 2020, available: https://doi.org/10.3390/jlpea10030021.

[13] A. L. da Silva Junior, L. A. P. Melek, C. Galup-Montoro, and M. C. Schneider, "Inadequacy of the classical formulation of the CMOS Schmitt trigger," *International Journal of Circuit Theory and Applications*, vol. 49, no. 5, 2021.

[14] M. Ahmed, A. Trigui, S. Genevey, Y. Audet, and Y. Savaria, "A 32-mV supply ring oscillator composed of modified Schmitt trigger delay cells for integrated start-up circuits in dc energy harvesting systems," *IEEE Access*, vol. 12, pp. 129 660–129 672, 2024.

[15] J. Maier, C. Hartl-Nesic, and A. Steininger, "Simulation-based approaches for comprehensive Schmitt-Trigger analyses," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 69, no. 3, pp. 1013–1026, March 2022.

[16] J. Maier, A. Steininger, and R. Najvirt, "The hidden behavior of a D-latch," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 70, no. 4, pp. 1660–1670, 2023.

[17] L. A. P. Melek, M. C. Schneider, and C. Galup-Montoro, "Operation of the classical CMOS Schmitt trigger as an ultra-low-voltage amplifier," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 65, no. 9, pp. 1239–1243, Sep. 2018.

[18] A. Nowbahari, L. Marchetti, and M. Azadmehr, "Subthreshold modeling of a tunable CMOS Schmitt trigger," *IEEE Access*, vol. 11, pp. 10 977–10 984, 2023.

[19] M. C. Schneider and C. Galup-Montoro, *CMOS Analog Design Using All-Region MOSFET Modeling*. Cambridge University Press, 2010.

[20] C. C. Enz, F. Krummenacher, and E. A. Vittoz, "An analytical MOS transistor model valid in all regions of operation and dedicated to low-voltage and low-current applications," *Analog Integrated Circuits and Signal Processing*, vol. 8, pp. 83–114, 1995.

[21] C. Galup-Montoro, M. C. Schneider, and I. J. B. Loss, "Series-parallel association of FET's for high gain and high frequency applications," *IEEE Journal of Solid-State Circuits*, vol. 29, no. 9, pp. 1094–1101, 1994.

[22] A. S. Sedra and K. C. Smith, *Microelectronic Circuits*, 6th ed. Oxford University Press, 2010.

[23] Y. Tsividis and C. McAndrew, *Operation and Modeling of the MOS Transistor*, 3rd ed. Oxford Univ. Press, 2011.