Current-Starved Inverter Cell Design Trade-Offs for Single Capacitively Coupled Ring VCOs

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***Abstract*—This paper presents a comparative study of inverter cell topologies for use in a single capacitively coupled (SCC) ring VCO targeting multi-phase RF applications. Three inverter cells are investigated: nMOS-only (N), pMOS-only (P), and complementary nMOS–pMOS (NP), each implemented with current-starved control for frequency tuning. The cells are designed in 28-nm FD-SOI technology under a common parameterization, ensuring that performance differences arise from intrinsic architectural properties rather than transistor sizing. Simulation results compare frequency tuning range, power consumption, output swing, signal symmetry and phase noise. The N cell achieves the widest tuning range, the NP cell offers better symmetry and the P cell shows limited swing and higher asymmetry but with lower power consumption. These results reveal intrinsic trade-offs between efficiency, signal integrity, and spectral purity, providing practical guidelines for inverter selection in SCC VCO designs.**

***Index Terms*—Ring VCO, current starving, multi-phase oscillators, low-power RF design**

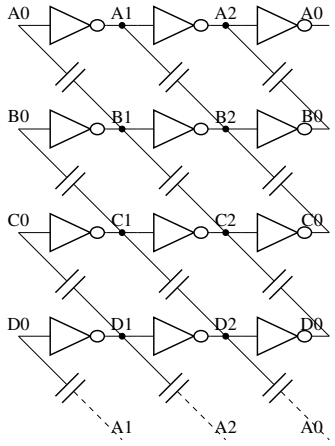

Fig. 1. Circuit schematic of the single capacitively coupled (SCC) ring VCO.

I. Introduction

LC-VCOs are widely used for local oscillators in integrated radiofrequency (RF) systems due to their frequency stability and low noise. However, they require large silicon area and do not inherently generate multi-phase signals. Ring oscillators (ROs) address both limitations, making them attractive for highly integrated systems requiring multiple phases, such as polyphase filter mixers [1] with digital clocks or N-path mixers [2] with analog-type ROs.

N-path systems [3] are increasingly relevant thanks to their frequency selectivity, agility [4], and ability to provide amplification [5] and mixing with excellent linearity [6]. Built only from switches and capacitors, they are compact and efficient, consuming only the oscillator's energy. However, some architectures, such as harmonic rejection N-path designs [7], demand multiple phases and duty cycles that cannot be generated by simple frequency division, motivating research in multi-phase RO solutions.

Among different RO architectures, the single capacitively coupled (SCC) ring VCO generates multiple evenly spaced phases with low phase noise [8]. The SCC VCO considered in this work (Fig. 1) consists of four coupled three-stage ROs, each stage implemented as a current-starved inverter to control oscillation frequency. This configuration, yields twelve outputs with 50% duty cycle and uniform phase distribution.

Previous works have investigated current-starved ROs [9], [10] and techniques for reducing power [11] and improving phase noise using resistive control [12], [13]. However, a systematic comparison of inverter cells as building blocks for VCOs is still missing. This paper fills that gap by evaluating three current-starved inverter cells—nMOS-starved (N), pMOS-starved (P), and symmetrically starved (NP)—and examining how their architecture affects not only frequency tuning but also critical metrics such as output swing, duty-cycle symmetry, and phase noise. These factors are critical in multi-phase systems, where deviations from ideal behavior can degrade linearity, reduce selectivity and undermine robustness.

The paper is organized as follows: Section II introduces the inverter cell designs and parameterization. Section III presents performance results and trade-offs across the three cells. Section IV concludes with design guidelines for selecting inverter cells in multi-phase SCC VCOs.

II. Design and Parameterization of Inverter Cells

Three inverter cell topologies are considered as candidates for the SCC VCO: an nMOS-only cell (N), a pMOS-only cell (P), and a complementary nMOS–pMOS cell (NP), as illustrated in Fig. 2. The NP topology is expected to provide improved symmetry, while the N and P cells, using only one device type, benefit from simpler layout and reduced parasitic loading.

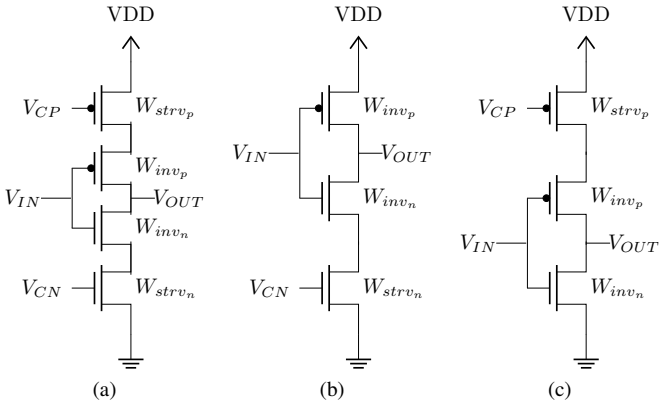

Fig. 2. Schematics of the inverter cells (a) NP cell, (b) N cell, and (c) P cell.

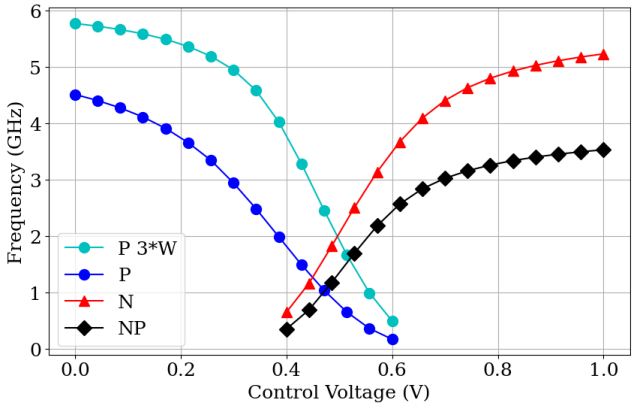

Fig. 3. Oscillation frequency as a function of control voltage V_C (tuning range) for the different inverter cells considered.

Current-starved operation is achieved by inserting control transistors in series with the pull-up and pull-down devices of the inverter; these transistors are biased to limit the available charging and discharging currents. A single input voltage V_C is used directly when the cell requires only one control voltage (the N and P cell cases): in an N-type cell V_C is applied as V_{CN} to bias the n-side starving transistor, and in a P-type cell V_C is applied as V_{CP} to bias the p-side starving transistor. By contrast, an NP cell requires two distinct gate biases, V_{CN} and V_{CP}, one for each control transistor; these must be produced from the single input V_C using a simple biasing circuit. Generating both V_{CN} and V_{CP} from V_C adds the extra circuitry and layout complexity that the NP cell exhibits compared with the N- and P-only cells, which can use V_C directly.

All simulations are performed in 28-nm FD-SOI technology. Each inverter drives a 10 fF capacitive load, with supply voltage $V_{DD} = 1\,\text{V}$ and a control voltage V_C. The channel length is fixed at 60 nm, appropriate for analog design, and transistor widths are parametric as indicated in Fig. 2.

Because nMOS devices have higher mobility than pMOS, using equal starving widths W_{strv_n} and W_{strv_p} would make the P cell intrinsically slower, biasing the comparison. Simulations confirm that scaling W_{strv_p} by three balances rise and fall times. Results are therefore reported for both the equal-width case and for $W_{strv_p} = 3 \times W_{strv_n}$ in the case of the P cell.

A fixed parameterization is maintained across all topologies rather than individually optimizing each cell. This strategy ensures that performance differences can be attributed to the intrinsic characteristics of the topologies themselves, rather than to transistor sizing choices. In this way, the analysis highlights fundamental trade-offs between the three architectures and their suitability for SCC VCO design.

III. Performance Results

This section presents simulation results of the SCC VCO implemented with each of the three inverter cells, evaluating frequency range, power consumption, output swing, signal symmetry and phase noise. The goal is to assess their suitability as building blocks of the SCC VCO and identify the main trade-offs. The transistor widths in Fig. 2 are set to $W_{inv} = 2\,\mu\text{m}$, $W_{strv} = 1.68\,\mu\text{m}$.

A. Frequency Tuning Range

Figure 3 shows the tuning range for the considered cells as a function of the control voltage V_C.

The NP and N cells do not reach as low frequencies as the P cell. This limitation could be addressed either by further reducing V_C—ensuring the oscillator still starts—or by adjusting transistor dimensions. Conversely, the P cell ($W_{strv_p} = 3 \times W_{strv_n}$) and N cell achieve higher maximum frequencies, indicating that sizing adjustments could enable more frequency coverage. As expected, the NP cell exhibits a smaller overall tuning range because one of its control voltages is constrained by the current mirror used to bias the dual-starved configuration.

The NP cell, which employs both nMOS and pMOS current-starving transistors, reaches the lowest maximum frequency. This behavior results from two main factors. First, the additional starving device increases parasitic capacitances at the inverter nodes, slowing charge and discharge transitions. Second, since both the nMOS and pMOS branches simultaneously limit current, the effective charging and discharging currents are inherently lower than in the N or P cells, where only a single branch is starved. This combined current limitation reduces the maximum achievable oscillation frequency for the NP cell.

B. Power Consumption

The power consumption of the oscillator built with each inverter cell is characterized as a function of oscillation frequency. The P and N cell-based oscillators do not include a voltage control circuit, so their consumption reflects only the oscillator itself. In contrast, for the NP cell-based oscillator, both the oscillator and its control circuit consumption are included. The results are shown in Figure 4.

All versions show a linear increase of power with frequency, with minor differences in slope. The oscillator built with the P

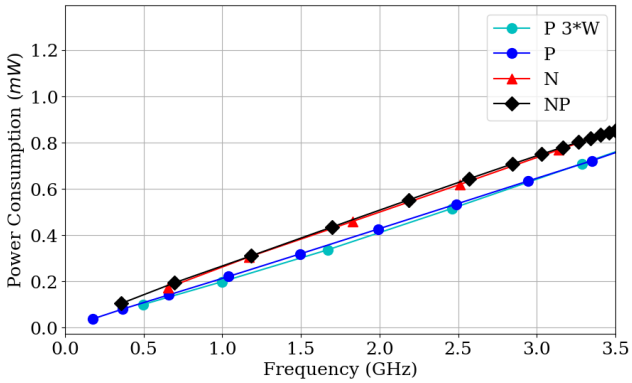

Fig. 4. Power consumption as a function of oscillation frequency for the different inverter cells considered.

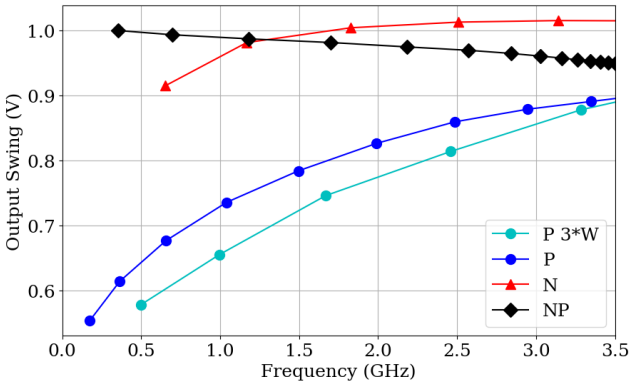

Fig. 5. Output swing as a function of oscillation frequency for the different inverter cells considered.

cell consumes the least power, as frequency control limits the charging current, whereas in the N cell it limits the discharging current. Increasing the P cell's starving transistor width by a factor of three does not affect the consumption trend. The N and NP cell-based oscillators exhibit higher overall power consumption.

C. Output Voltage Swing

The output swing of the oscillator implemented with each inverter cell is characterized as a function of frequency. The output swing is particularly relevant, as the cell structure directly affects the signal amplitude. Since the VCO outputs will pass through buffer stages, the main requirement is that the swing remains above a reasonable threshold, chosen here as 0.8 V. Figure 5 shows the results.

The NP cell-based oscillator maintains the most stable swing, close to the ideal 1 V, because both charging and discharging currents are symmetrically limited by dedicated starving transistors. In contrast, the P cell exhibits a significantly reduced output swing, dropping below 0.9 V for most frequencies and even below 0.6 V at some points. This occurs because only the pMOS branch limits the charging current, while the nMOS discharge path remains unrestricted. As a result, the high-level output voltage cannot reach the full supply, producing asymmetric swing. Increasing the pMOS width (e.g., three times larger) does not fully correct this effect, indicating that it stems from the intrinsic behavior of the single-branch starved topology rather than sizing. Consequently, the P cell cannot deliver sufficient high-level voltage, which may compromise switching in subsequent stages, making it less suitable for implementation.

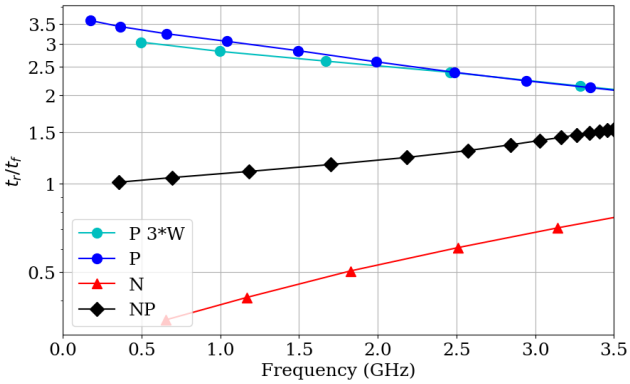

Fig. 6. Rise/fall time ratio t_r/t_f as a function of oscillation frequency for the inverter cells considered.

The N cell, by contrast, does not show this low-level swing limitation because its nMOS-starved configuration limits only the discharge current, leaving the charging path free to reach near-supply voltage. In the NP cell, both branches are actively limited but balanced, so charging and discharging currents remain symmetric, preserving nearly full swing.

D. Output Symmetry

To assess output signal symmetry, two metrics are evaluated for each oscillator: the rise-to-fall time ratio t_r/t_f (measured from 10% to 90% of the swing) and the dc output component V_{DC}. Ideally, $t_r/t_f = 1$ and $V_{DC} = 0.5\,\mathrm{V}$. Simulations out of the scope of this paper, including subsequent buffer stages, show that these metrics directly influence duty-cycle integrity and its frequency dependence. While output stages could partially tune nominal values, these simulations emphasize the intrinsic impact of the inverter cell topology on frequency-dependent variations.

Figures 6 and 7 show t_r/t_f and V_{DC} as functions of frequency, respectively. The P cell exhibits the largest t_r/t_f variation across frequency, reflecting significant asymmetry in its current paths and correlating with its reduced high-level output swing. The NP cell, despite being a symmetric topology, shows only a modest improvement over the N cell. Despite differing current limitations, both the N and NP cells exhibit relatively balanced operation, yielding improved symmetry across the frequency range. For V_{DC}, the NP cell remains closest to 0.5 V with minimal variation, followed by the N cell, while the P cell deviates significantly, even when the pMOS starving transistor width is increased by a factor of three.

A quantitative analysis over the full frequency range (0–3.5 GHz) confirms these observations. Two averaged

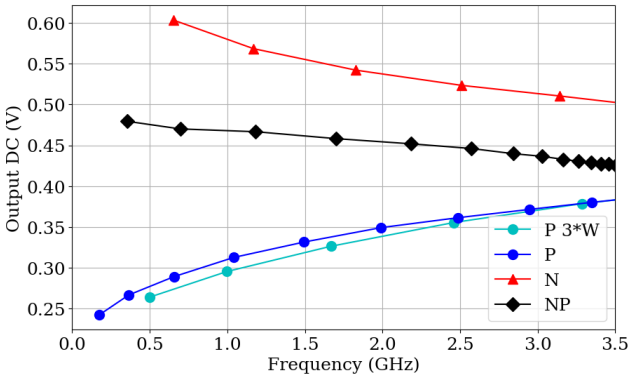

Fig. 7. Dc component at the output as a function of oscillation frequency for the inverter cells considered.

TABLE I
SYMMETRY METRICS AVERAGE OVER FREQUENCY RESULTS

Metric \ Topology	P	P 3*W	N	NP	Ideal
$\max\left(t_r/t_f,\ t_f/t_r\right)$	2.7	2.5	1.9	1.2	1
$\lvert V_{DC} - 0.5\,\mathrm{V}\rvert$ (mV)	160	160	38	46	0

metrics were considered. First, signal symmetry was assessed through the average of the maximum of t_r/t_f and t_f/t_r, where unity indicates perfect symmetry. Second, duty-cycle distortion was quantified through the average of $|V_{DC} - 0.5\,\mathrm{V}|$ across frequency. The results of these metrics are presented in Table I.

These metrics confirm that the N and NP cells maintain better signal symmetry and more consistent dc levels than the P cell.

E. Phase Noise

Phase noise of the different cells is characterized. Simulations show that the two versions of the P cell ($W_{strv_p} = W_{strv_n}$ and $W_{strv_p} = 3W_{strv_n}$) yield nearly identical results, so only the case $W_{strv_p} = W_{strv_n}$ is reported for simplicity.

Figure 8 presents phase noise as a function of oscillation frequency for offset frequencies of 100 kHz and 1 MHz.

Across all offset frequencies, the NP cell exhibits significantly higher phase noise compared to the N and P cells. This is likely due to the presence of two active devices per stage, increasing the total noise contributions. The N and P cells perform similarly at 100 kHz and 1 MHz.

F. Discussion

The P cell is the most power-efficient but suffers from a reduced output swing and worse symmetry. The NP cell exhibits the highest phase noise, while the N and P cells show similar results.

In symmetrically starved configurations, the effect of the control voltages V_{CN} and V_{CP} becomes particularly important. Each voltage is generated by a transistor under bias constraints, so neither can fully reach the supply rails. Consequently, one starving branch is always partially limiting the current available to charge or discharge the load capacitances. This inherent restriction explains the lower oscillation frequencies observed in starved cells and also introduces asymmetries that can impact duty-cycle integrity and phase noise.

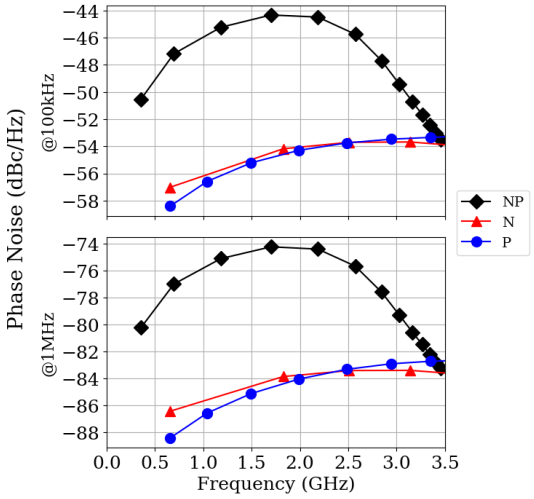

Fig. 8. Phase noise at 100 kHz and 1 MHz offset for the inverter cells NP, N and P.

Overall, the P cell favors power efficiency, the NP cell favors output swing robustness and the N cell provides the best compromise between symmetry, phase noise and moderate consumption, guiding inverter selection for multi-phase SCC VCOs.

IV. CONCLUSION

This work provides a systematic comparison of current starved inverter cells for SCC ring VCOs, highlighting how cell topology affects tuning range, output swing, signal symmetry, and phase noise. By evaluating different designs under consistent conditions, the study offers guidelines for selecting inverter cells based on design priorities such as power efficiency, signal integrity, and spectral purity. These insights can inform future multi-phase VCO designs and support optimized trade-offs in low-power applications.

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