A Low-Power 12-Phase Single Capacitively Coupled Ring VCO for Wideband N-Path Systems

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***Abstract*—This work presents a novel Single Capacitively Coupled (SCC) ring Voltage-Controlled Oscillator (VCO) designed for wideband N-path systems. It reduces the number of capacitors by half compared to the Double Capacitively Coupled (DCC) design, potentially requiring less silicon area while maintaining improved phase noise performance compared to the pseudo differential ring VCO, and with less power consumption than the DCC design. The proposed SCC VCO, tunable from 0.3 to 3.0 GHz, achieves the lowest power consumption among the state-of-the-art designs compared, consuming just 0.48 mW at 3 GHz, with a phase noise of -76.5 dBc/Hz at 1 MHz offset. Consequently, the figure of merit (FOM) remains modest at -147 dBc/Hz, comparable to other designs but leaving room for improvement. The analysis reveals that improper configuration may lead to unwanted oscillation modes of the three VCOs analyzed, making a startup circuit essential for stable operation. These results position the SCC ring VCO as a promising candidate for low-power, high-performance applications.**

Index Terms— Voltage-Controlled Oscillator (VCO), Ring Oscillators, Low-Power Design, Wideband Receiver, N-Path Systems

I. Introduction

In integrated radio frequency systems, LC voltage controlled oscillator (LC-VCO) architectures are commonly used to implement local oscillators due to their strong frequency stability and favorable noise performance. However, their silicon footprint significantly impacts the production costs of circuits, and they do not inherently generate multi-phase signals. For these reasons, ring oscillators (ROs) are particularly advantageous when system-level requirements demand high integration and specific phase number, as is notably the case in polyphase filter based mixers [1] where the multi-phase clocks are typically digital clocks, or in RF N-path filter based mixers [2], where the multi-phase clocks are analog-type ROs.

Interest in N-path systems [3] is growing due to their highly advantageous properties. They offer frequency selectivity while remaining agile [4], enabling amplification [5] and mixing functions with excellent RF performance, particularly in terms of linearity [6]. As they rely solely on switches and capacitors, they can be highly integrable and consume only the energy required by the driving oscillator. However, depending on the chosen architecture, they may require a significant number of distinct phases and duty cycles that cannot be generated through simple division, as it is the case with harmonic rejection N-Path architecture [7]. This makes the exploration of multi-phase RO architectures particularly relevant in this field of research.

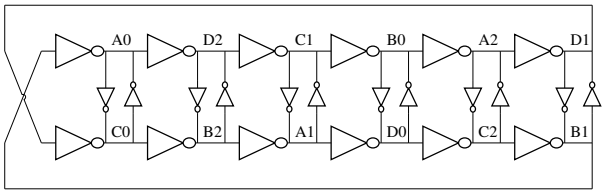

Fig. 1. Pseudo differential ring VCO.

The inverter rings are usually complemented with additional interstage coupling with inverters, which allows to improve phase noise performance. This is the case of the architecture referred as pseudo-differential ROs [8], [9] depicted in Fig. 1.

An alternative to the use of inverters as interstages is capacitive coupling between the rings. In [10] a 12-phase oscillator is built using 4 ROs, with 3 stages each, that are capacitively coupled from each stage output to the input of two other stages. Therefore 12 single-ended inverters (or 6 fully differential inverting stages) and 24 capacitors are used to build this double capacitevely-coupled (DCC) ring VCO depicted in Fig. 2a. In [11] 3 ROs with 4 inverting stages each are used. These stages are based on differential pairs. The capacitive coupling is done between the sources of the differential pair transistors, using 12 coupling capacitors to achieve a 24-phase oscillator.

The 12-phase oscillators have the advantage of enabling duty cycles and delays in multiples of 1/3, 1/4, 1/6 and 1/12 through the use of AND gates, to obtain the set of signals required in N-path systems. Here, a 12-phase oscillator architecture is proposed, consisting of 4 ROs with 3 stages each but with half the number of coupling capacitors with respect to the previously mentioned design [10] (12 capacitors instead of 24). Figure 2b shows the schematic of the single capacitevely-coupled (SCC) ring VCO proposed. It is shown that this approach results in significant savings in area and power consumption while preserving the phase noise perfor-

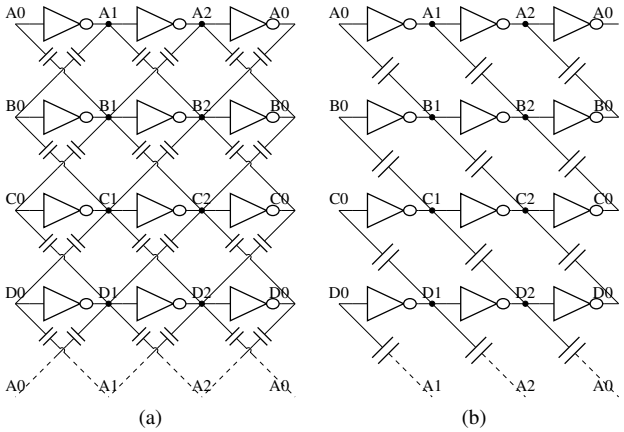

Fig. 2. (a) Double and (b) single capacitively coupled ring VCOs.

mance.

Furthermore, a simple way to identify the possible oscillation modes is discussed, highlighting the need for appropriate setting of initial conditions and verification of the proper operation in the desired oscillation mode. The proposed RO would be particularly interesting for the cases suggested in [7].

The paper is organized as follows. In Section II the proposed 12-phase oscillator is presented and its operation is explained. Then, the design of three different architectures implementing 12-phase ring VCOs are described and compared through simulations in Section III, and the performance of the proposed oscillator is compared against other state-of-the-art works. Finally, the conclusions are drawn in Section IV.

II. Proposed Simplification Technique for Capacitively Coupled Ring VCO

The DCC ring VCO presented in [10], based on a current starved inverter RO structure, is depicted in Fig. 2a.

It achieves very good results in terms of phase noise in comparison with other ROs, since it introduces phase injection-locking via capacitance coupling between four identical inverter based ROs. This circuit generates both phase and quadrature outputs, allowing the designer to produce the specific phase-shifted signals needed to drive the N-path mixer in the system.

In this work, a simplified version of the DCC ring VCO is proposed by removing half of the circuit's capacitances, leading to a single capacitively coupled (SCC) ring VCO, as seen in Fig. 2b. To the best of the authors' knowledge, this design is novel and provides the clear advantage of using significantly fewer components than the DCC version in [10], while maintaining the necessary coupling to generate phase and quadrature signals. With fewer capacitors, the SCC ring VCO achieves lower power consumption than the DCC version, yet retains the benefits of capacitive coupling, particularly the improved phase noise performance compared to a pseudo-differential ring VCO without such coupling, as will be shown in Section III.

By examining the circuit and using a symmetry argument, it can be concluded that all the inverters, being identical,

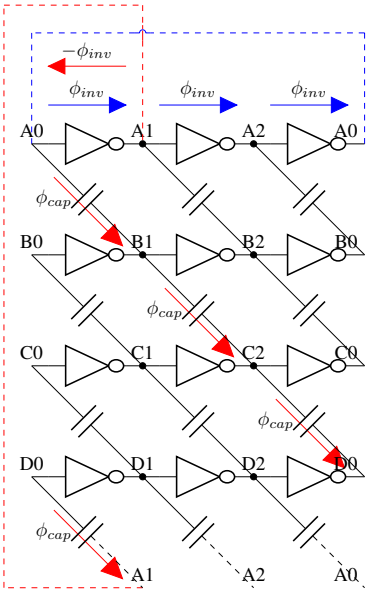

Fig. 3. Circuit schematic of SCC ring VCO, showing the phase shifts introduced by the inverters and the capacitances.

introduce the same phase shift ϕ_{inv}, while all the capacitors C_{coupling}, also identical, introduce the same phase shift ϕ_{cap}. Figure 3 shows the circuit schematic and these phase shifts. Following the blue arrows, starting from A0 and closing the loop, the total phase shift must be a multiple of 2π. Hence, adding the phase shifts of three inverters gives

$$\arg(A0) + 3\,\phi_{inv} = \arg(A0) + 2k_{inv}\pi, \tag{1}$$

where k_{inv} is an integer.

Similarly, adding the phase shift of four capacitances from A0 down to A1 and subtracting the phase shift of an inverter to close the loop, namely following the red arrows, gives

$$\arg(A0) + 4\,\phi_{cap} - \phi_{inv} = \arg(A0) + 2k_{cap}\pi, \tag{2}$$

where k_{cap} is an integer.

From (1) and (2), an expression for ϕ_{cap} can be obtained, given by

$$\phi_{cap} = k_{cap}\,\frac{\pi}{2} + k_{inv}\,\frac{\pi}{6}. \tag{3}$$

For different integer values of k_{inv} and k_{cap}, (1) and (3) yield different solutions for ϕ_{inv} and ϕ_{cap}, leading to various oscillation modes and corresponding phase numbers. Simulations show that, depending on the initial conditions, the oscillator may be forced into certain modes while avoiding others. Additionally, when forced into a 12-phase mode, it can produce phase and quadrature signals at different nodes based on the initial conditions. Therefore, to ensure the oscillator consistently operates as intended in steady state, a startup circuit is necessary for a robust design.

To verify the performance of the SCC ring VCO and compare it with the DCC and pseudo-differential (PD) ring VCOs, simulations were conducted for all three circuits, each optimized to meet the same specifications for a fair comparison.

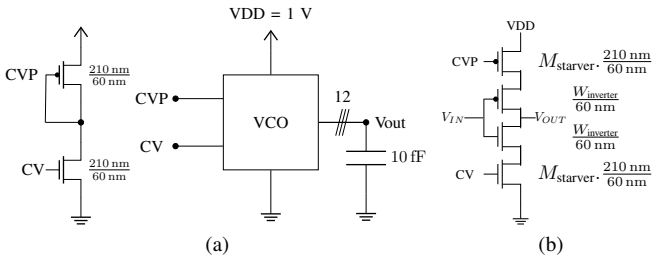

Fig. 4. Simulation test-bench circuit schematics used for the three ring VCO designed. (a) The current mirror to bias the VCO and the loaded VCO. (b) The current-starved inverter cell present in the three VCOs.

III. Performance Evaluation and Comparison of Ring VCO Topologies

This section aims to evaluate the performance of the proposed SCC ring VCO in relation to two established topologies, namely the DCC and PD ring VCOs. The goal is to verify how the SCC design compares to the alternatives, particularly in terms of power consumption and phase noise, while ensuring all designs meet the required specifications, namely operate over a frequency range from 0.3 GHz to 3 GHz with a power supply voltage of 1 V and a control voltage of 0 to 1 V in 28 nm FD-SOI CMOS process. The transistor channel length is set to 60 nm, suitable for analog circuit design. The designs are optimized to minimize power consumption at 3 GHz, while driving a 10 fF capacitive load at each of the 12 outputs. This load size represents the typical input capacitance of the buffer stages connected to the outputs.

Figure 4 shows the test-bench circuit schematics used to simulate the three ring VCOs. In Fig. 4a the current mirror to bias the VCOs is depicted. The input CV is fed to the current mirror and to the VCO. The voltage CVP is generated by the current mirror and fed to the VCO.

On the other hand, Fig. 4b shows the circuit schematic of the inverter cell used for all the ring VCOs designed. It is implemented using parallel arrangements of M_{starver} transistors, each with a width of 210 nm, as noted in the circuit schematic. The nMOS transistors are sized equally to the symmetric pMOS transistors. Both M_{starver} and the transistor width of the inverting transistors in the inverter cells, W_{inverter}, are swept through simulations to determine the value that minimizes power consumption for the SCC and DCC ring VCOs. In the case of the PD ring VCO, presented in Fig. 1, a third parameter is also swept, namely the width of the transistors that implement the coupling latches, W_{coupling}.

For both SCC and DCC ring VCOs, the coupling capacitance C_{coupling} is fixed at 9.5 fF. Smaller values are avoided to maintain a robust design, ensuring that parasitic capacitances from the routing and transistors remain negligible in comparison. Moreover, 9.5 fF is the smallest capacitance available in the PDK library.

Table I shows the design variables that optimize each design for minimum consumption at 3 GHz.

Figures 5 and 6 present the simulation results for power consumption and phase noise, respectively, for the three VCO designs.

TABLE I
Optimal Design Variables for Simulated VCOs

	W_{inverter} (µm)	M_{starver}	C_{coupling} (fF)	W_{coupling} (nm)
SCC	1.6	6	9.5	N/A
DCC	2.2	20	9.5	N/A
PD	3.5	22	N/A	210

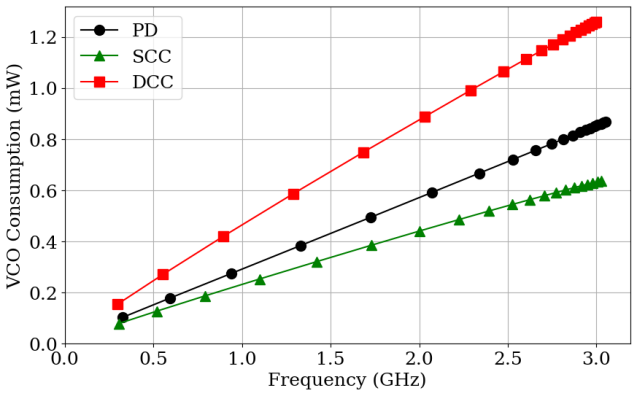

Fig. 5. Simulation results showing the power consumption of the three designed ring VCOs over frequency. The static power consumption of the current mirror depicted in Fig. 4a is excluded.

It is seen that the SCC ring VCO outperforms the other VCOs in terms of power consumption and achieves a phase noise performance very similar to the DCC ring VCO in most of the frequency range. However, from 2.5 GHz to 3.0 GHz the phase noise of the SCC ring VCO is higher than that of the DCC ring VCO.

The initial DCC ring VCO design consistently produced only 6 distinct phases, and no adjustments to the initial conditions could force it into a stable 12-phase mode. To address this, the authors increased the width of the inverter transistors (W_{inverter}), resulting in a modified DCC ring VCO that generates 12 evenly spaced phases. However, this modification led to higher power consumption and a reduced frequency tuning range. Simulations confirmed that the modified DCC design could operate in both 6-phase and 12-phase modes,

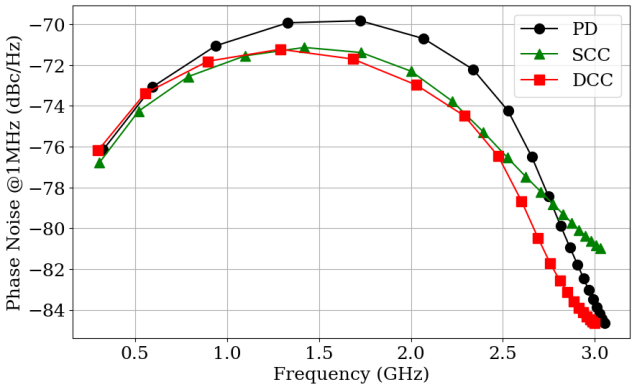

Fig. 6. Simulation results showing the phase noise at 1 MHz frequency offset of the three designed ring VCOs over frequency.

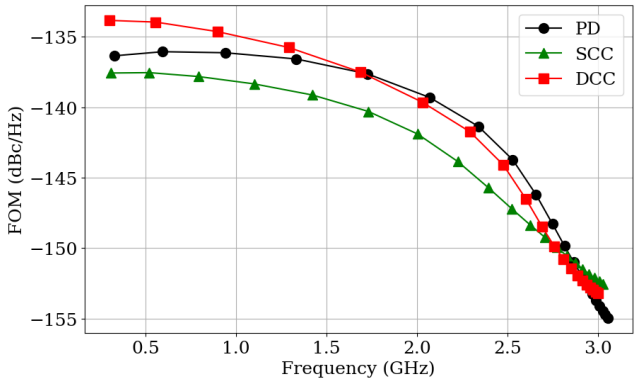

Fig. 7. The FOM in (4) for the three designed ring VCOs over frequency.

with identical power consumption and phase noise in each. For a fair comparison, the original DCC design, which offers competitive power consumption, was used in 6-phase mode.

A Figure of Merit (FOM) accounting for power consumption, phase noise and number of phases (i.e., the number of nodes exhibiting signal with different phases) is defined as a function of frequency as

$$FOM(f) = PN(f) + 10\log\left(\frac{12}{N} \times \frac{P(f)}{1\,\text{mW}}\right) - 20\log\left(\frac{f}{1\,\text{MHz}}\right). \quad (4)$$

Figure 7 shows the FOM in (4) for the three designs.

The averaged FOM over frequency, expressed in dBc/Hz, was calculated for each VCO design. The SCC ring VCO achieved the best performance in most of the frequency tuning range.

As a result, the SCC ring VCO outperforms the other designs in terms of phase noise efficiency, delivering better phase noise performance relative to power consumption across the frequency range.

In terms of minimum estimated area, the 9.5 fF capacitors occupy $3.354\,\mu\text{m} \times 3.354\,\mu\text{m}$ each, resulting in a total capacitor area of $135\,\mu\text{m}^2$ for SCC and $270\,\mu\text{m}^2$ for DCC. Meanwhile, the total transistor channel area is $4.46\,\mu\text{m}^2$ for SCC and $10.37\,\mu\text{m}^2$ for DCC. Thus, the overall estimated area, including both capacitors and transistors, is $139\,\mu\text{m}^2$ for SCC and $280\,\mu\text{m}^2$ for DCC.

Table II compares state-of-the-art coupled ring VCOs, including capacitively-coupled designs [10], [11] and inverter-coupled designs [8], [12].

The SCC ring VCO design achieves the lowest power consumption compared to other designs. Its FOM is comparable to that of [8], which was developed in the same 28 nm technology. All three presented designs were optimized to minimize power consumption, which led to higher phase noise as a trade-off.

Nevertheless, given that the SCC ring VCO design is competitive among the three in terms of overall performance, it would be worthwhile to optimize it specifically for phase noise reduction to explore potential improvements.

IV. Conclusion

The proposed SCC ring VCO reduces the number of capacitors by half, conveying a smaller silicon area, while maintaining phase noise improvements compared to the DCC design. Moreover, it achieves the lowest power consumption among the state-of-the-art designs taken into consideration, with phase noise performance comparable to the DCC across the frequency tuning range.

Further optimization could focus on enhancing phase noise performance while preserving power efficiency to meet more restrictive phase noise specifications in communication systems.

The analysis indicates that improper design may result in unwanted oscillation modes, making the inclusion of a startup circuit essential. Future work should explore the predictability of oscillation modes and their steady-state behavior. Investigating the influence of inverter and capacitor coupling on oscillation modes could deepen the understanding of circuit behavior and improve the overall figure of merit (FOM) of the SCC VCO.

TABLE II
State-of-the art of ring VCOs

	[10] **	[11] **	[12] **	[8] **	SCC ***	DCC ***	PD ***
Process (nm)	40	130	65	28	28	28	28
Number of Phases	12	24	8	4	12	12	12
Frequency tuning range (GHz)	0.8 - 28.2	1 - 1.5	5 - 8	0.7 - 2.78	0.3 - 3.0	0.3 - 3.0	0.3 - 3.0
Frequency tuning range (%)	97.9	33.3	42.9	120	108	108	108
Center frequency (GHz)	28	1.5	7	1.76	2.5	2.5	2.5
Power (mW)	0.88	13.8	4.3	1.1	0.54	1.06	0.72
Phase noise (dBc/Hz) @ 1 MHz	-120*	-110.2	-150*	-95.7	-76.5	-76.5	-74.2
$\lvert FOM_{OSC}\rvert$ (dBc/Hz)	209	165	219	155	147	144	144
$\lvert FOM_{VCO}\rvert$ (dBc/Hz)	229	175	232	176	168	165	165

*: Estimated from paper. **: Measurement results. ***: Simulation results.

$$\text{Frequency tuning range}\,(\%) = \frac{100 \cdot \text{Frequency tuning range}}{\text{Center frequency}}.$$

$$FOM_{VCO} = FOM_{OSC} - 20\log\left(\frac{\text{Frequency tuning range}\,(\%)}{10}\right).$$

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