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Design of DC/DC Switched Capacitor Monolithic Converter for ultra low Power

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To know that we know what we know, and to know that we do not know, that is true knowledge.

Nicolaus Copernicus

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Abstract

Integrated DC-DC switched capacitor converters are a subgroup of DC-DC converters that utilize only switches and capacitors to realize the desired voltage conversion. Unlike inductor-based converters that store energy by way of a magnetic field, the energy in a switched capacitor converter is stored by means of an electric field between the capacitor plates. Not utilizing inductors makes them ideal for integrated circuits Power Management, given that the use of inductors is inconvenient in integrated circuits [1]. Switched capacitor converters have been used historically to obtain the necessary voltage for programming FLASH type memories [2], voltages for the RS232 communication standard, and also powering LED-based lighting systems. More recently interest in fully integrated System on Chip(SoC) and reduction in the final size of products have popularized the use of these converters. A cellphone system has multiple continuous voltage domains that feed different parts of the system, all powered by only a battery whose voltage varies with its charge. The rise in number of transistors per unit-area of silicon has come with rising power dissipation, which must be managed. Combined with high power demand from the battery by laptops and cellphones or the Ultra Low Power(ULP) devices for Internet of things(IoT) or Active Implantable Medical Devices(AIMDs) has stimulated the use of Dynamic Power Management techniques like Dynamic Voltage Scaling(DVS) directed to satisfying all power demands of a fully integrated system in a tight budget. All of this has created an area of research in Power Management where DC-DC switched capacitor converters play a significant role.

This work is focused on the development of a monolithic switched-capacitor converter in a CMOS SOI technology of 1.8V. It consists in the design of a limited-energy system Switched-Capacitor DC-DC Converter working in SSL(Slow Switching Limit), powered by a battery and oriented to the ULP. The three main points of this work are the following, first to build a multi-phased architecture converter, which helps to reduce output ripple. Second, that power consumption is proportional to the switching frequency even for very low power delivered to the load. This enables the converter to maintain high efficiency for low output power loads. And lastly, to have a fast response to a load current step, this is important as the majority of loads will be digital circuits that consume a high current for a short time at the clock edge, this enables the system to reduce the size of the output filtering capacitor, facilitating the full integration of the system.

Furthermore, a novel optimization strategy was developed in order to determine the sizing of the converter components. The only other work done on the subject is [3], as far as the author is aware. This work is more general in the sense that it applies to all converter topologies, but it assumes the converter always operates in the intersection between SSL and FSL, because this point is optimum for a desired load and efficiency. It does not consider a varying load, where the converter should be able to work in a range of different loads and frequencies. This works

intends to solve the problem of optimum sizing so that the converter can operate successfully in a range of conditions and always satisfy its constrains.

Preface

This work is part of the project I3: "Wirelessly Powered Integrated Platform for biomedical wearable and implantable devices" as part of "Applied Investigation Project Maria Viñas - 2017" financed by ANII. These last decades have seen a rise of *"Active Implantable Medical Devices"*(AIMDs) such as pacemakers, electrical stimulators, and prostheses. To this one can add less invasive devices such as wearables that are highly implemented in sensing and tracking of biological signals and parameters, they would allow for a 24/7 monitor of patients. As these devices operate with a portable power source they have a limited Power Budget, the Project was aimed at solving the power challenges faced by these devices. The I3 Project undertook 3 main parts of the Power Management:

Design of digital sub-threshold circuity: To reduce power, digital circuits operating under nominal voltage have been implemented in the last decades. The dynamic power consumption decreases with the square power of voltage. This reduction of power is paid with reduced speed, so operating frequency must be lowered. As operating time increases so does static power, this leads to an optimal voltage where power is minimal. This strategy was evaluated for the digital computations in this Project.

Wireless Power Transfer: Although Wireless Power Transfer records go back to Tesla in the 1800s, new interest has sparked recently, it is of particular interest for AIMDs as accessing the devices implies a surgical procedure. Some classical devices as pacemakers are designed so that the battery lasts for the entire lifespan of the device, so that charge is not needed. But other devices with heavier energy demands as neuron stimulators must be charged regularly. Near-field inductive coupling is the widest implemented strategy as it is in this Project. The study of fast and efficient rectifiers, as well as control strategies to optimize the efficiency of the Wireless Power Transfer link, were undertaken.

DC/DC Converters: Finally the 3rd area of study as well as the subject of this work is the implementation of the dc-dc power conversion. To adapt the wireless induced voltage or the voltage from an energy harvesting system to the system nominal voltage a DC/DC block is needed. Furthermore, to implement the reduced voltage, power management strategies, previously listed, a DC/DC block is also needed. With this in mind, power-efficient topologies oriented to ultra low power were studied.

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Contents

Glossary

A_C Capacitance Area. 30

A_{sw} Switches Area. 30

A Maximum Area, result of minimizing Power. 30

C_{bott} Capacitance of the modular converter that is connected between voltages $V_{in}/3$ and ground in a particular switching instant. 25

C_{fly} Capacitance that switches between different node voltages. x, 9, 13, 17, 19, 30, 31, 35, 36, 43, 46

C_{mid} Capacitance of the modular converter that is connected between voltages $2/3V_{in}$ and $V_{in}/3$ in a particular switching instant. 25

C_{out} Capacitance seen by the load. 6, 9, 27, 41, 43, 44, 91

C_{ox} CMOS Metal oxide semiconductor capacitance per unit of area. 28

C_{top} Capacitance of the modular converter that is connected between voltages V_{in} and $2/3V_{in}$ in a particular switching instant. 25

E_{loss} Energy lost when 2 capacitors are short-circuited. 9

I_D CMOS Drain Current. 4

I_s Reverse Saturation Current. 4

I_{bias} Polarization Current of Analog Circuity. 5

I_{out} Output Current. 5, 6

L_{eff} CMOS effective channel length. 4

L_{min} Minimum channel Length of CMOS transistor. 28

N Number of Phases of Converter. x, 17, 27, 31, 34, 35, 36, 37, 38, 45, 114

P_{TBPC} Power loss due to charge/discharge of top botton capacitance. 28

$P_{\Delta V}$ Power loss due to capacitance short-circuit. 27, 36

P_{osc} Power consuption of oscillator. 28

P_{sw} Power loss due to driving the switches. 28

P Maximum Power, result of minimizing Area. 30

Q 1/3 of Charge delivered by source to converter, as well as by converter to load, in steady state. 25, 26, 31, 36

R_{FSL} Equivalent Output Resistance of Converter in Fast Switching Limit. 11, 13

R_{SSL} Equivalent Output Resistance of Converter in Slow Switching Limit. 11, 14

R_{out} Equivalent Output Resistance of Converter. 11, 12, 13, 17, 80, 82

R_{sw} On Resistance of CMOS switch. 27

S_{gnd} Switch that connects capacitor cell with ground. 40

S_{inter} Switch that connects capacitor cell with another higher voltage capacitor cell. 40

S_{in} Switch that connects capacitor cell power source. 40

S_{out} Switch that connects capacitor cell output node. 40

U_T Thermal Voltage. 4

V_P Pinch-off Voltage. 4

V_{DD} Nominal Voltage. 4, 46, 60, 66, 68

V_{DS} CMOS Drain to Source Voltage. 4

V_{NL} Output voltage when load current is null. 10, 12, 15, 17, 25, 36, 80

V_{bott} Voltage of capacitor that is connected between voltages $1/3V_{in}$ and ground in a particular switching instant. 26, 42

V_{in} Voltage input of Converter. 5, 6, 9, 26, 40, 88, 96

V_{mid} Voltage of capacitor that is connected between voltages $2/3V_{in}$ and $1/3V_{in}$ in a particular switching instant. 26, 42

V_{out} Voltage output of Converter. 5, 6, 9, 12, 17, 25, 29, 35, 36, 37, 38, 66, 79, 80, 81, 88, 96, 114

V_{ref} Reference Output Voltage of Converter. 6

V_{tn0} Threshold Voltage of N-type transistor. 28

V_{top} Voltage of capacitor that is connected between voltages V_{in} and $2/3V_{in}$ in a particular switching instant. 26, 29, 42, 113

V_{tp0} Threshold Voltage of P-type transistor. 28

W_{min} Minimum Width of channel of CMOS transistor. 31, 34

W Width of channel of CMOS transistor, in this work width of switches as optimization variable. x, 4, 28, 31, 34, 35, 36, 37, 38, 114

X Optimization Variable where $X = [W, N, f_{sw}, C_{fly}]$. 30, 31

ΔV Voltage difference between to capacitors before being short-circuited. 9, 28, 29, 30, 35, 36, 80, 96

δ_n Deplition to oxide capacitance for NMOS transistor. 28

δ_p Deplition to oxide capacitance for PMOS transistor. 28

η Converter Power Efficiency. 5

μ_n Electrical mobility of N-type semiconductor. 28

μ_p Electrical mobility of P-type semiconductor. 28

a_T Total Converter Area. 30, 34

f_{sw} Switching frequency of Converter. x, 12, 27, 30, 31, 34, 35, 36, 52, 63, 79, 81

g_{dsn} On Conductance of NMOS transistor in a switch. 28

g_{dsp} On Conductance of PMOS transistor in a switch. 28

g_{ds} On Conductance of CMOS switch. 27

n_p Charge carrier density of N-type semiconductor. 28

n_p Charge carrier density of N-type semiconductor. 28

p_T Total Converter Power consuption. 30, 34, 35

v_{ripple} Ripple Voltage of Converter Output. 35

BPC Botton Plate Capacitance. 28

CCO Current Controlled Oscillator. 28, 39, 65

CERO Cero Energy Per Cycle Ring Oscillator. viii, 59, 61, 63

CSRO Current Starved Ring Oscillator. viii, 57, 62

DVFS Dynamic Voltage Frequency Scaling. 5

DVS Dynamic Voltage Scaling. iii

FSL Fast Switching Limit. vii, 12, 17, 18, 113

GP Geometric Problem. 31

LDO Linear Dropout Regulator. 5

SCC Switched Capacitor Converter. vii, viii, 5, 6, 9, 10, 11, 12, 13, 25, 26, 28, 30, 32, 34, 36, 38, 61, 97, 98, 113

SCN Switched-Capacitor Network. 18

SSL Slow Switching Limit. iii, vii, 11, 13, 14, 15, 16, 17, 18, 23, 27, 79, 103, 113

TBPC Top Botton Plate Capacitance. 28

TPC Top Plate Capacitance. 28

ULP Ultra Low Power. iii, 90

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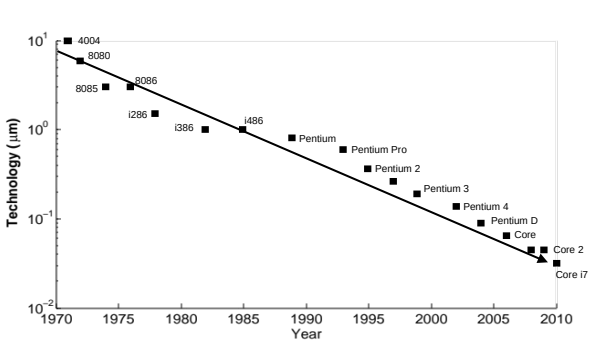
Chapter 1

Introduction

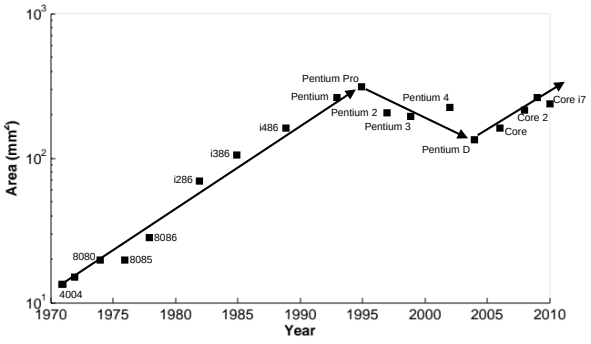
1.1 Power Trends

Although Moore's Law might be coming to an end, computational power will continue to increase, as it is required by society, and new methods are been developed constantly to increase computational power without depending on transistor technology [4]. [5]. But this computational power comes with a price in the form of electrical power, in 2007 the electrical power consumption of ICT Devices per capita exceeded the 100kWh/year [6], although much comes from large Data Centers, Data Centers are estimated to consume more than 200TWh/year, around of 1% of energy Worldwide [7]. As of 2021 Mining Bitcoins consumes more energy than Argentina(121TWh/year), according to a Cambridge Study [8].
There are 3 challenges that Power Management faces in the modern Era [9]:

Power Density With the increase of transistors per unit area, there has been a power density rise, Fig.1.1.3. For some time now design has hit a "Power Wall" given by the physical constraint of silicon thermal constant. To mitigate this different refrigeration methods have been implemented, however, this presents a high added cost, which leads to considering strategies of power managing.

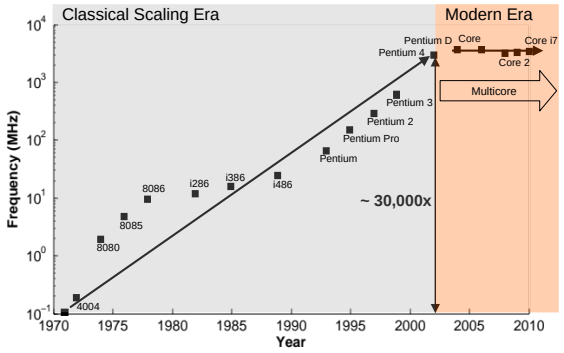


Technology Node Trend [10]

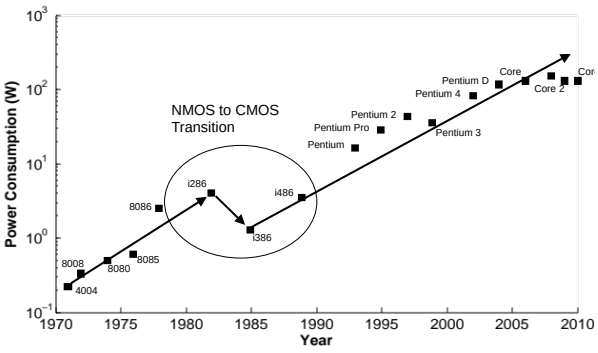


Chip Area Trend [10]

Figure 1.1.1: Trends I



Frequency Trend [10]



Power Trend [10]

Figure 1.1.2: Trends II

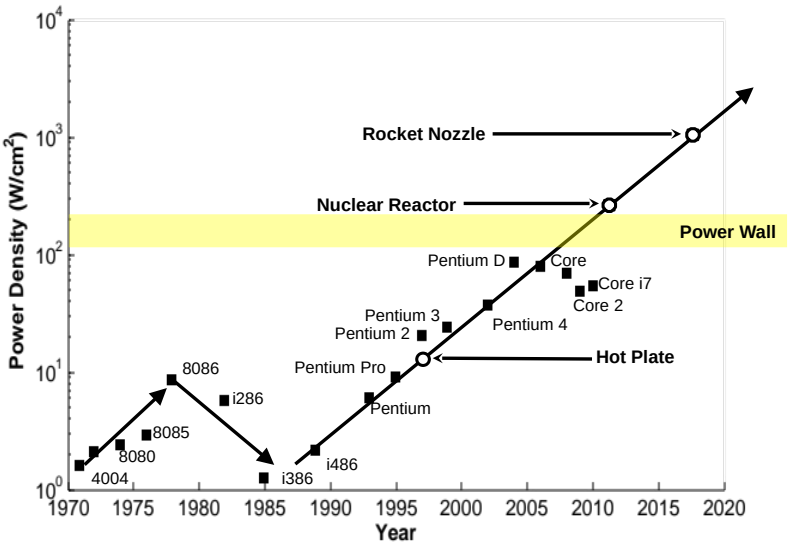


Figure 1.1.3: Power Density Trend [10]

Voltage Scaling In Fig.1.1.4 we see the tendencies of technology CORE nominal voltage with time. This presents a problem for battery-powered systems, nominal battery voltage goes from 1.2V for NiMH to 3.6V for Li-Ion batteries. Furthermore for example Li-Ion batteries can have a voltage between 3V to 4.2V depending on the battery charge. Figure 1.1.4 we see how voltages for modern technologies are below the Volt, making a power conversion inevitable.

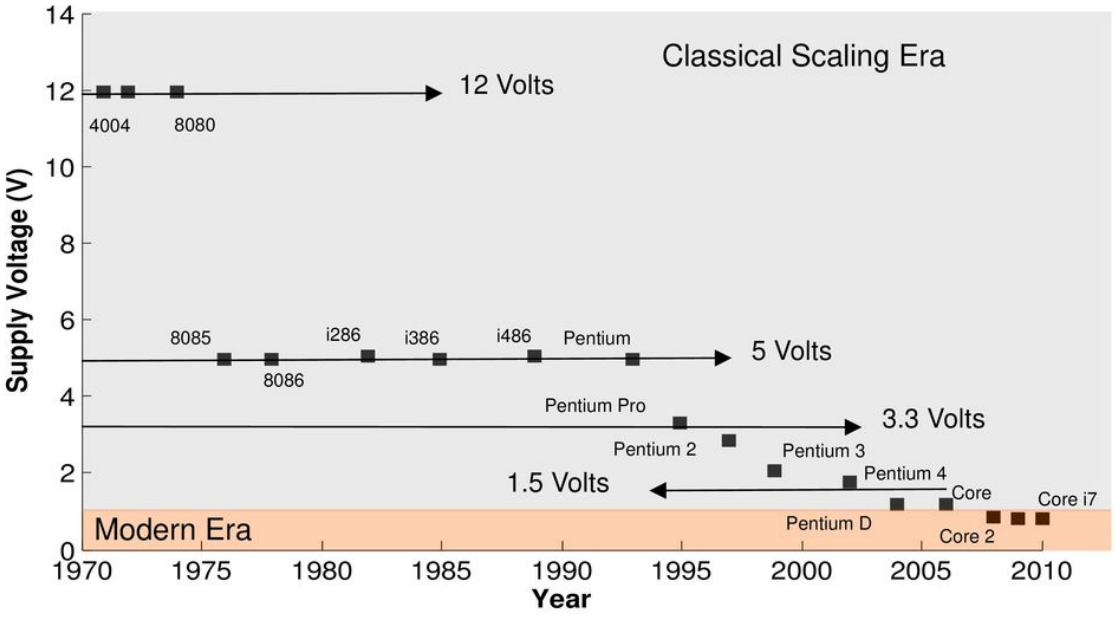


Figure 1.1.4: CORE Nominal Voltage Evolution [10]

Battery Capacity Furthermore, the human factor is if not decisive at least highly influential, with the rise of computational capacity has come the popularization of portable devices and the high use and computational demand of these portable systems has increased the power demanded from their batteries. Fig.1.1.5 shows a graphic with the general energy consumption in an interval of two days against the energy capacity of a $1cm^3$ battery. Since 2007, with the dissemination of smart cell phones, the energy demand has overcome the batteries capacity.

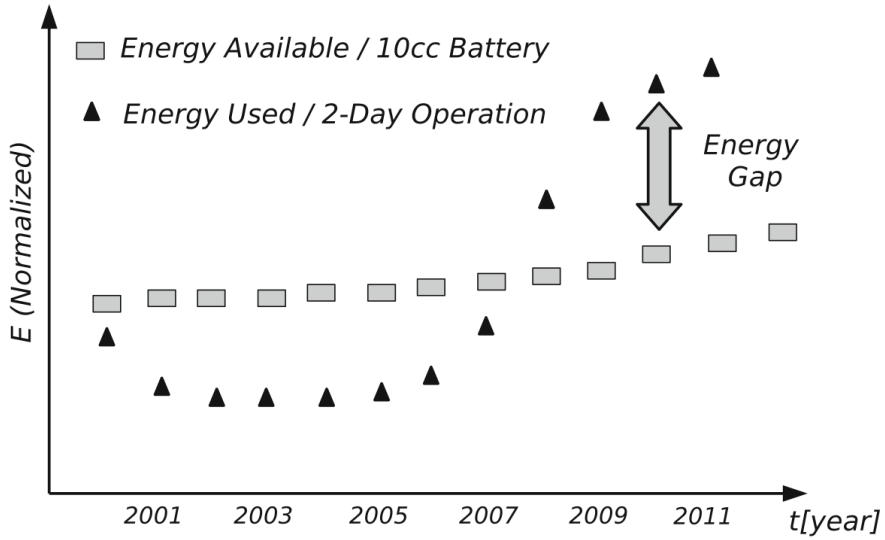


Figure 1.1.5: Energy Demand against Battery Capacity [9]

1.2 Power in DC-DC Converters

Power consumption in an integrated circuit can be divided between analog circuit and digital circuit power consumption.

Analog Power In Analog Circuits the power consumption is determined mainly by bias currents:

$$P_{analog} = \sum_i V_{DD_i} Ibias_i \tag{1.1}$$

However, excepting radio frequency transmitters/receivers, in most cases the majority of the power is consumed by digital circuits, this power can be divided into 3 parts:

Dynamic Consumption The greater part of power is consumed by the charge and discharge of the node capacitance C_{gate_i} that switch between V_{DD} and $0V$ at frequency f_{clk_i} and a Duty Factor D_i. This power is given by 1.2 and is present only when the clock is active in synchronous logic circuit or an input changes in combinational logic circuits.

$$P_{Dynamic} = \sum_i D_i C_{gate_i} V_{DD_i}^2 f_{clk_i} \tag{1.2}$$

Shoot-Through Current Consumption This power loss is also only present when a node switches from one state to another and is relevant when signals that drive the transistors gates are slow. The loss is given by a direct path from the power source to ground that exists when both a nMos and pMos transistors connected in series between source and ground are active at the same time. This power loss is significant in a Ring Oscillator operating at low frequency as will be seen in chapter 5.

Leakage Current Power Consumption This consumption is the only present when there is no node switching from one state to another, it's is given by transistor subthreshold currents being not null. The subthreshold currents equation is given by 1.3 and represents a substantial percentage of total power in modern technologies.

$$I_D = \frac{W}{L_{eff}} I_s e^{V_P} \left(1 - e^{\frac{-V_{DS}}{U_T}}\right) \tag{1.3}$$

1.3 Power Management Techniques

Clock Gating [11] The classical form of saving power in digital circuits is to shut down the clock signal in the parts of the system that are not processing data, this is called Clock Gating, preventing the Flip Flops of these circuits from being clocked unnecessary so that the Dynamic and Shoot-Through Current consumption is not present. Data is retained as supply voltage remains high but also Leakage Current losses remain present.

Dynamic Voltage and Frequency Scaling(DVFS) [12] Frequently the maximum operating frequency is not necessary to meet the minimum time requirements. Reducing the frequency is a basic method to reduce Dynamic Power given by 1.2, another alternative is to reduce the supply voltage, which 1.2 depends on quadratically. As the propagation time is inversely proportional to the voltage supply the frequency must be scaled in an equal manner, to maintain the Propagation Time-Period relation, therefore voltage scaling must be done along with frequency scaling. DVFS is done through software and is conservative by nature so as to always meet the time requirements, a more advanced way of DVFS is to perform adaptive scaling in a feedback control manner, where a control unit assesses the power demand and sets the optimum frequency.

In order to achieve greater Power efficiency by DVFS, it is necessary to have a way of modifying the supply voltages, this introduces the necessity of DC/DC Voltage Converters.

1.4 DC-DC Converters

Linear Dropout Regulator(LDO) An LDO Regulator is an active linear circuit as the one in Fig.1.4.1, where the dropout voltage refers to the voltage between input and output. This type of Regulator is mostly used to convert an unstable and noisy voltage source into a well-regulated power output. They are simple and easy to implement, their drawback is that the efficiency is inversely proportional to the difference between input and output voltage Eq.1.4, so when there is a considerable voltage difference this type of Voltage Conversion is not used.

$$\eta = \frac{V_{out}}{V_{in}(1 + I_{bias}/I_{out})} \tag{1.4}$$

Switched Inductor Converter The majority of DC/DC Converters are based in Switched Inductive Converters, where the inductor act as an energy storage intermediate between the two voltage domains. This type of converter has high efficiency and can provide great power output. Fig.1.4.2 shows a typical Buck-Boost Converter, which can deliver output voltages higher or lower than its input. The energy is stored in the inductor, in the way of a magnetic field, to transfer power between input and output voltage levels. But in the search for miniaturization and SoC(System on Chip) solutions they present a problem as the footprint of a passive off-chip inductor is quite large and integrated inductors have low-quality factors which lower the converter efficiency.

Switched Capacitor Converter An alternative converter is a SCC(Switched Capacitor Converter), this converter uses capacitors and electric fields in place of inductors and magnetic

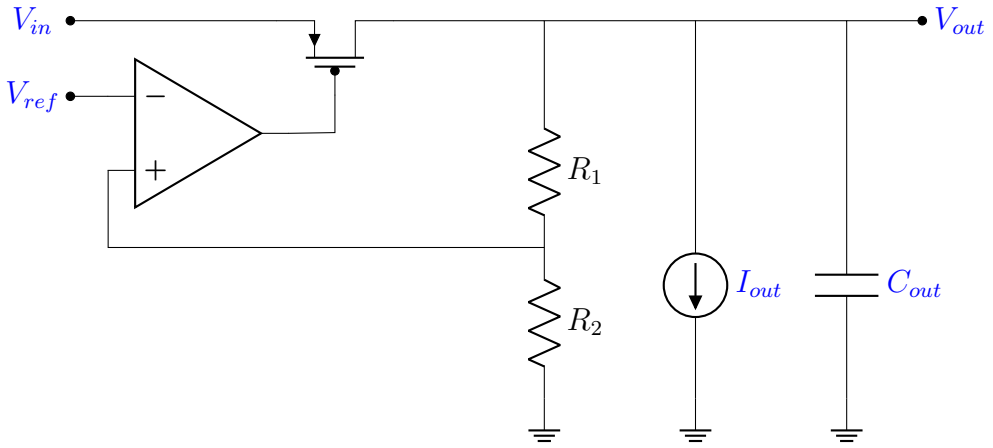


Figure 1.4.1: Low Dropout Linear Regulator

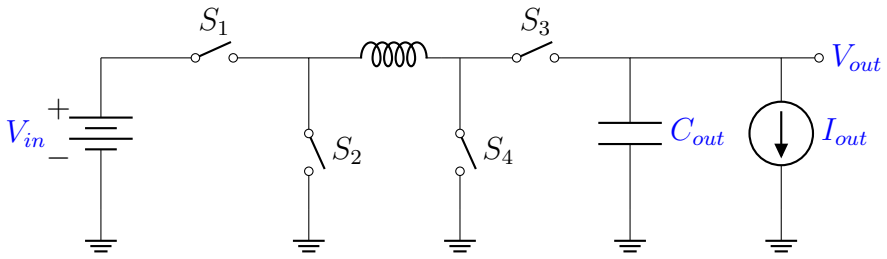


Figure 1.4.2: Switched Inductor Buck-Boost Converter

fields to store energy. The advantage of SCC is that capacitors have a greater energy density than inductors and can be integrated with good quality factors [1], [13].
Modern Ultra-Low Power applications as IoT sensors, Wearable or Implantable Medical Devices may employ Energy Harvesting Schemes [14] to extract power from the environment, like solar, vibration or thermal. But the voltages extracted through these schemes are very low and can fluctuate considerably bases on the power source intensity and availability, to obtain a steady nominal voltage a DC-DC conversion is needed. Also for battery-powered devices, the battery voltage fluctuates as the charge depletes, so voltage conversion might be necessary. In cases where a high degree of integration is desirable, a SSC is a good alternative.

Power in DC-DC switched capacitor converters is conformed of the three types seen in 1.2, where analog and leakage losses are constant, so are more dominant at low frequencies. Shoot through current losses happens only at low frequencies, therefor all three will determine low frequency power. On the other hand at high frequencies, dynamic losses are greater, as they grow with frequency. Dynamic losses can be divided in three:

- Logic switching losses: these losses correspond to logic circuity power.
- Power switching losses: which drive the power switches that connect to the capacitors
- Top-bottom capacitance losses: due to charging-discharging of parasitic capacitors to bulk, when a capacitance nodes are changed.

In the next chapters, the design of a modular interleaved switched-capacitor converter will

be laid out. Interleaved Capacitor Modulator is a Multi-phasing techniques, where several converters are connected in parallel in order to reduce ripple and eliminate the need of and output capacitance. There were no hard specs for the converter, but from now on it would be assumed that the desired output voltage is between $0.2V$ and $0.5V$ and the load current can vary from a maximum of $1mA$ to zero.

$$V_{out} = [0.2, 0.5]V$$
$$I_L = [0, 1m]A$$

In Chapter 3 a novel type of optimization method is demonstrated to determine the parameters of a DC-DC switched capacitor converter. Chapter 4 presents the main blocks of a Modular Interleaved Converter. In Chapter 5 the problem that ring oscillators present to converter efficiency at low loads is explained and it is shown how the proposed oscillator topology avoids these problems. Lastly, in Chapters 6 and 7 the Feedback strategy to control output voltage is analyzed, both a transconductor based linear feedback loop and a non-linear comparator-based feedback loop are analyzed. In 8 the full converter is evaluated, its main problems are presented and possible solutions are proposed.

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Chapter 2

DC/DC Switched Capacitor Converters

2.1 Introduction

In this chapter we will analysis the theoretical functioning of Switched Capacitors Converters. Including the classic Topologies used, how are output voltages defined, the main techniques for determining the efficiency of the converter and the control strategies as well as modern techniques to address some of the problems presented in switched capacitor converters.

2.2 Topologies

The basic idea behind SCC is connecting capacitors in convenient ways as to charge them at one voltage level:V_{in} and discharge them at another voltage level: V_{out}. If $V_{in} \geq V_{out}$ this can be done simply connecting one capacitor C_{fly} to V_{in} in the first phase of the period and then connecting it to V_{out} in the second phase. This would achieve charge transfer from V_{in} to V_{out}, assuming the output is another output capacitor: C_{out}, the charge transfer is achieved by short-circuiting two capacitor with a voltage difference:$\Delta V = V_{C_{fly}}^{S_1} - V_{C_{out}}^{S_1}$. In the example of Fig.2.2.1 ΔV will be the voltage difference between C_{fly} and C_{out} before they are short-circuited in parallel to each other. Short-circuiting 2 capacitor with different voltages implies an energy loss as given by Eq.2.1, the energy loss is proportional to the square of the voltage difference between the capacitors, because of this it is better to not have a too large ΔV. However, the amount of charge transferred also depends of ΔV, this introduces an intrinsic limitation in the efficiency of the converter as will be seen later. The energy lost is dissipated in the switches resistance, no matter how low this resistance is the energy disipated is always the same. As the lower the switches resistance the greater the current peak at time of switching. If the switching frequency is much lower than the RC contant of the circuit, then the RC charge/discharge always converges, therefore power is a constant depending only of voltage.

$$E_{loss} = \frac{C_{fly}C_{out}}{C_{fly} + C_{out}} \frac{\Delta V^2}{2} \tag{2.1}$$

Series Parallel 1/2 Converter In Fig.2.2.2 a converter that divides the input voltage by two is shown, Eq.2.4 proofs the steady state no load value of V_{out}, see Appendix D for full proof

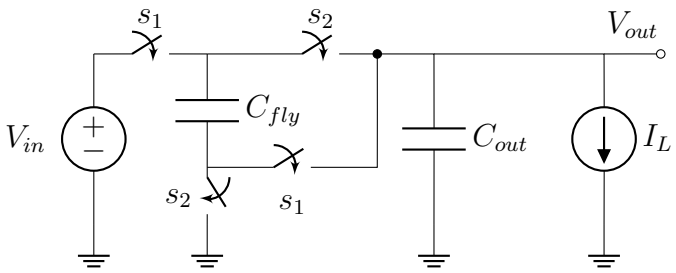


Figure 2.2.1: Intrinsic Power Loss in Capacitor charge transfer

including transitory.

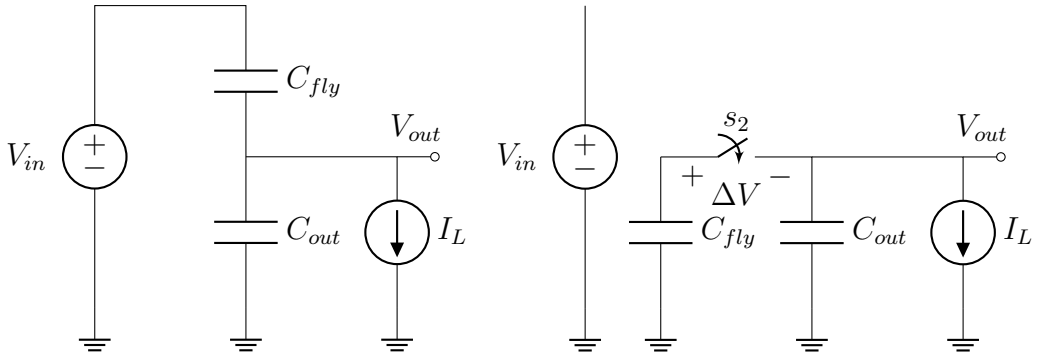
$$(V_{in} - V_{out})C_{fly} + V_{out}C_{out} = (C_{fly} + C_{out})V_{out} \tag{2.2}$$

$$(V_{in} - V_{out})C_{fly} = C_{fly}V_{out} \tag{2.3}$$

$$V_{in}\frac{C_{fly}}{2C_{fly}} = V_{out} \tag{2.4}$$

Note that this result is independent of value of C_{out}.

The basic strategy is changing the capacitor from series to parallel or vice versa in order to form the input and output voltages. This way if $V_{out} = V_{in}/2$, then $\Delta V = 0$ and there is no power loss, but there is also no charge transfer, this output voltage when there is no charge transfer is call: *No Load Voltage* V_{NL}. The idea is to have output voltages close to V_{NL} to have low power loss. This converter is appropriate to V_{out} a little under $V_{in}/2$.



subfigure Series

subfigure Parallel

Figure 2.2.2: Series Parallel Converter

Next are presented figures of the classical Switched Capacitor Converter (SCC) topologies, where it is assumed that a capacitor C_{out} is connected to V_{out} and hold the output voltage in switching phase Φ_1.

Note that the series-parallel case in Fig.2.2.7 is different from the case of Fig.2.2.2, in Fig.2.2.7 case all capacitors switch voltages, and in this case V_{out} will be a function of the capacitors values.

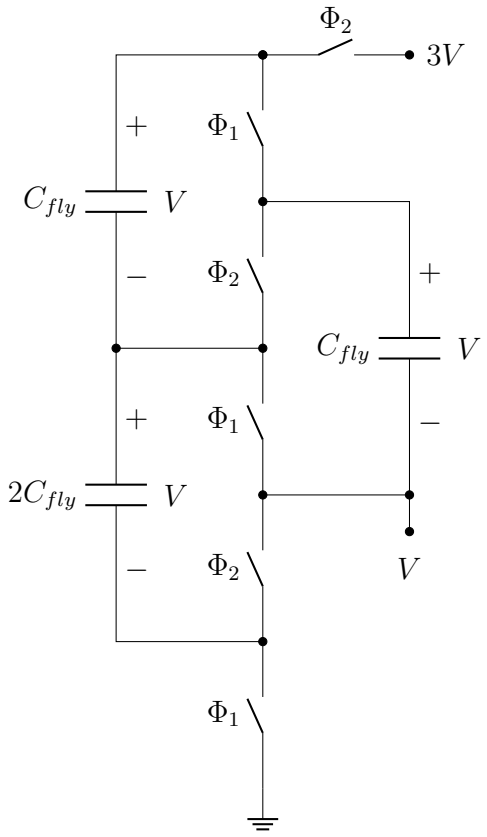


Figure 2.2.3: Ladder Converter

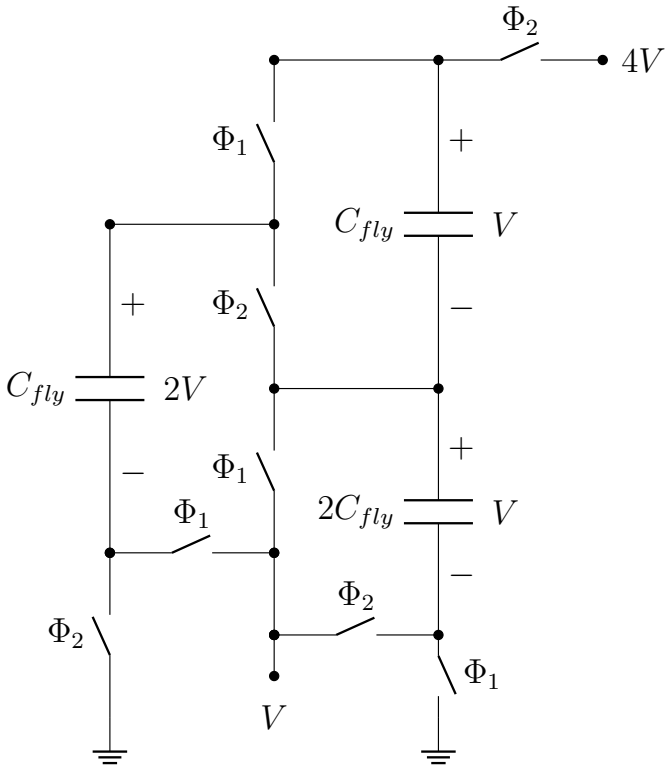


Figure 2.2.4: Dickson Converter

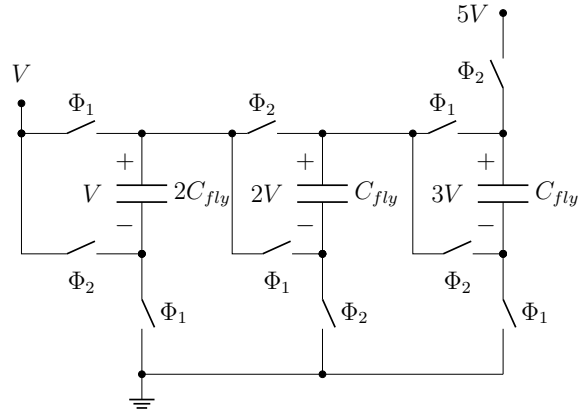


Figure 2.2.5: Fibonacci Converter

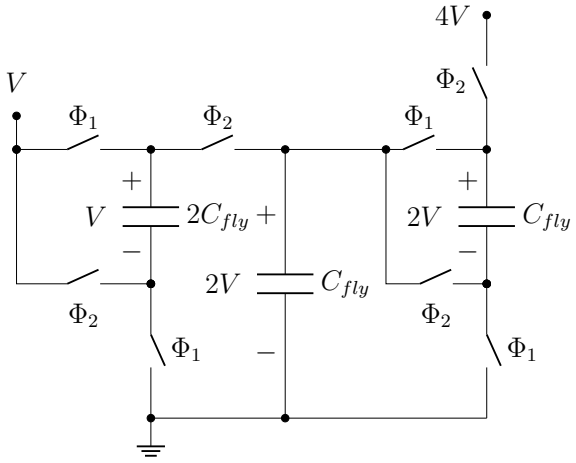


Figure 2.2.6: Double Converter

2.3 Charge Flow Analysis

A SCC can be modeled as no-load voltage source and an output resistance as shown in 2.3.1. As shown in [15] the output resistance of a SCC is a function of frequency, see Fig.2.3.2.

At low/high frequencies R_{out} behaves asymptotically tending to R_{SSL}/R_{FSL}. Where in SSL the RC constant of Switch/Capacitor is much smaller than switching frequency, the converter losses are dominated by capacitor short circuit and are independent of Switch Resistance. While

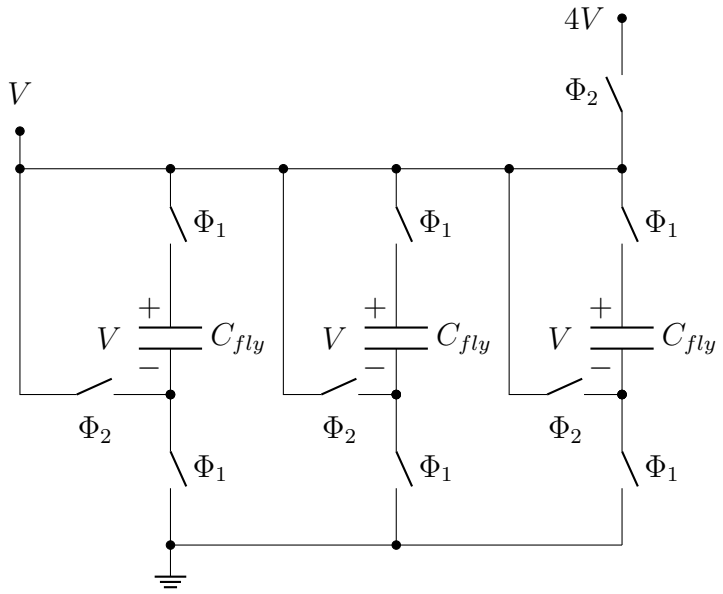


Figure 2.2.7: Series-Parallel Converter

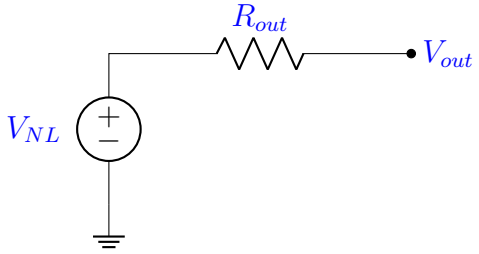


Figure 2.3.1: Output Impedance Model.

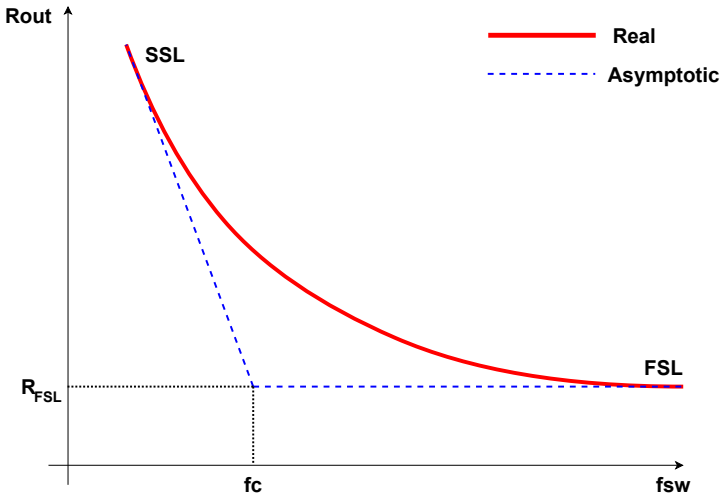


Figure 2.3.2: SCC Output Resistance vs Frequency

at FSL the RC constant is much grater than f_{sw} and the RC circuit doesn't reach equilibrium before the next switch, here the losses are dominated by the series losses in Switch Resistance.

Low Power applications operate in SSL, as switching losses are lower. In addition, on SSL, as the output resistance depends on the frequency, the output voltage can be controlled easily by controlling the frequency.

In [16] an approximate model for R_{out} was proposed, as shown in Eq.2.5. Being R_{FSL} a constant depending on the switches resistance and the converter topology, and $R_{SSL} = \frac{K}{f_{sw} C_{fly}}$(proof in Sec.2.4) where K is a constant depending on the capacitance C_{fly} and the converter topology.

$$R_{out} = \sqrt{R_{FSL}^2 + R_{SSL}^2} \tag{2.5}$$

Charge Flow Analysis is a classical approach to SCC analysis, based on the extraction of charge flow vectors $a_c^{(j)}$, which qualify the converters performance and facilitate comparison between different topologies. The method consists of identifying the different states (j) of the converter, and for each element(input,output,capacitance) identify the charge transfer $q_i^{(j)}$ of this element in this particular state. Then the flow vectors $a_c^{(j)}$ are obtained as follows:

$$\begin{cases} a^{(1)} = \left[q_{out}^{(1)}\ q_1^{(1)}\ \dots\ q_n^{(1)}\ q_{in}^{(1)}\right] / q_{out} = \left[a_{out}^{(1)}\ a_1^{(1)}\ \dots\ a_n^{(1)}\ a_{in}^{(1)}\right] \\ a^{(2)} = \left[q_{out}^{(2)}\ q_1^{(2)}\ \dots\ q_n^{(2)}\ q_{in}^{(2)}\right] / q_{out} = \left[a_{out}^{(1)}\ a_1^{(1)}\ \dots\ a_n^{(1)}\ a_{in}^{(1)}\right] \end{cases} \tag{2.6}$$

These charge vector elements are obtained by inspecting every state of conversion period assuming the following hypothesis:

- Kirchhoff's Law: The sum of charge flow elements equals zero in each node.
- In steady state, for each capacitor, the sum of both state's charge flow elements is zero.
- Output Capacitor C_{out} is larger than flying capacitors, so that it behaves as a voltage source, this implies no voltage ripple at the output node.

For example the vector a_c of the Fig.2.2.2 is represented in Eq.2.12

$$a^{(1)} = \left[q_{out}^{(1)}\ q_{C_{fly}}^{(1)}\ q_{in}^{(1)}\right] / q_{out} \tag{2.7}$$

$$\tag{2.8}$$

$$a^{(1)} = \left[\frac{1}{2}\ \frac{1}{2}\ \frac{1}{2}\right] \tag{2.9}$$

$$\tag{2.10}$$

$$a^{(2)} = \left[\frac{1}{2}\ -\frac{1}{2}\ 0\right] \tag{2.11}$$

$$\tag{2.12}$$

Note that the sum of the charge vector elements of the flying capacitor equals zero, while the sum of the output elements equals 1. Further more the conversion ratio is determined by the input to output charge fraction:

$$N = \frac{q_{in}}{q_{out}} \tag{2.13}$$

2.4 Slow Switching Limit aproximation to output resistance

Tellegen's theorem says that, for each state, the charge flow vectors are orthogonal with the voltages across the components, assuming we have n capacitors:

$$v_{out}\left(a_{out}^{(1)}+a_{out}^{(2)}\right)+\sum_{i=1}^{n}\left(a_{c,i}^{(1)}v_{c,i}^{(1)}+a_{c,i}^{(2)}v_{c,i}^{(2)}\right)=0 \tag{2.14}$$

Knowing that $a_{out}^{(1)}+a_{out}^{(2)}=1$ and $a_{c,i}^{(1)}=-a_{c,i}^{(2)}$, Eq.2.14 can be simplified in Eq.2.15.

$$v_{out}q_{out}+\sum_{i=1}^{n}(q_i\ \delta v_i)=0 \tag{2.15}$$

Assuming a linear model for the capacitance $\delta v_i = q_i/C_i$, then dividing Eq.2.15 by $q_{out}^2 f_{sw}$ we obtain the next equation:

$$\frac{v_{out}}{q_{out}f_{sw}}-\sum_{i=1}^{n}\left(\frac{q_i}{q_{out}}\right)^2\frac{1}{f_{sw}C_i}=0 \tag{2.16}$$

Finally remembering that $a_{c,i}=q_i/q_{out}$, we can write the equation for the Slow Switching Limit Resistance R_{SSL}:

$$R_{SSL}=\sum_{i=1}^{n}\frac{a_{c,i}^2}{f_{sw}C_i} \tag{2.17}$$

In the case of Fig.2.2.2 the output resistance is:

$$R_{SSL}=\frac{1}{2f_{sw}C_{fly}} \tag{2.18}$$

Slow Switching Limit hypothesis means that the switching period is large enough, so that in each cycle, the systems converges to it's final value. This implies that losses are independent of the switch's resistance, therefore the R_{SSL} is independent of switch resistance. For each topology, the R_{SSL} takes the form:

$$R_{SSL}=\frac{K}{f_{sw}C_{fly}} \tag{2.19}$$

Where the constant K only depends of the topology, and gives a figure of merit for how low can the losses be. Lower K will allow for lower f_{sw}, diminishing losses. Increasing C_i will also have this effect, but this is paid for in area.

The usual figure of merit used to qualify converter output impedance is:

$$M_{SSL}=\frac{V_{out}^2/R_{SSL}}{\sum_i \frac{C_i\delta v_{c,i}^2}{2}f_{sw}} \tag{2.20}$$

Topology	R_{SSL}	M_{SSL}
Ladder	$\frac{(n-1)^2}{C_{fly}f_{sw}}$	$\frac{2n^2}{(n-1)^4}$
Dickson	$\frac{n(n-1)/2}{C_{fly}f_{sw}}$	$\frac{8}{(n-1)^2}$
Fibonacci[1]	$\frac{F_{k+1}^2(F_{k+2}-1)}{C_{fly}f_{sw}}$	$\frac{2F_{k+2}^2}{\left(F_{k+1}^2(F_{k+2}-1)\right)^2}$
Doubler	$\frac{n(2log_2(n)-1)}{2C_{fly}f_{sw}}$	$\frac{8}{(2log_2(n)-1)^2}$
Series-Parallel	$\frac{n-1}{C_{fly}f_{sw}}$	$\frac{2n^2}{(n-1)^2}$

Table 2.1: Output Impedance vs Conversion Ratio

Taking input voltage of $1V$ we have $V_{out} = nV_{in} = n(1V)$, and the capacitance $C_i = a_{c,i}C_{fly}$ to minimize ripple, we obtain:

$$M_{SSL} = \frac{2n^2}{\left(\sum_i a_{c,i}^2\right) R_{SSL}C_{fly}f_{sw}} = \frac{2n^2}{K^2} \tag{2.21}$$

Table 2.1 shows Output Impedance and Conversion Ratio for classic topologies. In Fig.2.4.1 we see that at conversion ratio of 2 all converters are the same, and as conversion ratio increases all converters decrease in efficiency except for the series-parallel converter that sustains it's conversion efficiency for conversion level equal or above 3.

2.5 Control Strategies

In order to regulate the output voltage, as it depends on output resistance, frequency controlled can be used to regulate tge output. SSL have a no load voltage , which is valid when the converter is delivering no current to the load. When load is different from cero, the output voltage falls below the SSL no load voltage. To define a specific, desired output voltage as load varies, the converter must regulate the amount of charge delivered to the output in order to maintain the desired output voltage. Classical control schemes are presented in this chapter. As seen in Fig.2.3.1 we will model the converter as a no load voltage source and an output impedance.

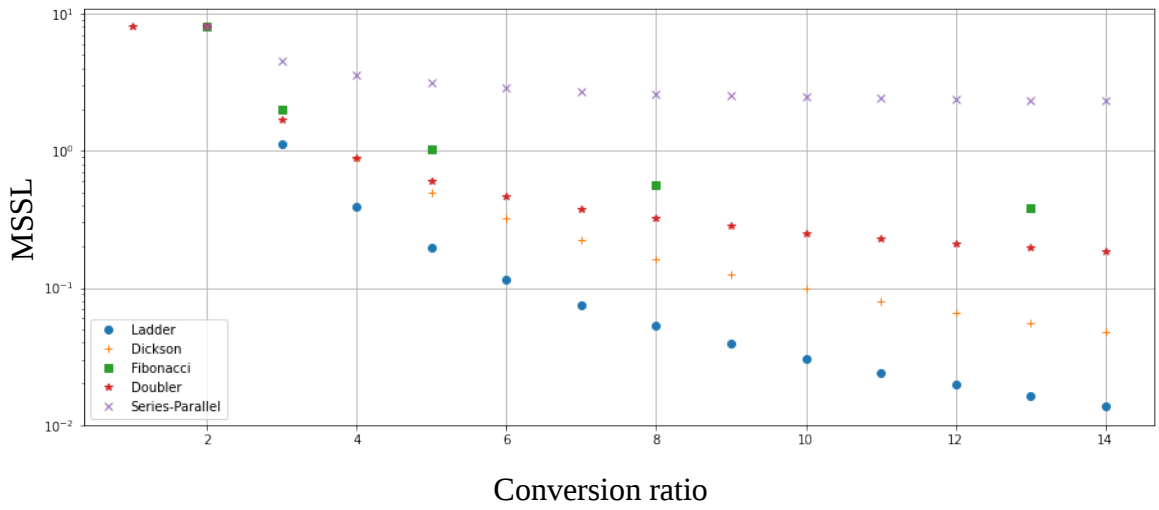


Figure 2.4.1: Output Impedance vs Conversion Ratio

2.5.1 Pulse-Frequency Modulation

Pulse-Frequency Modulation Modulation is perhaps the most intuitive approach in SSL, given the output resistance equation of Eq.2.19. It modulates the output current by controlling the amount of charge delivered to the load per unit of time. Fig.2.5.1 shows the block diagram, where $\Psi(f_{sw}, I_L)$ is the non-linear system representing the converter and it's load, and the H block represents the feedback voltage to frequency block.

The main advantage of this method against capacitance or pulse-width modulation is that as

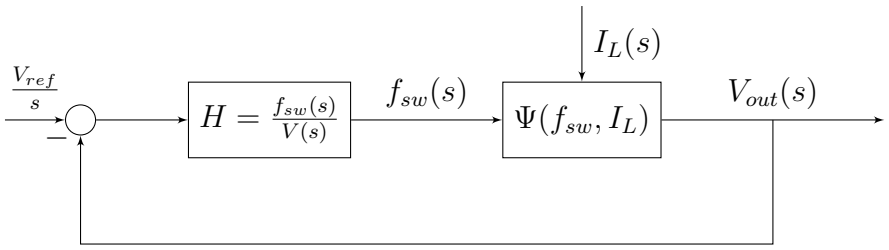


Figure 2.5.1: Linear Loop Block Diagram

frequency is scaled proportional to load, the efficiency can be sustained for low loads, therefor it is the preferred method in low or ultra-low power systems. As load keeps decreasing efficiency will eventually degrade, as leakage current losses become significant or, as will be seen in Chapter 5, short-circuit current losses in the oscillator degrade it's efficiency, this will also be addressed in Chapter 5.

The problems present in this strategy are that the main pole of the system is given by Ψ, and the pole is load dependent, so as the load changes eventually phase margin will decrease and instability will appear, further analysis of this is done in Chapter 7. Possible solutions to this are adding zeros to the feed-back loop, so as to cancel the pole of H, reducing the system to a first order system and eliminating phase margin problems.

2.5.2 Capacitance Modulation

In SSL the output impedance of a switched capacitor converter can also be modified by changing the amount of flying capacitance C_{fly}. The converter is equally sensitive to changes in it's flying capacitance value as it is in it's frequency. Capacitance Modulation approach is similar to multi-phasing techniques, the total capacitance is divide in N modules, see Fig.2.5.2, the switching frequency is constant, so that each NR_{out} has a constant value. As load increases more modules are activated, therefore increasing output current. Ripple is not increased, as output capacitance is added at the same time as output current. If each module is interleaved in time then ripple is actually reduced as load increases, but this is not an advantage over Pulse-Frequency Modulation control strategy, as in it, all available capacitance is always used and ripple is minimum for all loads. The trade off here is as follows, in Pulse-Frequency Modulation control more gates switch at lower frequency, in Capacitance Modulation control less gates switch at higher frequency.

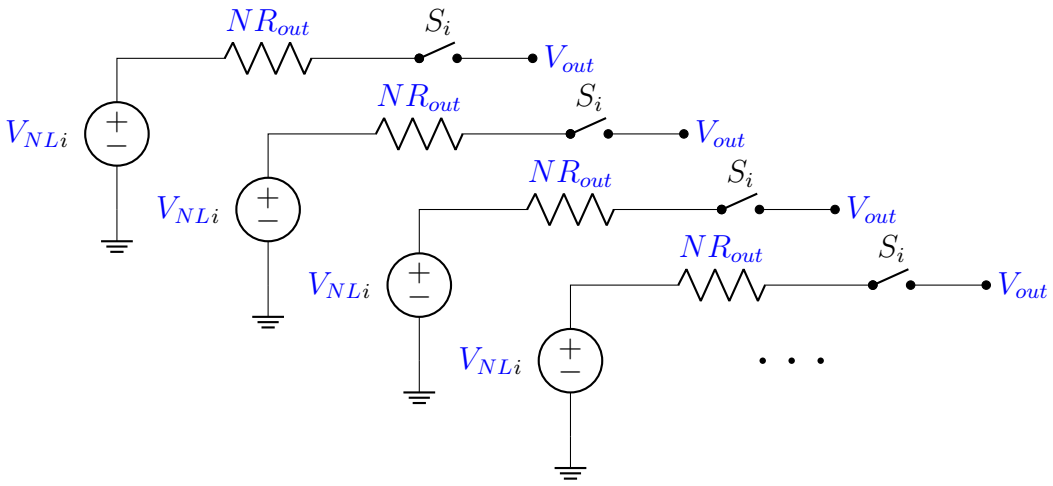


Figure 2.5.2: Capacitance Modulation Model

2.5.3 Pulse-Width Modulation in Fast Switching Limit Approximation(FSL)

In the case of FSL switching time is not long enough so that capacitance fully charge/discharge. In this case the circuit behaves as a classic RC charge/discharge circuit, as shown in Fig2.5.3.

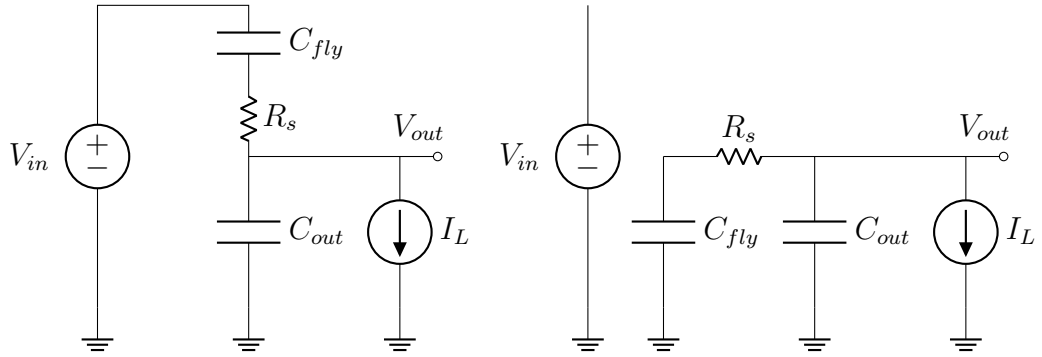
The equations that represent the behavior in each Phase are:

Phase I:

$$\begin{cases} C_{fly}\frac{dV_{C_{fly}}}{dt} - C_{out}\frac{dV_{C_{fly}}}{dt} = \frac{V_{C_{out}}}{R_L} \\ V_{C_{fly}} = V_{in} - V_{C_{out}} - R_s C_{fly}\frac{dV_{C_{fly}}}{dt} \end{cases} \quad \begin{cases} \frac{dV_{C_{fly}}}{dt} = \frac{V_{in}-V_{C_{out}}-V_{C_{fly}}}{R_s C_{fly}} \\ \frac{dV_{C_{out}}}{dt} = -\frac{V_{C_{fly}}}{R_s C_{out}} - \left(\frac{1}{R_s C_{out}} + \frac{1}{R_L C_{out}}\right) V_{C_{out}} + \frac{V_{in}}{R_s C_{out}} \end{cases} \tag{2.22}$$

Phase II:

$$\begin{cases} -C_{fly}\frac{dV_{C_{fly}}}{dt} - C_{out}\frac{dV_{C_{out}}}{dt} = \frac{V_{C_{out}}}{R_L} \\ V_{C_{fly}} = V_{C_{out}} - R_s C_{fly}\frac{dV_{C_{fly}}}{dt} \end{cases} \quad \begin{cases} \frac{dV_{C_{fly}}}{dt} = \frac{V_{C_{out}}-V_{C_{fly}}}{R_s C_{fly}} \\ \frac{dV_{C_{out}}}{dt} = \frac{V_{C_{fly}}}{R_s C_{out}} - \left(\frac{1}{R_s C_{out}} + \frac{1}{R_L C_{out}}\right) V_{C_{out}} \end{cases} \tag{2.23}$$



subfigure
Phase I

subfigure
Phase II

Figure 2.5.3: Series-Parallel in FSL

Taking a state variable $\dot{X} = AX + BU$ with $X = [V_{C_{fly}}\ V_{out}]$ and using a Time Averaged Analysis(TAA) [17] one can write a single set of equations by adding the equations of both Phases:

$$\begin{cases} \frac{dV_{C_{fly}}}{dt} & = \frac{-1}{R_s C_{fly}} V_{C_{fly}} + \frac{1-2D}{R_s C_{fly}} V_{C_{out}} + \frac{D}{R_s C_{fly}} V_{in} \\ \frac{dV_{C_{out}}}{dt} & = \frac{1-2D}{R_s C_{fly}} V_{C_{fly}} - \left(\frac{1}{R_s C_{out}} + \frac{1}{R_L C_{out}} \right) V_{C_{out}} + \frac{D}{R_s C_{out}} V_{in} \end{cases} \tag{2.24}$$

Defining $\omega_1 = \frac{1}{R_s C_{fly}}, \omega_2 = \frac{1}{R_s C_{out}}, \omega_3 = \frac{1}{R_L C_{out}}$

$$\begin{cases} \frac{dV_{C_{fly}}}{dt} & = \omega_1 V_{C_{fly}} + (1-2D)\omega_1 V_{C_{out}} + \omega_1 D V_{in} \\ \frac{dV_{C_{out}}}{dt} & = (1-2D)\omega_2 V_{C_{fly}} - (\omega_2 + \omega_3) V_{C_{out}} + D\omega_2 V_{in} \end{cases} \tag{2.25}$$

Where D represents the Duty Cycle. The system is non-linear in D, but can be linearized and controlled through a feed-back loop controlling the Duty Cycle. Note that now the equations depend of the switch's resistance R_s. In SSL as the switching period is long enough so as to be greater than the poles $\omega_1, \omega_2, \omega_3$, the amount of charge transfered is only a function of capacitance sizes, as the integral of the current is constant. Now R_s determines current, and total charge transfered is determined by Duty Cycle and current.

2.6 Soft-Charging

The work presented in [18] proposed the soft charging strategy, no capacitor being short-circuited, in [19] further formal analysis was presented. This has a great advantage as the intrinsic losses of a SCN are not present. The circuit is a variation of the Dickson converter, it is presented in Fig.2.6.1 and Fig.2.6.2. In order to eliminate current peak losses a capacitor can be charged using a voltage source, of course losses would still be present in the voltage of this source, but if the load itself is the source then no losses are present. This is the principle behind soft-charging, the load is used as a current source with which to charge the capacitor. The main

drawback of this technique is that the voltage variation ΔV that each capacitor experiments in each phase, is also experimented by the load. Basically ripple is incremented, this can be mitigated by using bigger C_{fly} value, or by increasing the number of phases.

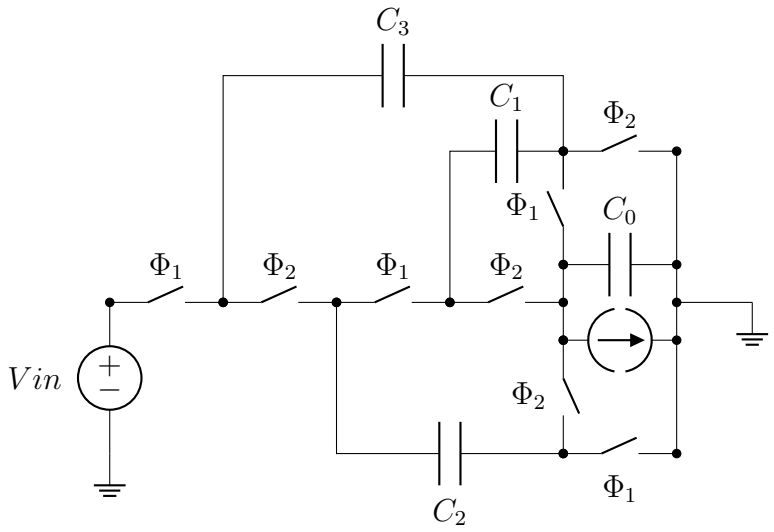


Figure 2.6.1: Dickson Converter

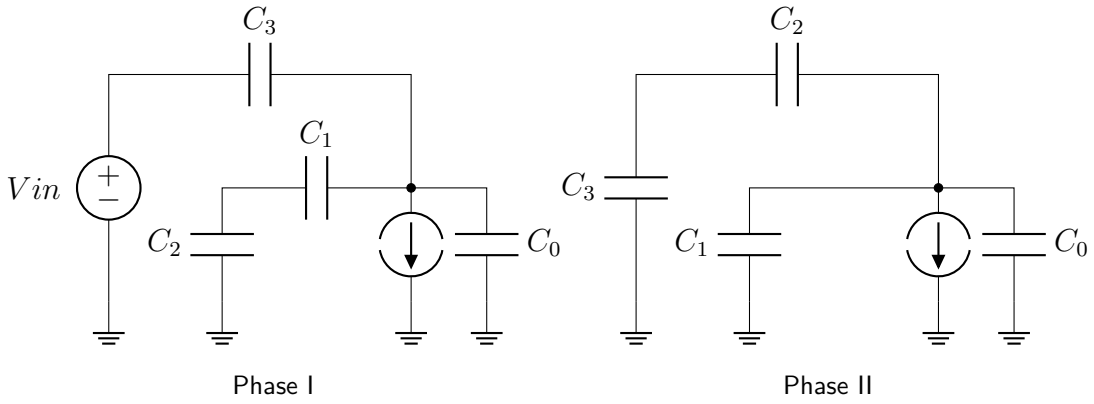


Figure 2.6.2: 4-to-1 Soft-Charging Dickson Converter

2.7 Modern Techniques

2.7.1 Stage Outphasing(SO)

In [20] the strategies of Stage Outphasing and Multiphase Soft-Charging were proposed. The idea is as follows, using a normal Dickson Converter as from Fig.2.7.1, each stage that connects capacitors C_k to C_{k+1} is phase-shifted 90 deg, so that not all stages commute at the same time. Then a second identical converter is added, with a phase shift of 180 deg, Fig.2.7.2 shows a diagram of the connection between stages k and $k+1$.

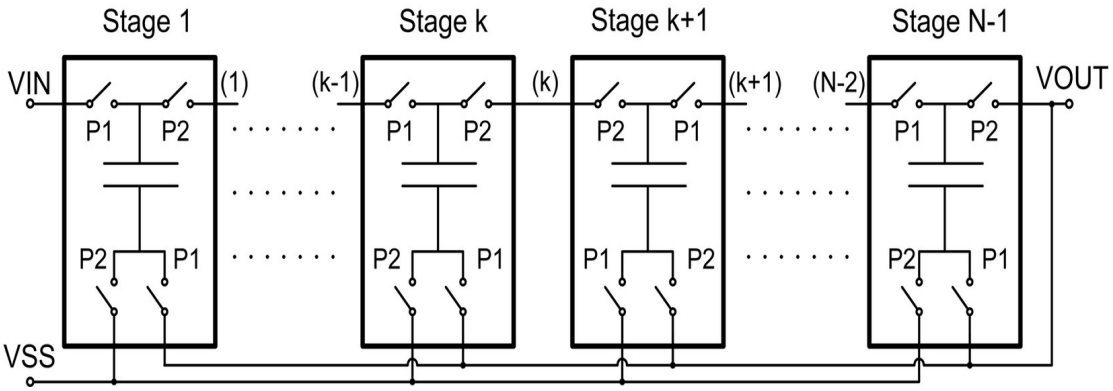


Figure 2.7.1: Normal N:1 Dickson Converter, taken from [20]

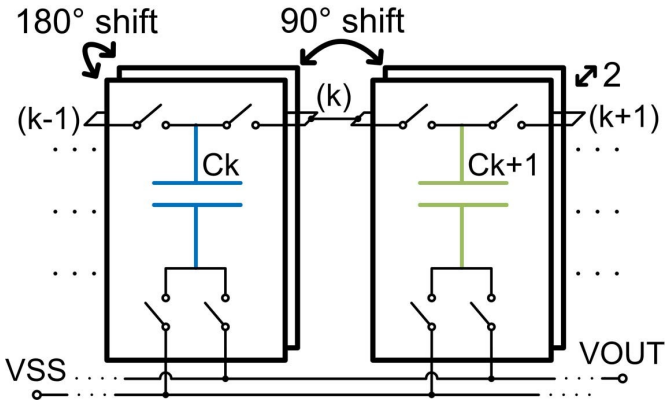


Figure 2.7.2: Stage Outphasing in stage k to $k+1$, taken from [20]

Where normally power loss in a charge transfer is:

$$P_{loss} = \frac{q^2}{C_k} \tag{2.26}$$

where q is the charge transferred between capacitor in one cycle. With Stage-Outphasing power losses are cut by half:

$$P_{loss} = 2C_k \left(\frac{\Delta V}{2}\right)^2 = \frac{q^2}{2C_k} \tag{2.27}$$

obtaining a factor of 2 improvement in comparison with the regular case. This means twice as much charge transfer without incrementing losses, equivalent to having twice as much flying capacitance. As the stages where divided in two and phase shifter, transistors are twice as much, but half in size, so driving losses do not increase.

2.7.2 Multiphase Soft-Charging(MSC)

The previous idea is expanded in [20] to a M number of phases, the authors name this Multiphase Soft-Charging, a diagram is presented in Fig.2.7.3. The concept is basically the same, but now having a phase-shift of 360 deg $/M$ between parallel stages, and a phase-shift of 180 deg $/M$ between adjacent stages. Each nose is split into M separate nodes: $(k, 1)$ to (k, M), and a switch is added from each cell to all adjacent nodes, one full cycle takes $2M$ phases, half charging, half discharging phases. In this case further switching power is added with extra phases.

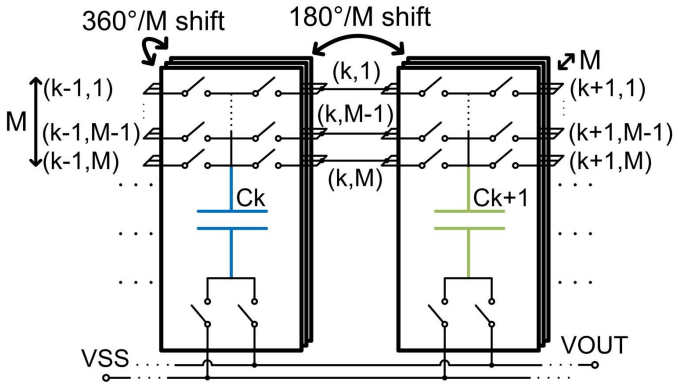


Figure 2.7.3: Multiphase Soft-Charging in stage k to $k+1$, taken from [20]

In Fig.2.7.4 a graph with capacitor voltages corresponding to each phase is presented. The effect can decreasing power losses proportionally to the number of phases used:

$$P_{loss} = \frac{q^2}{MC_K} \tag{2.28}$$

if Stage-Outphasing is used with MSC, Fig.2.7.5, both effects can be obtained simultaneously, obtaining further power loss reduction:

$$P_{loss} = \frac{q^2}{2MC_K} \tag{2.29}$$

The greater the number of phases the greater the improvement, theoretical values for the output impedance of converter are presented in Fig.2.7.6, where N is the conversion ratio and K_C is the constant of the output resistance $R_{SSL} = K_C/Cf_{sw}$. This efficiency gain trend will break when adding more phases causes increased losses associated with leakage.

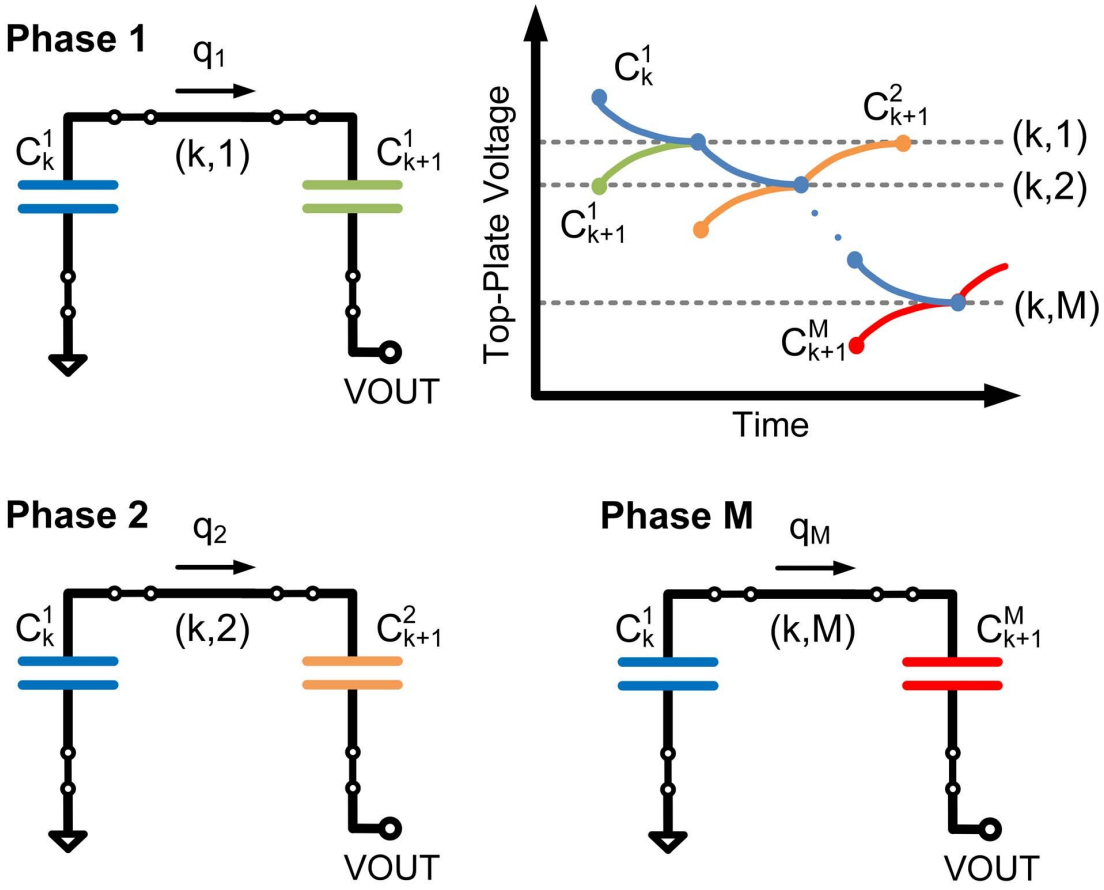


Figure 2.7.4: Charge Transfer bwtween adjacent cells with MSC, taken from [20]

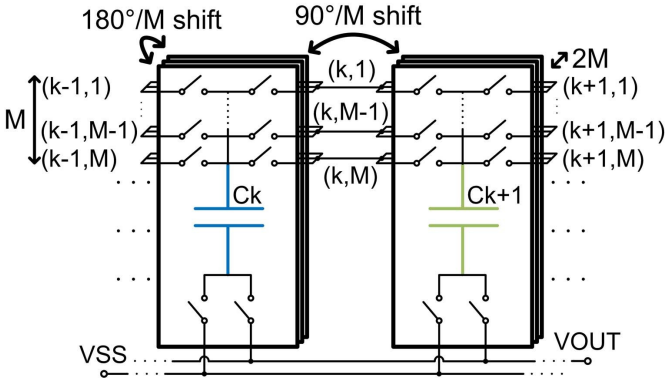


Figure 2.7.5: Charge Transfer bwtween adjacent cells with MSC and SO, taken from [20]

The authors of SO and MSC present a novel dc-dc converter in [21], fabricated with $28nm$ technology, with large voltage swing flying capacitor, which achieves a high efficiency of 90% across a wide output voltage range of $[0.9, 2.03]V$. Instead of minimizing the flying capacitor voltage swing in order to improve efficiency, using advanced multiphasing soft charging it is

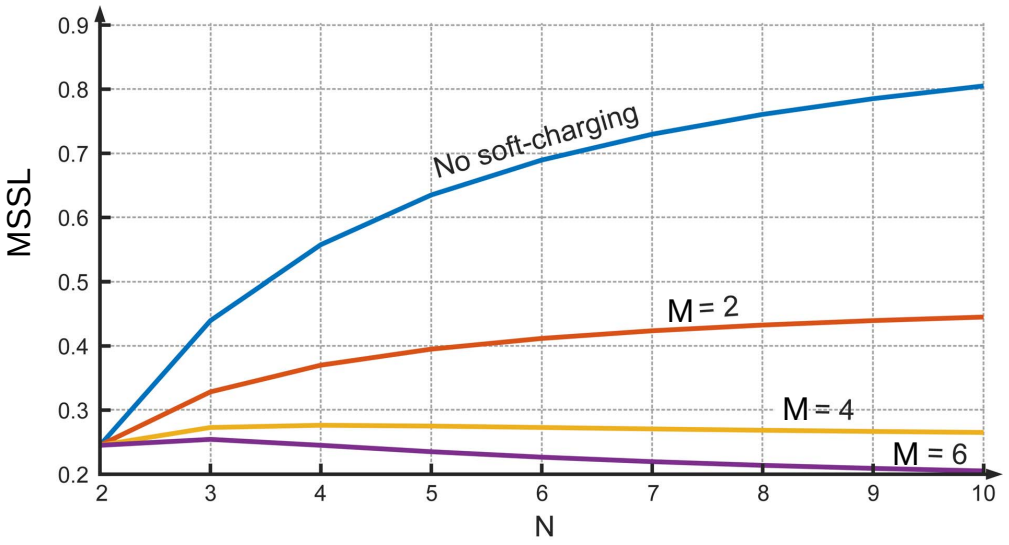


Figure 2.7.6: SSL figure of merit for N:1 Dickson Converter with MSC, taken from [20]

possible to maximize capacitor voltage swing, so as to obtain maximum output voltage range. Therefor capacitor swing is set between V_{in} and $0V$, the maximum possible swing.

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Chapter 3

SCC parameter Optimization through Convex Optimization

3.1 Introduction

In this chapter a modular converter is described and a method is analyzed to optimize its parameters in order to obtain the best relation between efficiency and area. This method is developed and applied in the technology `SOIxt018` . This analyze will be done on a Modular Converter that is presented next. And the results shows a formal method to determine the converter parameters and manage the trade-off between area and efficiency.

3.2 Modular Converter

What now if one doesn't know the output voltage exactly, or wishes to use the converter in several cases with different output voltages, a modular converter as shown in Fig.3.2.1 can be used. Here we have 2 V_{NL}, one corresponding to the 1/3 conversion $V_{NL1/3}$ and corresponding to the 2/3 conversion $V_{NL2/3}$. This allows more possibilities of V_{out}. It is possible to keep adding capacitors and having even more No Load voltages, but increasing the number of capacitors in series also increases the output impedance [22], which lowers the efficiency, as higher frequency is needed to compensate. For our analysis, we will use this 3 Capacitor Modular Interleaved Converter. As illustrated in Fig.3.2.1 each period the capacitors rotate allowing for them to be recharged. Each capacitor C_0, C_1, C_2 rotates between the positions $C_{top}, C_{mid}, C_{bott}$ and has a value C_{fly}. We will proceed to analyze the case of 1/3 conversion and deduce the Objective Function and Constraints to Optimize it.

Assuming a 1/3 voltage conversion we have that the bottom capacitor $C_{bott}(C_2)$ discharges as it delivers current to the load, while the middle $C_{mid}(C_1)$ and top $C_{top}(C_0)$ capacitors charges as current flows from the source through them to the load. In steady-state, the charge of one capacitor is the same after it completes a full rotation, and the source always delivers a set amount of charge Q. Then we conclude that each period C_{mid} and C_{top} receive Q while C_{bott} delivers $2Q$, and the load receives $3Q$. As the sum of the 3 capacitors voltages must be

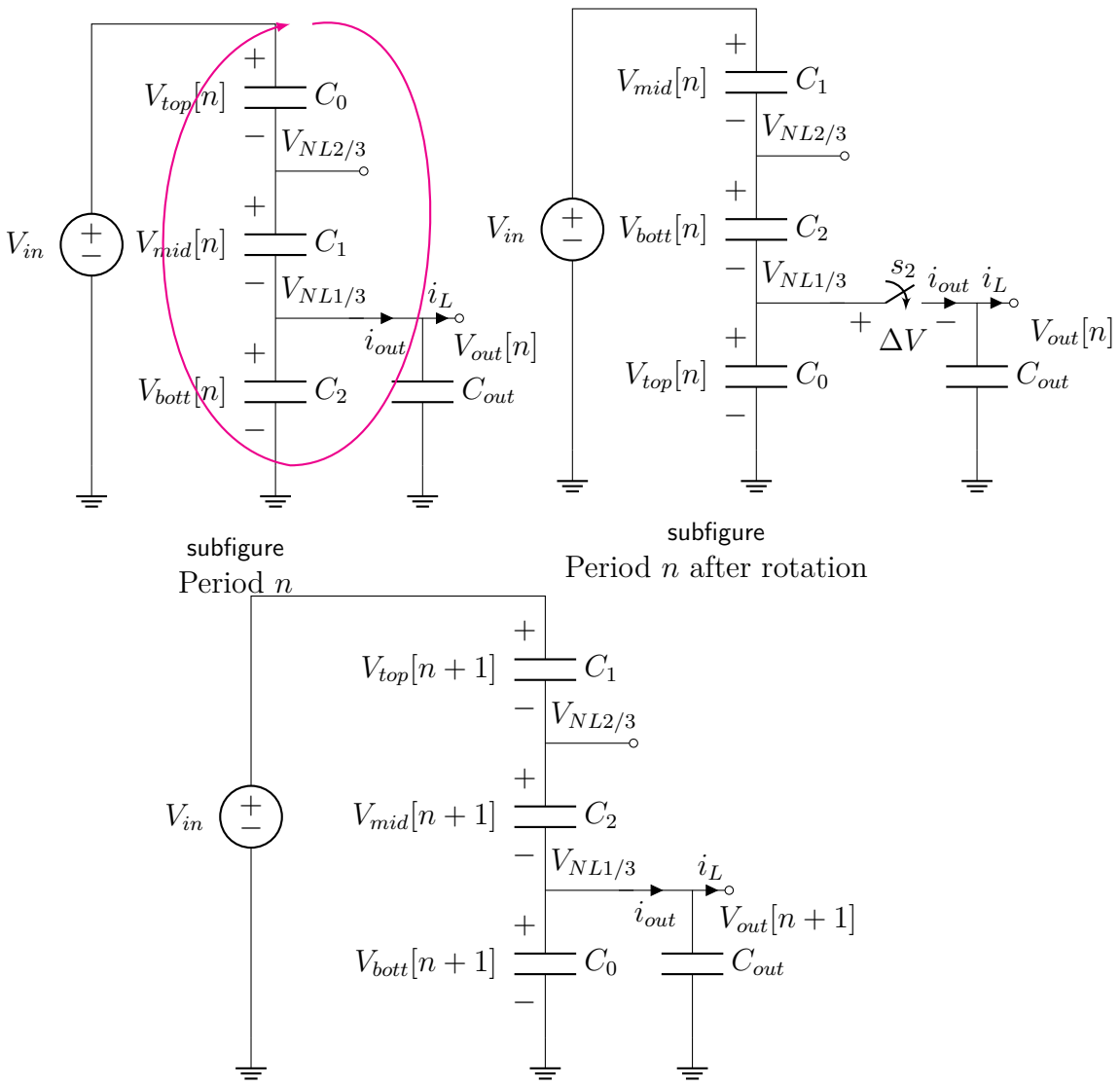

Figure 3.2.1: Modular 3 Capacitor Converter

$V_{in} = V_{top} + V_{mid} + V_{bott}$ it is proved in Appendix B that:

$$\begin{cases} V_{top} = V_{in}/3 + \Delta V/2 \\ V_{mid} = V_{in}/3 \\ V_{bott} = V_{in}/3 - \Delta V/2 \end{cases} \tag{3.1}$$

Where

$$Q = C_{fly}\Delta V/2 \tag{3.2}$$

If a capacitor receives a charge Q its voltage varies $\Delta V/2$.
Also we found that $V_{out} = V_{in}/3 - \Delta V/2$ and $I_{out} = 3Q/T_{sw} = 3Qf_{sw}$, then:

$$I_{out} = (3/2)C_{fly}\Delta V f_{sw} \tag{3.3}$$

To determine the power loss due to capacitor short circuit we need to know the value of C_{out}, instead of having a fixed C_{out}, the output capacitance is composed of other capacitor rings identical to this, which rotate one at a time with a phase shift, we will call N to the number of phases in the converter and it will be an optimization variable. In Fig.3.2.2 we see, for example, a 5 phases converter, where one ring rotates as the others hold the output voltage.
Eq.3.4 presents power losses caused by short-circuiting capacitance charged at different voltage

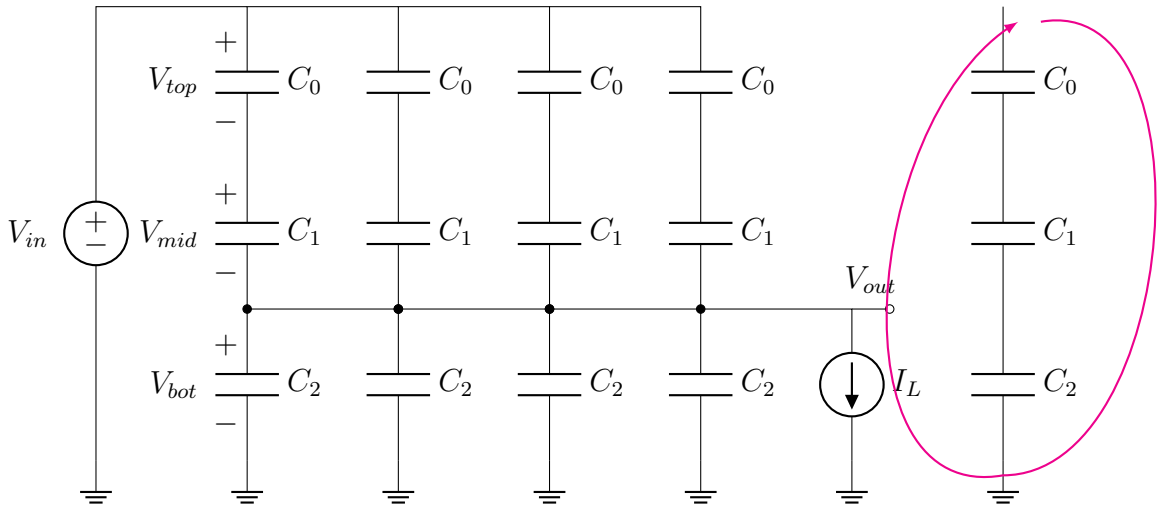

Figure 3.2.2: $N = 5$ Phase Converter

values and the seen output capacitance from one phase. In which C_{out} is the seen capacitance from the output node, which is constituted by the parallel seen capacitance of the $N-1$ phases that are not switching.

$$\begin{cases} P_{\Delta V} = \frac{C_A C_B}{C_A+C_B}\frac{\Delta V^2 f_{sw}}{2} = \frac{\frac{3}{2}C_{fly}C_{out}}{\frac{3}{2}C_{fly}+C_{out}}\frac{\Delta V^2 f_{sw}}{2} = \frac{3}{4}\frac{N-1}{N}C_{fly}\Delta V^2 f_{sw} \\ C_{out} = \frac{3}{2}C_{fly}(N-1) \end{cases} \tag{3.4}$$

Another important power loss is the switching power, all the switches that commute the capacitors introduce a series of gate capacitance that must be charged and discharged, this creates a power loss as given by Eq.1.2, and the sizes of these switches must be properly defined.

The fact that in each period the charge delivered to the load is constant ($3Q$), independent of f_{sw}, is given by the Hypothesis of working in SSL(Slow Switching Limit). In SSL the time constant of the RC circuit given by switch resistance and flying capacitor is much smaller than the period of operation i.e. $f_{sw} \ll 1/R_{sw}C_{fly}$. Working in this regime implies a maximum frequency of operation that corresponds to full load, this maximum frequency,and full load corresponds to our variables f_{sw} and I_L.This condition is expressed in Eq.3.5, where $R_{sw} = 1/g_{ds}$, the factor 3 corresponds to 3τ time of first order system convergence constant with $\tau = C_{fly}/g_{ds}$. The exact value of the RC constant depends on the converter architecture, where $C_{fly}^{eq}, g_{ds}^{eq}$ are a parallel-series combination of the capacitors C_{fly} and switches g_{ds} involved, for simplicity sake we approximate it to the value of one C_{fly}, g_{ds}. Finally as it takes N cycles to reach the same ring of capacitors, there is a relaxation of f_{sw} in the frequency.

$$\frac{1}{3}\frac{g_{ds}}{C_{fly}} \approx \frac{1}{3}\frac{g_{ds}^{eq}}{C_{fly}^{eq}} \geq \frac{2\pi f_{sw}}{N} \tag{3.5}$$

The conductance of a CMOS Switch, shown in Eq.3.6, is the sum of pMOS conductance g_{dsp} and nMOS conductance g_{dsn}, they are proportional to the width of the transistors W, setting $W = W_n = W_p/2$ we obtain the other optimization value $W(\mu m)$ and it's condition given by Eq.3.7, where g'_{ds} is the conductance per μm.

$$\begin{aligned} g_{ds} =& g_{dsn} + g_{dsp} = \mu_n n_p C_{ox} \frac{W_n}{L_{min}} \left[V_{in} - V_{tn0} - \delta_n V_{out} - n_n \Delta V/2\right] + \\ & \mu_p n_p C_{ox} \frac{W_p}{L_{min}} \left[V_{NL} - V_{tp0} - \delta_p (V_{in} - V_{NL}) - n_n \Delta V/2\right] \end{aligned} \tag{3.6}$$

$$\begin{cases} W \geq \frac{3\pi f_{sw} C_{fly}}{N g'_{ds}} \\ g'_{ds} = g_{ds}/W \end{cases} \tag{3.7}$$

Now we can determine the switching power P_{sw} as Eq.3.8, where L_{min} is the length of the transistors and C_{ox} the capacitance by a unit of area, k_{sw} is a constant to factor the many switches per converter as well as their buffers and losses given by logic blocks, k_{sw} was set to $k_{sw} = 13.5$.

$$P_{sw} = k_{sw} N f_{sw} V_{in}^2 W L_{min} C_{ox} \tag{3.8}$$

Finally, we'll add a couple more power losses:

- P_{TBPC} the power dissipated by charging and discharging the Top(TPC) and Bottom(BPC) Plate Capacitance of the flying capacitors. The top and bottom capacitance(TBPC) are defined as a fraction of the flying capacitance as: $C_{TPC} = C_{BPC} = k_{TBPC} C_{fly}$, with $k_{TBPC} = 10^{-4}$ the factor that determines the fraction, this small factor is chosen as the technology is SOI(Silicon over Insulator) and provides low capacitance to bulk silicon.

$$P_{TBPC} = f_{sw} N k_{TBPC} C_{fly} \left[2\left(\frac{V_{in}}{3} + \frac{\Delta V}{2}\right)^2 + \left(\frac{2V_{in}}{3} - \frac{\Delta V}{2}\right)^2\right] \tag{3.9}$$

- P_{osc} the power consumes by the CCO(Current Controlled Oscillator). This block generates a frequency proportional to its input current and is part of the feedback strategy in order to control the output voltage, see Chapter 6 and 7. As a simplification, this power will be assumed to be proportional to frequency, and the proportion constant k_{osc} is obtained from simulations done in the technology `SOIxt018` of node $0.18\mu m$, see Chapter 5.

$$\begin{cases} P_{osc} = k_{osc} \times f_{sw} \\ k_{osc} = 3.7 \times 10^{-13} (sW) \end{cases} \tag{3.10}$$

The ripple voltage is a function of ΔV. The ripple will be the voltage change after short-circuiting two capacitors A and B, with initial voltages V_o^A and V_o^B. When short-circuited this two capacitors will have the same final voltage $V_f = V_F^A = V_f^B$. The ripple is voltage is the difference between initial and final voltage of the output capacitance, if B were the output capacitance:

$$\Delta V = V_o^A - V_o^B \tag{3.11}$$

$$v_{ripple}^B = V_f^B - V_o^B = \frac{CA}{C_A + C_B} \Delta V \tag{3.12}$$

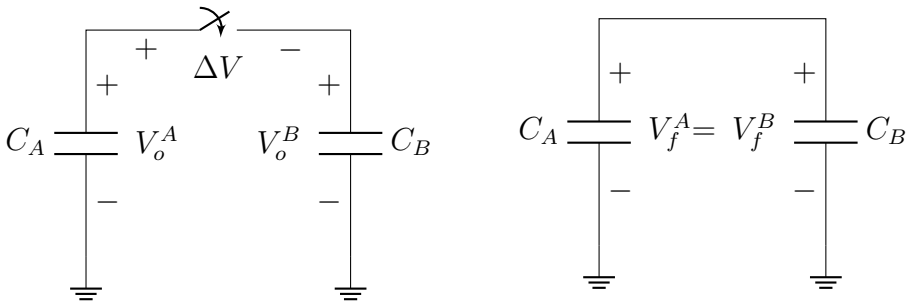

Figure 3.2.3: Ripple in Capacitance Short-Circuit

For our case when the ring capacitance is short-circuited with the output capacitance:

$$v_{ripple} = \frac{3/2C_{fly}}{3/2C_{fly} + C_{out}}\Delta V \tag{3.13}$$

$$v_{ripple} = \frac{3/2C_{fly}}{3/2C_{fly} + (N-1)3/2C_{fly}}\Delta V = \frac{\Delta V}{N-1} \approx \frac{\Delta V}{N} \tag{3.14}$$

In Fig.3.2.4 we have in the left figure, the voltage of one capacitor plate as it switches. From this graphic we can measure how much is the V_{top} Voltage (the voltage of the capacitor of higher voltages), which in the next period will be short circuited against output. We can obtain the ΔV from the difference between this voltage V_{top} and the output voltage, then $\Delta V = V_{top} - V_{out} = 690mV - 510mV = 180mV$, with $N = 12$, we have a ripple of $v_{ripple} = 180mV/12 \approx 15mV$, as seen in the right figure.

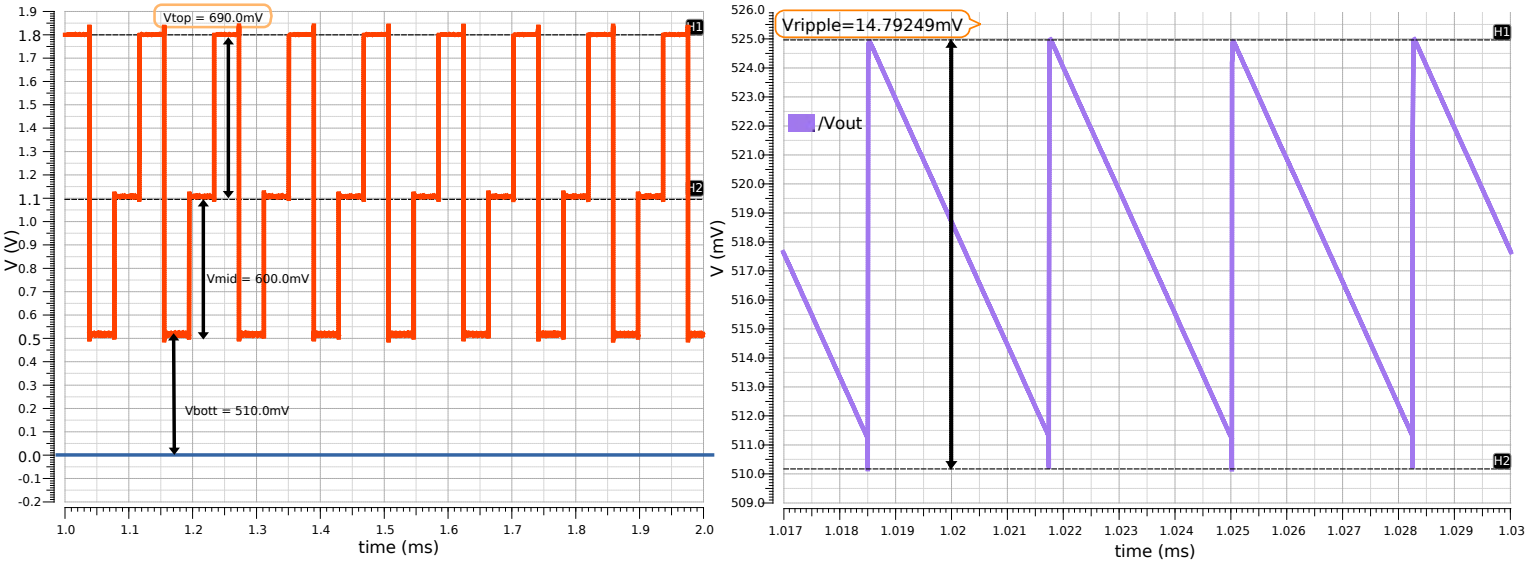

Figure 3.2.4: V_{top}(Left Figure) and v_{ripple}(Right Figure) for $N = 12$ converter.

The output current I_L is given by I_{out} from Eq.3.3 plus the charge taken from the rotating capacitors q_{ripple} when the ripple voltage discharges them, generally this can be ignored:

$$\begin{aligned} I_L &= I_{out} + q_{ripple} f_{sw} && (3.15)\\ &= (3/2) C_{fly} \Delta V f_{sw} + (3/2) C_{fly} v_{ripple} f_{sw} && (3.16)\\ &= (3/2) C_{fly} \Delta V f_{sw} + \frac{3/2}{N} C_{fly} \Delta V f_{sw} && (3.17)\\ &= (3/2) C_{fly} \Delta V f_{sw} \left(1 + \frac{1}{N}\right) \underset{N \gg 1}{\approx} (3/2) C_{fly} \Delta V f_{sw} && (3.18)\\ &\Rightarrow I_L \approx I_{out} && (3.19) \end{aligned}$$

From Eq.3.3 we note that we can deliver more power by increasing C_{fly}, ΔV or f_{sw}. ΔV is determined by the output desires voltage, increasing C_{fly} implies more losses as given by Eq.2.1 and increasing f_{sw} will imply more switching losses as will be seen later.

Now we are in condition to formulate our area vs power optimization problem.

3.3 Geometric Problem Formulation

We define the total power loss, expressed in Eq.3.20 as the sum of losses defined by Eq.3.4, 3.8, 3.9, 3.10. We would like to minimize it while at the same time minimize the area of the converter. The total area a_T has two main components, the area of the capacitance A_C and the area of the switches A_{sw}, defined in the Eq.3.21, where K is the same constant used in Eq.3.8.

$$p_T = P_{\Delta V} + P_{sw} + P_{tbpc} + P_{osc} \tag{3.20}$$

$$\begin{cases} a_T = A_C + A_{sw} \\ A_C = 3N \frac{C_{fly}}{C_{mosvc}} \\ A_{sw} = KNWL_{min} \end{cases} \tag{3.21}$$

Based on the work from [23], to minimize 2 functions at the same time it is necessary to construct a Pareto front, we will define the vector $\gamma \in [0, 1]$, where each element of γ corresponds to a point of the front in our Pareto-optimal design. As we go through the elements of γ the weight assigned to p_T and a_T in the objective function changes, having both equal weights when $\gamma = 1/2$. But to do this we must normalize p_T and a_T, so we will define P as the maximum power loss, obtained by minimizing only a_T and calculating the power loss in this case, and A as the maximum area, obtained by minimizing only p_T and calculating the total area for this case. The maximum power loss is defined in Eq.3.22, the maximum area is defined in Eq.3.23, and the geometric problem is shown in Eq.3.24.

$$P = Argmin\left\{\min_X \quad a_T\right\} \tag{3.22}$$

$$A = Argmin\left\{\min_X \quad p_T\right\} \tag{3.23}$$

$$GP = \min_{X=[W,N,f_{sw},C_{fly}]} \quad \gamma \frac{p_T}{P} + (1-\gamma)\frac{a_T}{A} \tag{3.24}$$

$$\text{s.t.} \quad 3\frac{2\pi f_{sw} C_{fly}}{g'_{ds} N} \leq W \quad (from\ Eq.3.7) \tag{3.25}$$
$$0.22 \leq W \leq 1000 \tag{3.26}$$
$$1 \leq N \leq 1000 \tag{3.27}$$
$$I_L \leq \frac{3}{2} C_{fly} \Delta V f_{sw} \quad (from\ Eq.3.18) \tag{3.28}$$
$$\frac{\Delta V}{N} \leq v_{ripple} \quad (from\ Eq.3.33) \tag{3.29}$$
$$1 \leq f_{sw} \leq 1GHz \tag{3.30}$$
$$10fF \leq C_{fly} \leq 10\mu F \tag{3.31}$$

In Eq.3.24 we have used all the restrictions deduced so far plus some reasonable limitations for our optimization variable

$$X = [W, N, f_{sw}, C_{fly}] \tag{3.32}$$

Setting W between W_{min} and $1mm$; number of Phases N between one and a thousand; f_{sw} between $1Hz$ and $1GHz$, which is a reasonable upper limit for this technology; and C_{fly} between $10fF$ and $10\mu F$ to have a reasonable charge transfer.

One final restriction for the ripple voltage by defining it as:

$$v_{ripple} = \frac{3Q}{C_{out}} = \frac{3/2 C_{fly} \Delta V}{3/2 C_{fly}(N-1)} \approx \frac{3/2 C_{fly} \Delta V}{3/2 C_{fly} N} = \frac{\Delta V}{N} \tag{3.33}$$

using value of Q from Eq.3.2 and approximating $C_{out} \approx 3/2 N C_{fly}$ from Eq.3.4. The need for this approximation comes from that in a geometric problem the objective function and restrictions must be posynomials, posynomials are sums monomials. A posynominal is of with the form shown in Eq.3.35.

$$monomial \Rightarrow m(x_1, x_2, \ldots, x_n) = c x_1^{a_1} \ldots x_n^{a_n} \tag{3.34}$$
$$posynomial \Rightarrow p(x_1, x_2, \ldots, x_n) = \sum_{k=1}^{K} c_k x_1^{a_{1k}} \ldots x_n^{a_{nk}} \tag{3.35}$$

Posynomials are not convex functions, so to have a convex problem it is necessary to do a change of variable: $y = log(x)$ and take the logarithm of the objective and constrain functions. In the case of monomials the change of variable yields an exponential of an affine function.

$$m(x_1, x_2, \ldots, x_n) = c x_1^{a_1} \ldots x_n^{a_n} \tag{3.36}$$
$$\begin{cases} m(e^{y_1}, e^{y_2}, \ldots, e^{y_n}) = e^{b + a_1 y_1 + \cdots + a_n y_n} = e^{A^T Y + b} \\ b = log(c) \end{cases} \tag{3.37}$$

In the case of posynomials the variable change yields a log-sum-exp form of affines functions. See Appendix.A for proof that this form is convex.

$$\begin{cases} p(e^{y_1}, e^{y_2}, \ldots, e^{y_n}) = \sum_{k=1}^{K} e^{b_k + a_{1k} y_1 + \cdots + a_{nk} y_n} = \sum_{k=1}^{K} e^{A_k^T Y + b_k} \\ b = log(c) \end{cases} \tag{3.38}$$

Making the change of variable $Y = [y_1, y_2, y_3, y_4] = log(X) = log([W, N, f_{sw}, C_{fly}])$ we obtain the problem shown in Eq.3.39. See Appendix.A for proof that this form is convex. Optimization of log-sum-exp forms is called a Geometric Problem (GP):

$$GP = \min_{e^{y_1},e^{y_2},e^{y_3},e^{y_4}} \quad log\left(\gamma\frac{p_T}{P} + (1-\gamma)\frac{a_T}{A}\right) \tag{3.39}$$

$$\text{s.t.} \quad log\left(3\frac{2\pi e^{y_3}e^{y_4}}{g'_{ds}e^{y_2}e^{y_1}}\right) \leq 0 \quad (from\ Eq.3.25) \quad [1] \tag{3.40}$$

$$-log\left(\frac{e^{y_1}}{0.22}\right) \leq 0 \quad (from\ Eq.3.26) \quad [2] \tag{3.41}$$

$$log\left(\frac{e^{y_1}}{10^3}\right) \leq 0 \quad (from\ Eq.3.26) \quad [3] \tag{3.42}$$

$$log\left(\frac{e^{y_2}}{10^3}\right) \leq 0 \quad (from\ Eq.3.27) \quad [4] \tag{3.43}$$

$$-log(e^{y_2}) \leq 0 \quad (from\ Eq.3.27) \quad [5] \tag{3.44}$$

$$-log\left(\frac{3}{2}e^{y_4}\Delta V e^{y_3}/I_L\right) \leq 0 \quad (from\ Eq.3.28) \quad [6] \tag{3.45}$$

$$log\left(\frac{3\Delta V}{4e^{y_2}v_{ripple}}\right) \leq 0 \quad (from\ Eq.3.29) \quad [7] \tag{3.46}$$

$$log\left(\frac{e^{y_3}}{10^9}\right) \leq 0 \quad (from\ Eq.3.30) \quad [8] \tag{3.47}$$

$$-log(e^{y_3}) \leq 0) \quad (from\ Eq.3.30) \quad [9] \tag{3.48}$$

$$log\left(\frac{e^{y_4}}{10^{-5}}\right) \leq 0 \quad (from\ Eq.3.31) \quad [10] \tag{3.49}$$

$$-log\left(\frac{e^{y_4}}{10^{-14}}\right) \leq 0 \quad (from\ Eq.3.31) \quad [11] \tag{3.50}$$

$$GP = \min_{y_1,y_2,y_3,y_4} log\left(\gamma\frac{p}{P} + (1-\gamma)\frac{a}{A}\right) \tag{3.51}$$

$$\text{s.t.} \quad log\left(3\frac{2\pi e^{y_3}e^{y_4}}{g'_{ds}e^{y_2}e^{y_1}}\right) \leq 0 \iff log\left(\frac{6\pi}{g'_{ds}}\right) + y_3y_4 - y_2 - y_1 \leq 0 \quad [1] \tag{3.52}$$

$$\iff r_1 + y_3y_4 - y_2 - y_1 \leq 0 \tag{3.53}$$

$$-log\left(\frac{e^{y_1}}{0.22}\right) \leq 0 \iff log(0.22) - y_1 \leq 0 \quad [2] \tag{3.54}$$

$$log\left(\frac{e^{y_1}}{10^3}\right) \leq 0 \iff y_1 - log(10^3) \leq 0 \iff y_1 - r_3 \leq 0 \quad [3] \tag{3.55}$$

$$log\left(\frac{e^{y_2}}{10^3}\right) \leq 0 \iff y_2 - log(10^3) \leq 0 \iff y_2 - r_4 \leq 0 \quad [4] \tag{3.56}$$

$$-log(e^{y_2}) \leq 0 \iff -y_2 \leq 0 \quad [5] \tag{3.57}$$

$$-log\left(\frac{3}{2}e^{y_4}\Delta V e^{y_3}/I_L\right) \leq 0 \iff log\left(\frac{2I_L}{3\Delta V}\right) - y_4 - y_3 \leq 0 \quad [6] \tag{3.58}$$

$$\iff r_6 - y_4 - y_3 \leq 0 \tag{3.59}$$

$$log\left(\frac{3\Delta V}{4e^{y_2}v_{ripple}}\right) \leq 0 \iff log\left(\frac{3\Delta V}{4v_{ripple}}\right) - y_2 \leq 0 \iff r_7 - y_2 \leq 0 \quad [7] \tag{3.60}$$

$$log\left(\frac{e^{y_3}}{10^9}\right) \leq 0 \iff y_3 - 9log(10) \leq 0 \iff y_3 - r_8 \leq 0 \quad [8] \tag{3.61}$$

$$-log(e^{y_3}) \leq 0 \iff -y_3 \leq 0 \quad [9] \tag{3.62}$$

$$log\left(\frac{e^{y_4}}{10^{-5}}\right) \leq 0 \iff y_4 + 5log(10) \leq 0 \iff y_4 + r_{10} \leq 0 \quad [10] \tag{3.63}$$

$$-log\left(\frac{e^{y_4}}{10^{-14}}\right) \leq 0 \iff -y_4 - 14log(10) \leq 0 \quad [11] \tag{3.64}$$

$$
\begin{aligned}
GP = \quad \min_{y_1,y_2,y_3,y_4} \quad & log\left(\gamma\frac{p}{P} + (1-\gamma)\frac{a}{A}\right) && (3.65)\\
\text{s.t.} \quad & r_1 + y_3 y_4 - y_2 - y_1 \leq 0 && (3.66)\\
& y_1 - r_3 \leq 0 && (3.67)\\
& y_2 - r_4 \leq 0 && (3.68)\\
& r_6 - y_4 - y_3 \leq 0 && (3.69)\\
& r_7 - y_2 \leq 0 && (3.70)\\
& y_3 - r_8 \leq 0 && (3.71)\\
& y_4 + r_{10} \leq 0 && (3.72)\\
& y_2, y_3 \geq 0 && (3.73)
\end{aligned}
$$

3.4 Simulation and Results

The problem of Eq.3.39 was solved using the package `cvxopt` of `Python3.7.3`.

Pareto Front At Fig.3.4.1, the Pareto Front of problem is plotted next to the efficiency. The idea of the Pareto Front graph is to determine the γ value at the knee of the curve, which gives the minimum value of one part of the cost function, in this case a_T, that is near enough of the minimum of the other part of the cost function: p_T. In this case, to maintain good enough efficiency we should set the γ value between $[0.1, 0.5]$ (in the shown circle), and we have an espected Area Range of $a_T = [1, 4](mm^2)$

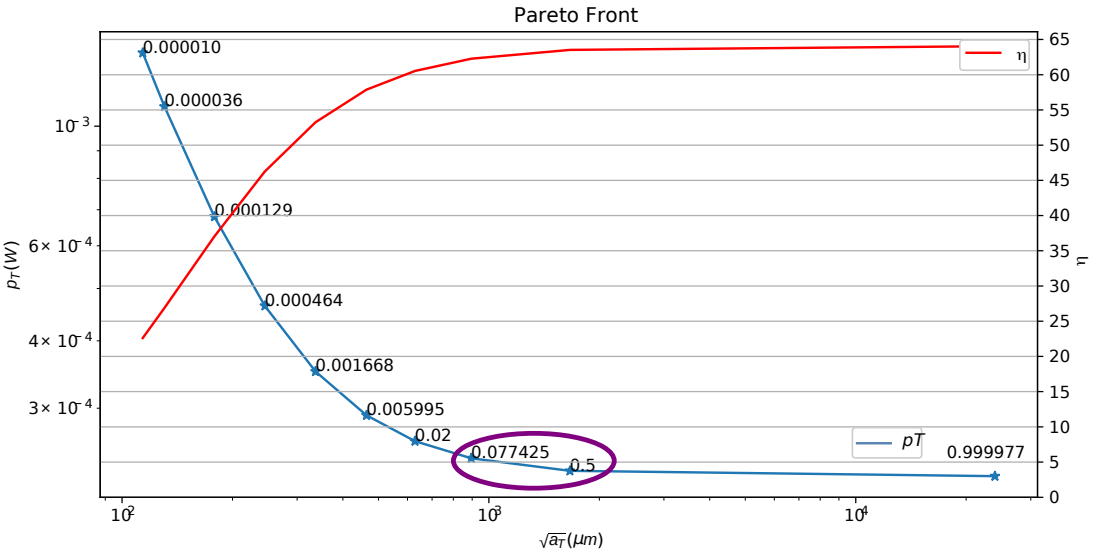

Figure 3.4.1: Pareto Front vs Efficiency

Results are shown in Fig.3.4.2, 3.4.3 for the parameters of Eq.3.74, which are constrains obtained from the technology nominal voltage $V_{DD} = 1.7V$, a maximum load of $I_L = 1mA$, and a maximum ripple of $v_{ripple} = 50mV$. The no load elected voltage is the closest to desired output voltage, but also a greater than output voltage.
Variable f_{sw} is calculated as a real number and then rounded to the nearest integer for convenience. Meanwhile W is rounded to the nearest multiple of $W_{min} = 0.22$, which is the minimum width of transistors, for layout construction purposes. For this reason N and W are many times constant $\forall\ \gamma$, the resultant constant N and W are shown in Eq.3.75.

$$\begin{cases} I_L = 1mA \\ v_{ripple} = 50mV \\ V_{DD} = 1.8V \Rightarrow V_{NL} = [1.8, 1.2, 0.6] \\ V_{out} = 0.4V \Rightarrow V_{NL} = 0.6 \Rightarrow \begin{cases} \Delta V = 0.4V \\ V_{NL} = 0.6V \end{cases} \end{cases} \tag{3.74}$$

$$\begin{cases} N = 6 \\ W = 10.56\mu m \end{cases} \tag{3.75}$$

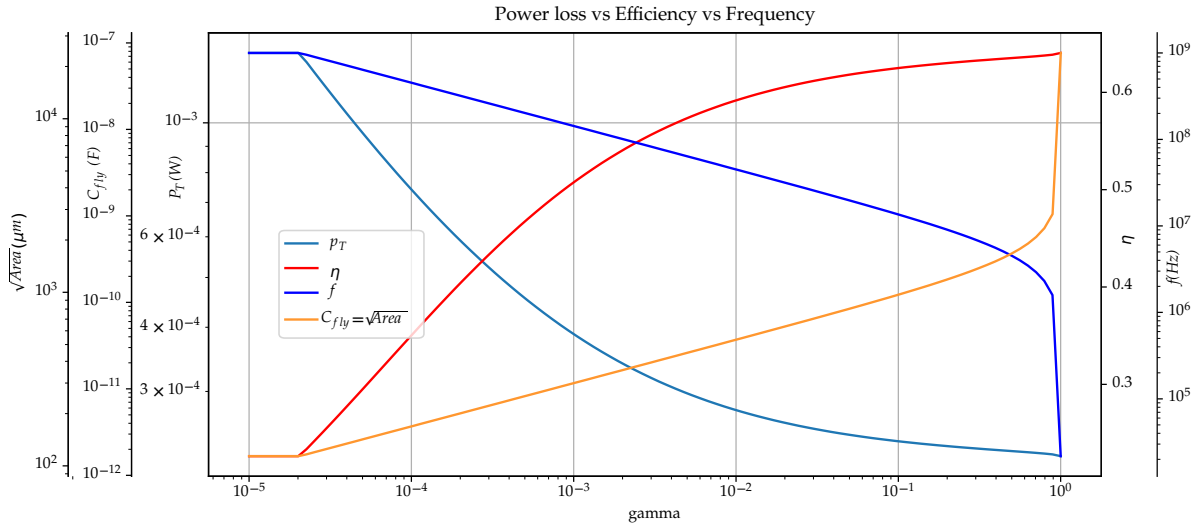

Figure 3.4.2: Power Loss vs Efficiency vs Frequency

As expected as gamma increases the weight of p_T in the Objective Function the Efficiency increases and p_T and f_{sw} decreases. There is an upper limit for the Efficiency, and intrinsic Efficiency, Eq.3.77, which is given by the losses of ΔV Eq.3.4, this limit depends only on the value of ΔV the greater the ΔV the lower the Efficiency. This effect also influences the form of Fig.3.4.3 which increases with gamma as this intrinsic power loss can not be eliminated.
The curve of Area is the same as the curve of C_{fly} as the capacitors dominate the total area, and as seen in Fig.3.4.2 the points of higher Efficiency correspond to the points of higher area.

$$\eta_{intr} = \frac{P_{out}}{P_{out} + P_{\Delta V}} = \frac{3/2 V_{out} f_{sw} C_{fly} \Delta V/2}{3/2 V_{out} f_{sw} C_{fly} \Delta V/2 + \frac{3}{2}\frac{N-1}{N} C_{fly} \Delta V^2/2 f_{sw}} \tag{3.76}$$

$$= \frac{V_{out}}{V_{out} + \frac{N-1}{N}\Delta V} \approx 0.71 \tag{3.77}$$

In order to have an efficiency of over 90%, we need $\Delta V \leq V_{out}/10$, this means that $\Delta V/2 = V_{NL} - V_{out} \leq V_{out}/20$ so the output voltage must be really close to the no load voltage: $V_{out} \approx 0.95 V_{NL}$, with $V_{NL} = 0.6V$ then $V_{out} \geq 0.57V$.

Let us move from over specification restrictions of Eq.3.74, by allowing V_{out} (Fig.3.4.5) or v_{ripple} (Fig.3.4.4) to vary.

The ripple voltage only influences the number of phases N as shown in Eq.3.14, and the width of transistors W as the lower v_{ripple} means higher $C_{fly} f_{sw}$ if N is constant, which requires bigger switches. Therefore v_{ripple} is proportional to W and nversely proportional to N, see Fig.3.4.4.

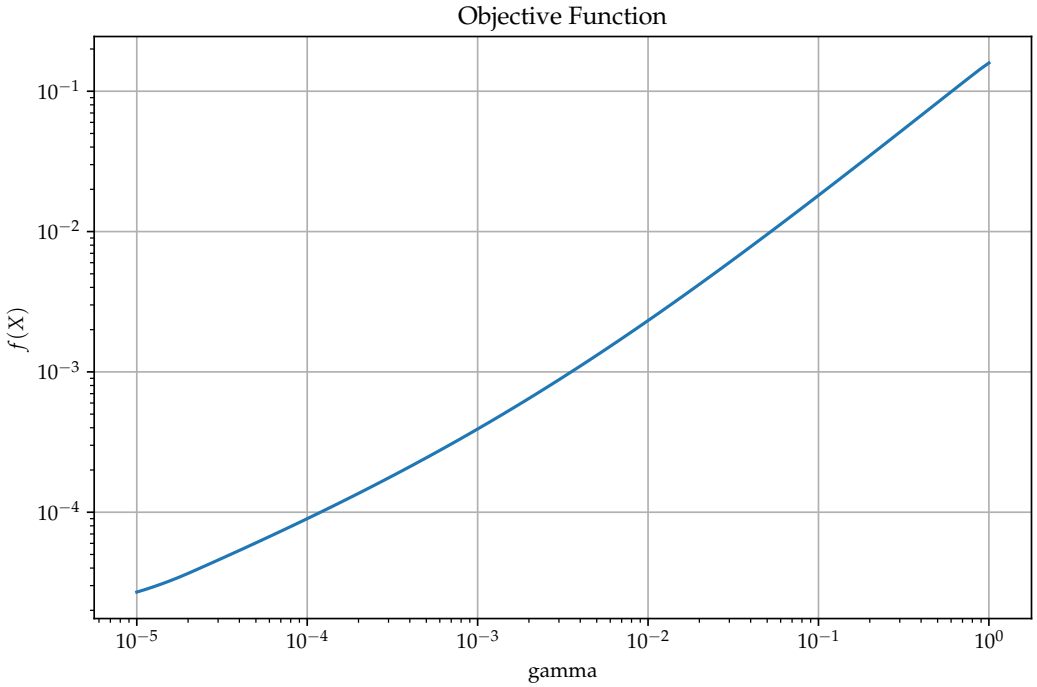

Figure 3.4.3: Objective Function

$$2\pi f_{sw} = \frac{1}{R_{sw}C_{fly}} \propto \frac{1}{WC_{fly}} \Rightarrow W \propto \frac{1}{2\pi f_{sw}C_{fly}} \tag{3.78}$$

$$\begin{cases} cte = I_L = C_{fly}f_{sw}\Delta V \\ v_{ripple} = \Delta V/N \end{cases} \Rightarrow I_L = C_{fly}f_{sw}v_{ripple}N \Rightarrow C_{fly}f_{sw} \propto \frac{1}{v_{ripple}N} \tag{3.79}$$

$$\Rightarrow W \propto \frac{1}{2\pi f_{sw}C_{fly}} \propto v_{ripple}N \tag{3.80}$$

$$W \propto v_{ripple}N \tag{3.81}$$

Finally, in Fig.3.4.5 we can see the classical SCC Efficiency vs V_{out} curve, as the Power loss is dominated by the $P_{\Delta V}$ the Efficiency Peaks right before the no-load voltage and fall drastically after them, while the Power loss has opposite behavior. As the amount of charge delivered to the load is also proportional to ΔV the frequency increases as we approach V_{NL}, to compensate the low charge in this ΔV, and falls drastically after it.

In Fig.3.4.6 we see the changes in N, W and C_{fly} as V_{out} is swept. Here N does vary, when far from V_{NL} the ΔV is high so Q will be high and that means more ripple, therefore N is large in this case. As we approach V_{NL} N decreases, but to keep delivering the same output power C_{fly} must increase. As C_{fly} increases, and we saw in Fig.3.4.5, approaching V_{NL}, f_{sw} also increases, therefore the Switches must grow in order to keep their RC constant larger than the switching frequency f_{sw}.

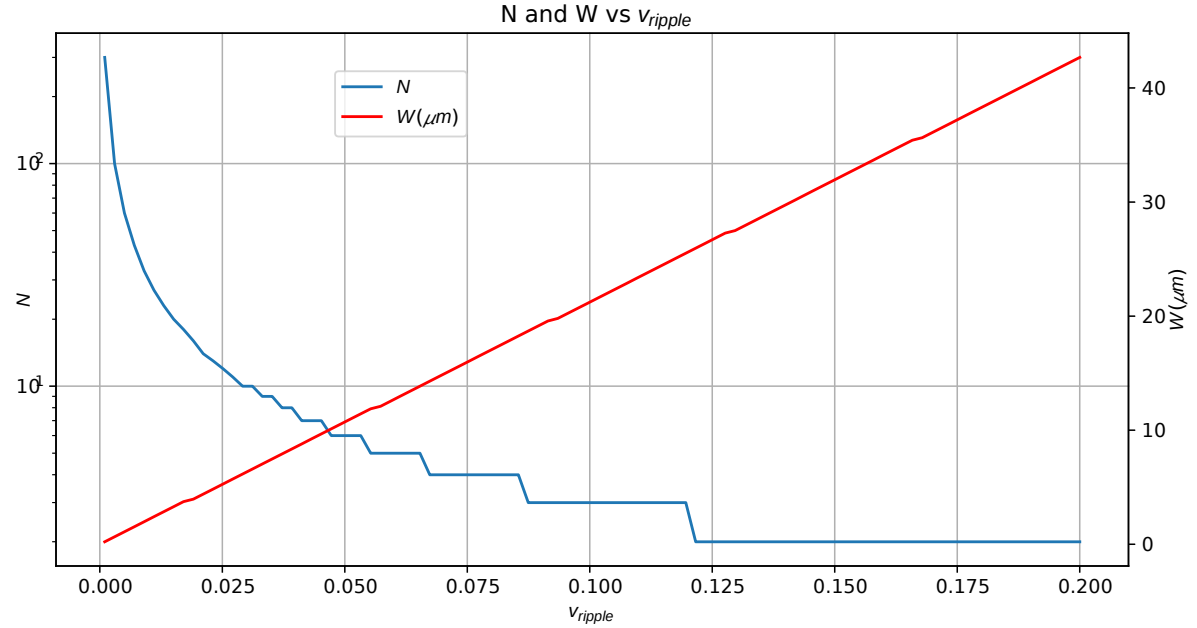

Figure 3.4.4: Ripple Voltage v_{ripple} vs constant Number of Phases N or constant Switch width W

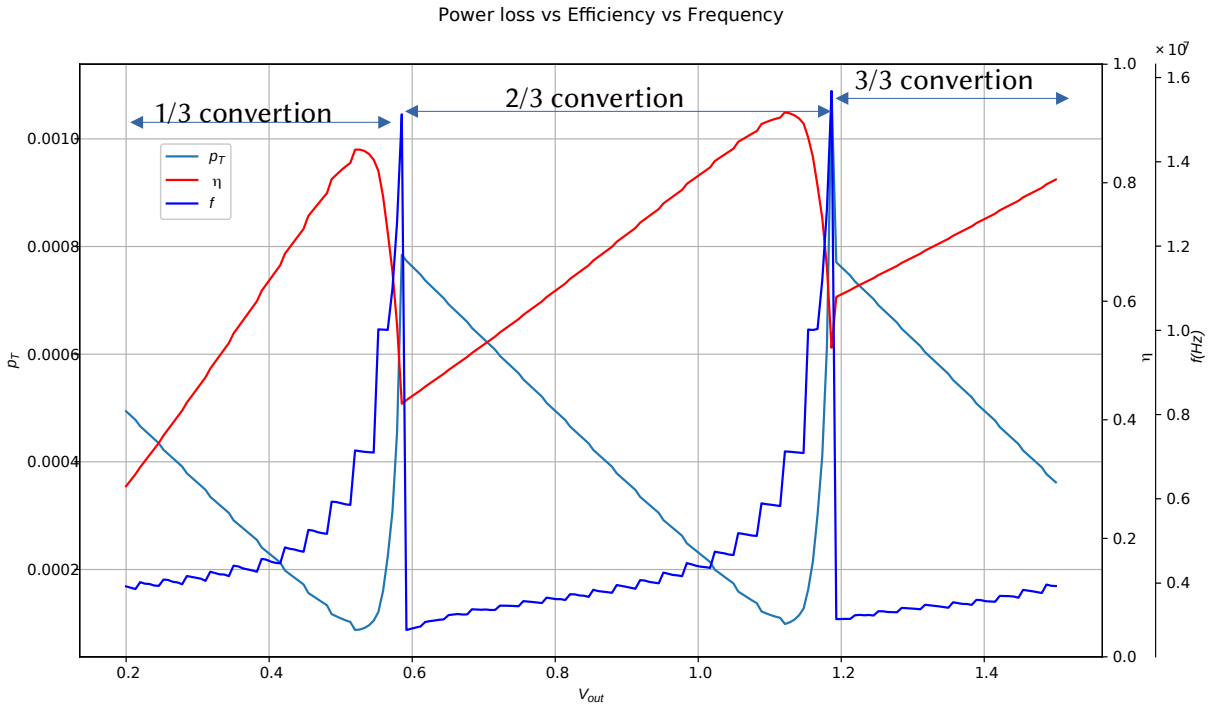

Figure 3.4.5: Power Loss, Efficiency and Frequency vs V_{out} Sweep

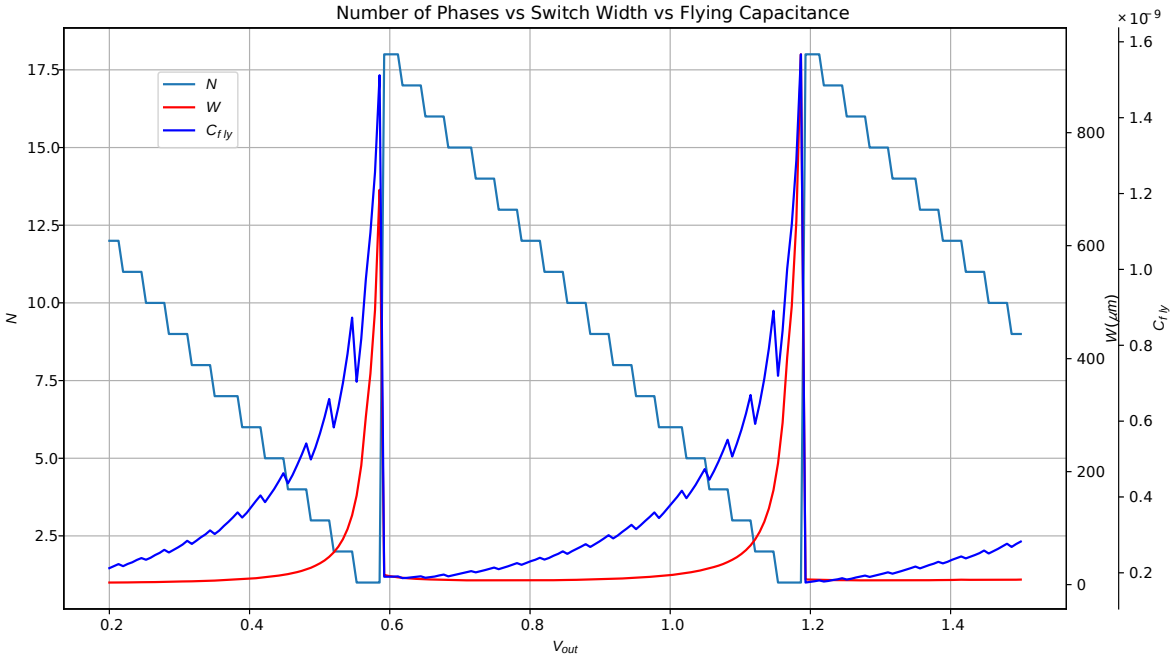

Figure 3.4.6: Number of Phases N, Switch width W and Flying Capacitance vs V_{out} Sweep

Chapter 4

Open-Loop Blocks

4.1 Converter Topology

The optimization process is a way to create a starting point for the design. In order to reduce ripple during transitory load changes, the number of phases was increased to $N = 12$ and the switches sized were reduced.

As it would be hard to fit images for a converter with lots of phases, for the purpose of describing the topology, lets describe an interleaved Converter of only 4 Phases, shown in Fig.4.1.1. This converter is composed of 3 types of blocks:

- **3CapRing:** Each one of these blocks corresponds to one phase of the converter and each contains a 3 Capacitor Ring that rotates according to the Phase signals $V\mathbb{X}0, V\mathbb{X}1, V\mathbb{X}2$, where $\mathbb{X}$ denotes the phases:A, B, C, D. These Signals are high one at a time in the form of Non-Overlapping Pulses, when each one of the 3 is high corresponds to the 3 possible positions of the Capacitor Ring.
  A total cycle lasts $T = 3N_{Phases}T_{sw} = T_{VA0}+T_{VA1}+T_{VA2}$, the switching period is the time between the rise of the same voltage for two consecutive phases: $T_{sw} = t[V(B)0] - t[VA0]$.

- **NOPG:** Non-Overlapping Pulse Generator: This block is the one that generates all the signals that rotate each Capacitor Ring when it corresponds.

- CCO **Current Controlled Oscillator:** This is a modified Ring Oscillator that creates the clock signal with frequency proportional to its input current.

Each of the 3CapRing blocks is composed of 2 blocks, as shown in Fig.4.1.2:

- **Switches and Capacitors:** CMOS Switches that connect the 3 capacitance between one another and with the input voltage and output voltage. It's commanded by the signals of the Logic Circuity, and its output are the gate voltages of the switches.

- **Logic:** This block controls when the Switches commute, making sure the Switches commute in correct order to guarantee that no short circuit happens. The outputs are a Logic Function of the Switches Gate Voltages, the Phase Signals VX0, VX1, VX2, and the bit0, bit1 signals that determine the conversion ratio.

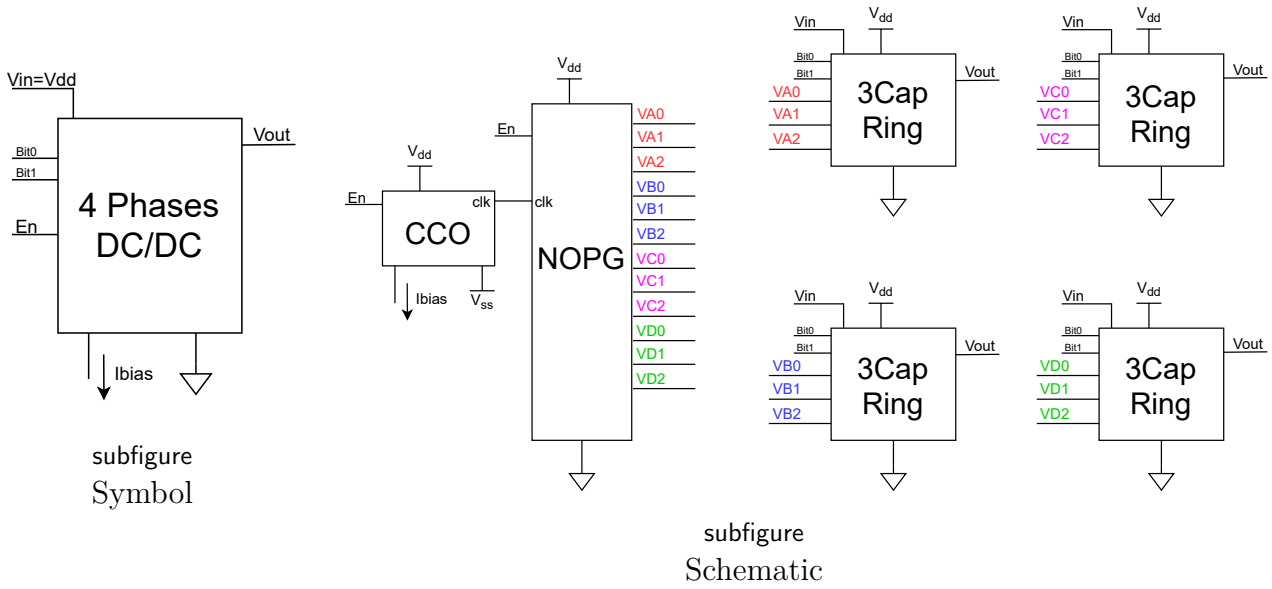

Figure 4.1.1: 4 Phases Open Loop Switched Capacitor Converter

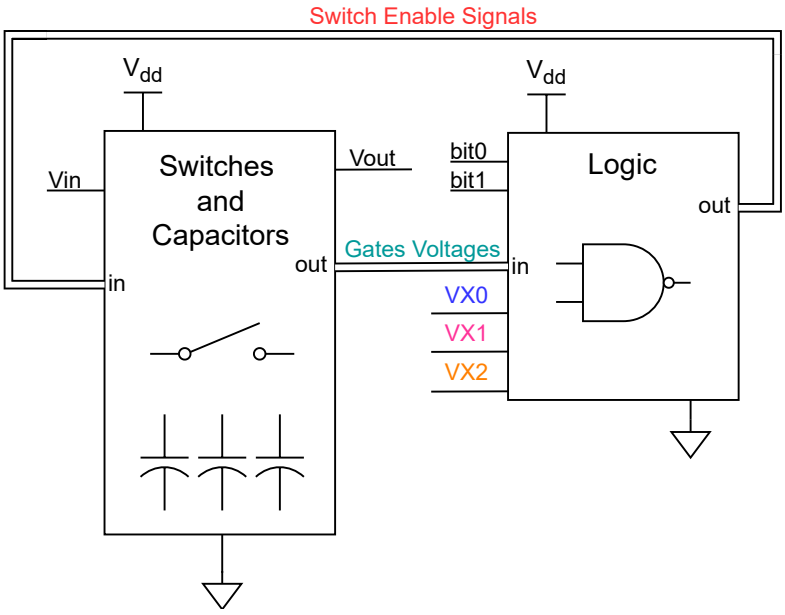

Figure 4.1.2: 1 Phase Open Loop Switched Capacitor Converter

4.2 3CapRing

The 3 Capacitor Ring's schematic is shown in Fig.4.2.1. Each Capacitor has 4 Switches whose state determines the positions of each Capacitor in the ring. A Switch S_{in} is connected only to the top Capacitor and a Switch S_{gnd} is connected only to the bottom capacitor. The Switch S_{out} is connected according to the voltage conversion ratio to the capacitor which in a given time gives the desired voltage conversion ratio. Finally the Switch S_{inter} is connected to all Capacitors, except the top capacitor, to close the ring between V_{in} and ground.

Taking for example a 1/3 Voltage Conversion Ratio, let's see in Fig.4.2.3. The load is

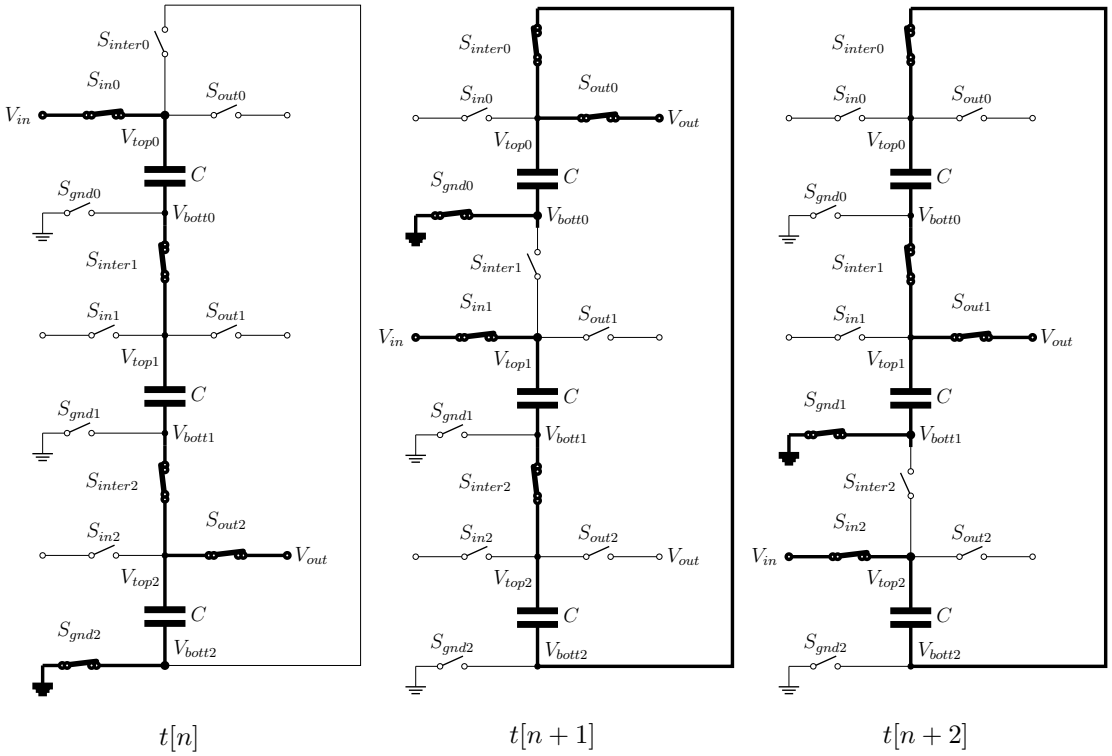

Figure 4.2.1: Capacitors and Switches

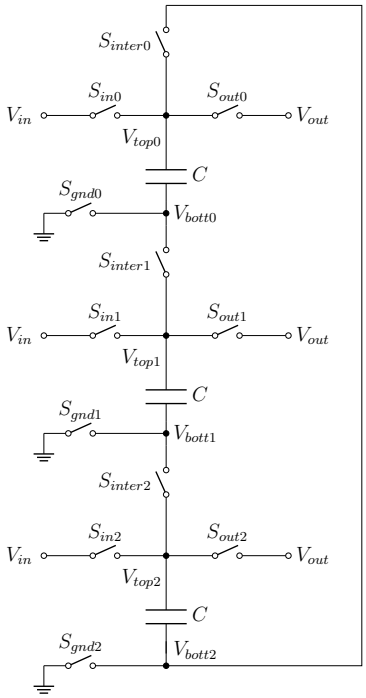

Figure 4.2.2: Capacitors-Switches Cell

composed of an output capacitor C_{out} and a current source I_L. Each of the 3 Capacitors will rotate in each period, passing the bottom one to the top and the top and middle ones go down

one position. In Fig.4.2.4 we see the Ring Rotation from time $t[n]$ to time $t[n+1]$. The figure to the left represents the state at the end of time $t[n]$, at this time the output voltage is $V_{out}[n]$. Notice that the top Capacitor Voltage is the last output voltage $V_{out}[n-1]$ plus the charge that delivered the input in this period, which is a third of the output charge. The figure to the right shows the state right before the switches close and the time $t[n+1]$ begins, as the capacitors rotate the top Capacitor moves to the middle and the bottom Capacitor moves to the top. In order to find a differences equation for out discrete time circuit charge balance is implemented in Eq.4.1, equating charge at time $t[n]$ and $t[n+1]$. So in order to find the voltages at time $t[n+1]$ we equate the charges before and after the closing of the switches of Fig.4.2.4. Note that after the switches close the source will deliver a charge $Q[n+1]/3$ and the load will take a charge $Q[n+1]$, which corresponds to charges that enter and output the ring at time $t[n+1]$ respectively.

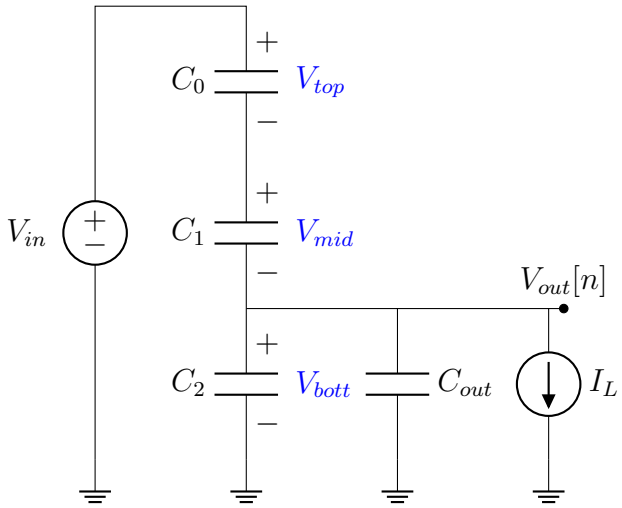

Figure 4.2.3: 1/3 Convertion Ratio

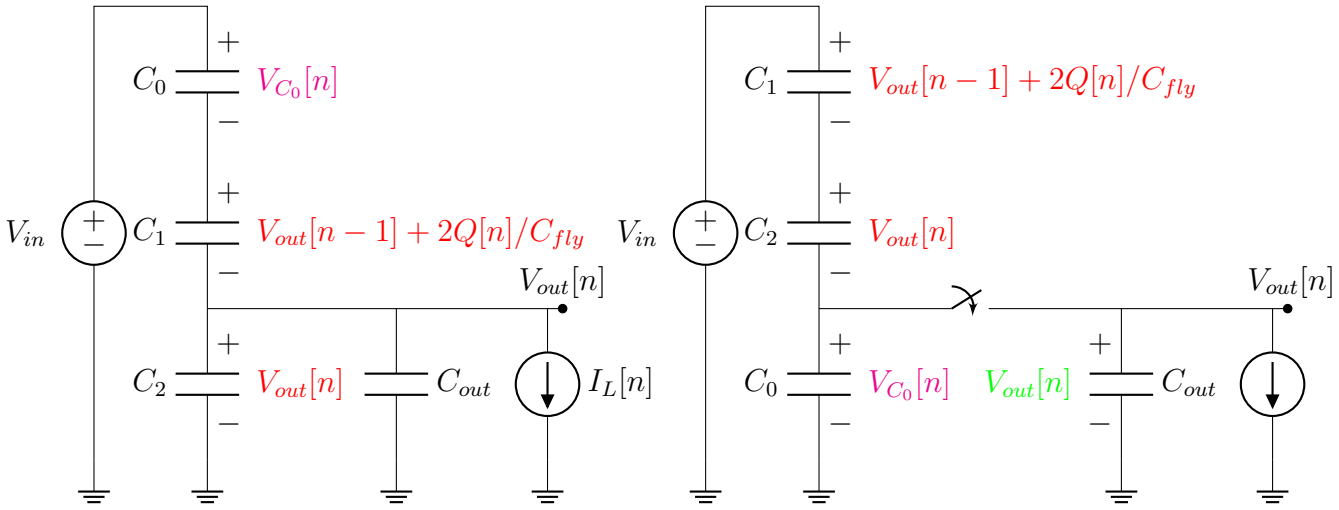

Figure 4.2.4: Capacitor Ring Rotation time $t[n]$

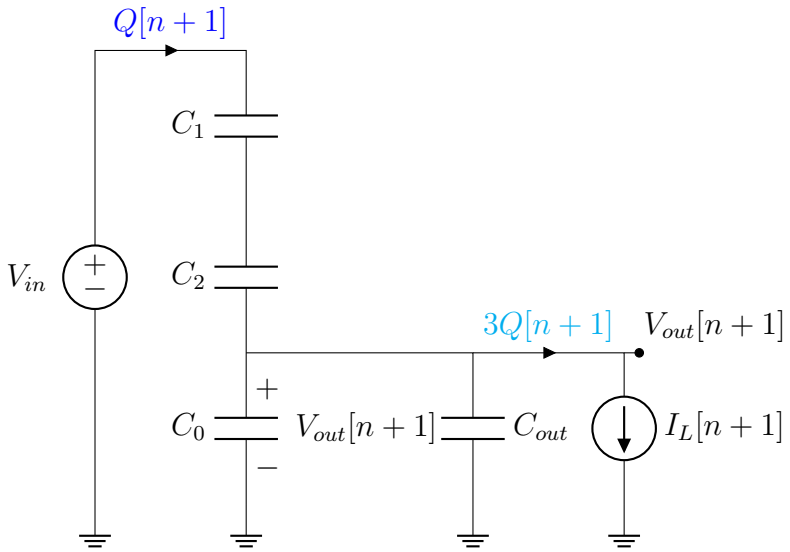

Figure 4.2.5: Capacitor Ring Rotation time $t[n+1]$

$$\begin{aligned}
&\frac{C_{fly}}{2}\left[V_{out}[n]+V_{out}[n-1]+\frac{2Q[n]}{C_{fly}}\right] \\
&+C_{fly}\left[V_{in}-V_{out}[n]-V_{out}[n-1]-\frac{2Q[n]}{C_{fly}}\right] \\
&+C_{out}V_{out}[n]+\frac{C_{fly}}{2}\frac{2Q[n+1]}{C_{fly}} \\
&=3Q[n+1]+\frac{C_{fly}}{2}\left[V_{in}-V_{out}[n+1]\right]+(C_{out}+C_{fly})V_{out}[n+1]
\end{aligned} \tag{4.1}$$

$$\begin{cases} 3Q[n] = I_L[n]T_s \\ 3Q[n+1] = I_L[n+1]T_s \end{cases} \tag{4.2}$$

$$\begin{aligned}
&-\frac{C_{fly}}{2}\left[V_{out}[n]+V_{out}[n-1]\right]+C_{fly}V_{in}+C_{out}V_{out}[n]-I_L[n+1]T_s \\
&=\frac{C_{fly}}{2}(V_{in})+(C_{out}+C_{fly}/2)V_{out}[n+1]
\end{aligned} \tag{4.3}$$

Using Eq.4.1 and taking Z Transform we obtain a transfer function in Eq.4.4. The transfer function has two poles and corresponds to a overdamped second order system, which means the poles are real, as long as C_{out} is sufficiently greater than C_{fly}, when $C_{fly} = 2/3C_{out}$ the system becomes critically damped.

$$V_{out}[z] = \frac{\frac{z^2}{z-1}\frac{V_{in}C_{flu}/2}{C_{out}+C_{fly}/2} - \frac{z^2 I_L[z]T_s}{C_{out}+C_{fly}/2}}{z^2 - \frac{C_{out}-C_{fly}/2}{C_{out}+C_{fly}/2}z + \frac{C_{fly}/2}{C_{out}+C_{fly}/2}} \tag{4.4}$$

$$z_p = \frac{1}{2}\frac{\frac{C_{out}}{C_{fly}} - \frac{1}{2} \pm \sqrt{\left(\frac{C_{out}}{C_{fly}} - \frac{1}{2}\right)^2 - 2\left(\frac{C_{out}}{C_{fly}} + \frac{1}{2}\right)}}{\frac{C_{out}}{C_{fly}} + \frac{1}{2}} \tag{4.5}$$

$$z_p = \frac{1}{2}\frac{1 - \frac{C_{fly}}{2C_{out}} \pm \sqrt{\left(1 - \frac{C_{fly}}{2C_{out}}\right)^2 - \left(2\frac{C_{fly}}{C_{out}} + \left(\frac{C_{fly}}{C_{out}}\right)^2\right)}}{1 + \frac{C_{fly}}{2C_{out}}} \tag{4.6}$$

$$z_p \approx \frac{1}{2}\frac{1 - \frac{C_{fly}}{2C_{out}} \pm \sqrt{1 - 3\frac{C_{fly}}{C_{out}}}}{1 + \frac{C_{fly}}{2C_{out}}} \approx \frac{1}{2}\frac{1 - \frac{C_{fly}}{2C_{out}} \pm \left(1 - \frac{3}{2}\frac{C_{fly}}{C_{out}}\right)}{1 + \frac{C_{fly}}{2C_{out}}} \tag{4.7}$$

$$\tag{4.8}$$

If we take $C_{out} \gg C_{fly}$ the poles can be approximated according to Eq.4.9, with a sufficiently big C_{out} the z_p approaches 1 and 0. The continuous time poles are shown in Eq.4.10, they are proportional to the switching frequency and with a sufficiently big C_{out} the w_p approaches 0 and infinity. Using the equality $(N-1)C_{fly} = 2/3C_{out}$:

$$z_p \underset{C_{out} \gg C_{fly}}{\approx} \begin{cases} \frac{1-C_{fly}/C_{out}}{1+C_{fly}/2C_{out}} & \approx \frac{N-2}{N-1/2} \underset{N=12}{\approx} 0.87 \\ \frac{C_{fly}}{2C_{out}} & \approx \frac{1}{2(N-1)} \underset{N=12}{\approx} 0.045 \end{cases} \tag{4.9}$$

$$f_p \overset{f_s=116kHz}{\underset{C_{out} \gg C_{fly}}{\approx}} \begin{cases} -2\pi f_s log\left[\frac{1-C_{fly}/C_{out}}{1+C_{fly}/2C_{out}}\right] \underset{N=12}{\approx} 44kHz \\ -2\pi f_s log\left[\frac{C_{fly}}{2C_{out}}\right] \underset{N=12}{\approx} 980kHz \end{cases} \tag{4.10}$$

If we take $I_L[n] = I_L Y[n]$ as step function the transfer function becomes the one in Eq.4.11. The final time value can be obtained using the Final Value Property of the z Transform, Eq.4.12, here we obtain the steady state Thevenin equivalent with the No Load Voltage $V_{NL} = V_{in}/3$ and the output resistance $R_{out} = 2/3/f_s C_{fly}$.

$$I_L[z] = \frac{z}{z-1} I_L \Rightarrow V_{out}[z] = \frac{\frac{z^2}{z-1}\left(\frac{V_{in}C_{flu}/2}{C_{out}+C_{fly}/2} - \frac{I_L T_s}{C_{out}+C_{fly}/2}\right)}{z^2 - \frac{C_{out}-C_{fly}/2}{C_{out}+C_{fly}/2}z + \frac{C_{fly}/2}{C_{out}+C_{fly}/2}} \tag{4.11}$$

$$\lim_{n\to\infty} V_{out}[n] = \lim_{z\to 1}(z-1)V_{out}[z] = \frac{V_{in}}{3} - \frac{2}{3}\frac{I_L}{f_s C_{fly}} = V_{NL} - R_{out} I_L \tag{4.12}$$

$$R_{out} = \frac{K}{f_s C_{fly}} \tag{4.13}$$

This value can be verified using the charge multiplier vector, Eq.4.14, which is formed by the fractions of the charges that each capacitor receives or delivers each period divided by the total charge delivered to the load. Using Tellegen's Theorem we can find an equation for the output resistance, Eq.4.17. In our case, the charge multiplier vector is shown in Eq.4.18 and verify the value obtained for the output resistance.

$$a = [\, Q_{out} \quad Q_1 \ \ldots \ Q_n \,]/Q_{out} = [\, 1 \quad a_c \,] \tag{4.14}$$

$$\begin{cases} Q_{out} v_{out} + \sum_{cap} Q_i \Delta v_i = 0 \\ \Delta_i = Q_i / C_i \end{cases} \tag{4.15}$$

$$\frac{v_{out}}{Q_{out}} + \sum_{cap} \left(\frac{Q_i}{Q_{out}} \right)^2 \frac{1}{C_i} = 0 \tag{4.16}$$

$$R_{out} = -\frac{v_{out}}{Q_{out}} = \sum_i \frac{a_{c,i}^2}{f_{sw} C_i} \tag{4.17}$$

$$a = [\, 1 \quad 1/3 \quad 1/3 \quad 2/3 \,] \Rightarrow R_{out} = \frac{2}{3} \frac{1}{f_s C_{fly}} \tag{4.18}$$

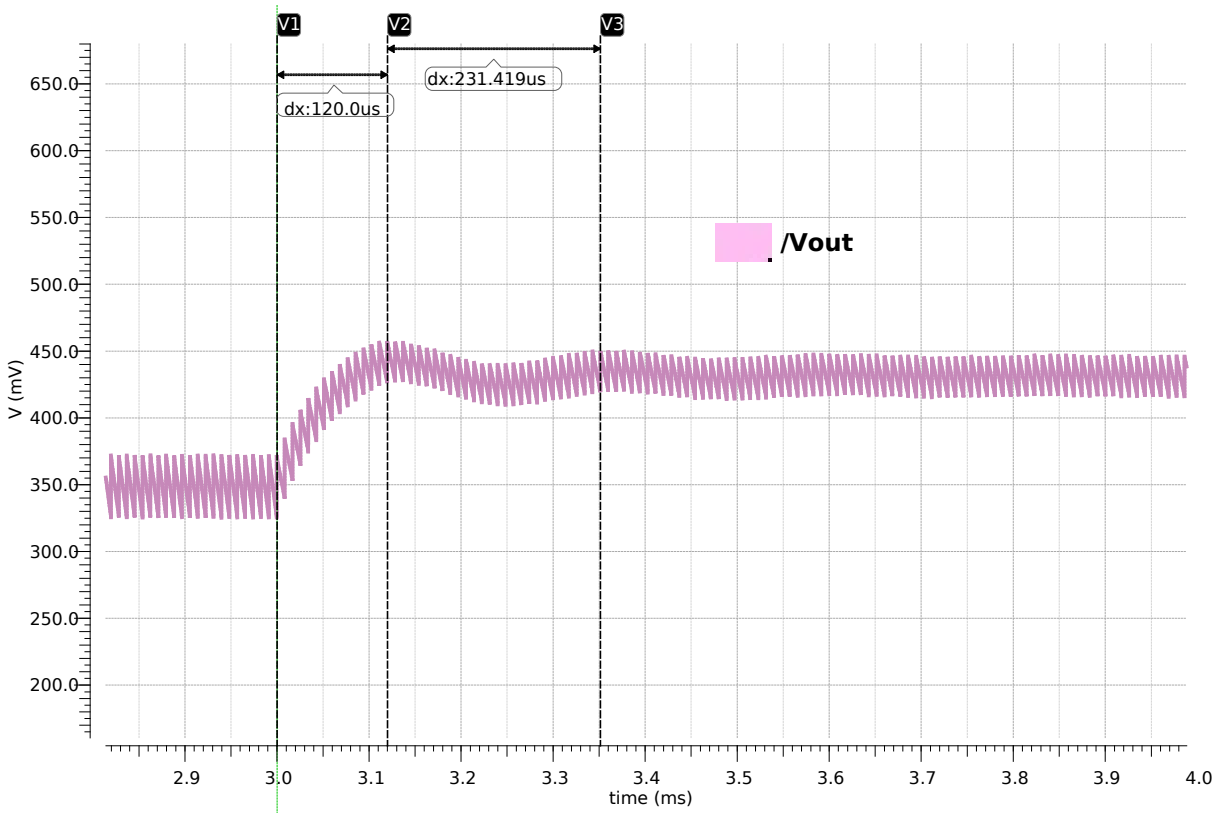

Figure 4.2.6: OpenLoop I_L step from $1.2u$ to $800n$ at $F_{sw} = 116k$.

However, when observing the open-loop response to a step in the load current I_L, as shown in Fig.4.2.6, it can be seen that the $N = 12$ phases system presents second-order system behavior. Eq.4.11 refers to a singly phase switching at frequency F_{sw}, but actually the converter is composed of N phases switching at a frequency F_{sw}/N. So for a single-phase there wouldn't be a $[n-1]$ and $[n-2]$ delays but a $[n-12]$ and $[n-24]$ delays. This means that previously calculated poles of Eq.4.9 would take the form:

$$x_p = z_p^{12} \tag{4.19}$$

$$x_p = \frac{1}{2}\frac{\frac{C_{out}}{C_{fly}} - \frac{1}{2} \pm \sqrt{\left(\frac{C_{out}}{C_{fly}} - \frac{1}{2}\right)^2 - 2\left(\frac{C_{out}}{C_{fly}} + \frac{1}{2}\right)}}{\frac{C_{out}}{C_{fly}} + \frac{1}{2}} \tag{4.20}$$

$$z_p = x_p^{1/12} e^{\frac{j2i\pi}{N}} \underset{dominant\ pole}{\Rightarrow} z_p = \left(\frac{1 - C_{fly}/C_{out}}{1 + C_{fly}/2C_{out}}\right)^{1/12} e^{\frac{j2i\pi}{N}},\ i \in [1, 12] \tag{4.21}$$

$$f_p = -f_s \log\left[\frac{1 - C_{fly}/C_{out}}{1 + C_{fly}/2C_{out}}\right]^{12} = -\frac{f_s}{12} log\left[\frac{1 - C_{fly}/C_{out}}{1 + C_{fly}/2C_{out}}\right] \underset{\text{N=12}}{\overset{f_s=156kHz}{\approx}} 3.7KHz \tag{4.22}$$

$$T_p = 1/f_p \approx 270\mu s \tag{4.23}$$

Then each phase adds 5 second-order systems with a phase delay T_s. We can see that the period calculated in Eq.4.23 is close to the oscillation's period, present in the step response of Fig.4.2.6.

The actual C_{fly} capacitor used were the XT018 mosvc 1.8V N-type Varactor , see Fig.4.2.11. Which have a capacitance of $8fF/\mu m^2$, each capacitor is $40\mu m \times 40\mu m$ giving a capacitance of $C_{fly} = 12.8pF$.
The Switch's sizes are depicted in Table 4.1, although in the previous chapter it was assumed that all switches would have the same size, as the ground and input switches are close to ground and V_{DD} respectively, this switches can be smaller and can be implemented with a single Mosfet, while the inter and output switch must be larger CMOS switches. Images of the Switch's schematics with their buffers are presented in Fig.4.2.7 to Fig.4.2.10.

Switch	type	$W(\mu m)$	$n_{fingers}$	Total $W(\mu m)$
SwIn	pMos	2.2	2	4.4
SwGnd	nMos	2.2	1	2.2
SwInter	2nMos//pMos	2.2	6	13.2
SwOut	2nMos//pMos	1.1	4	4.4

Table 4.1: Switches Sizes

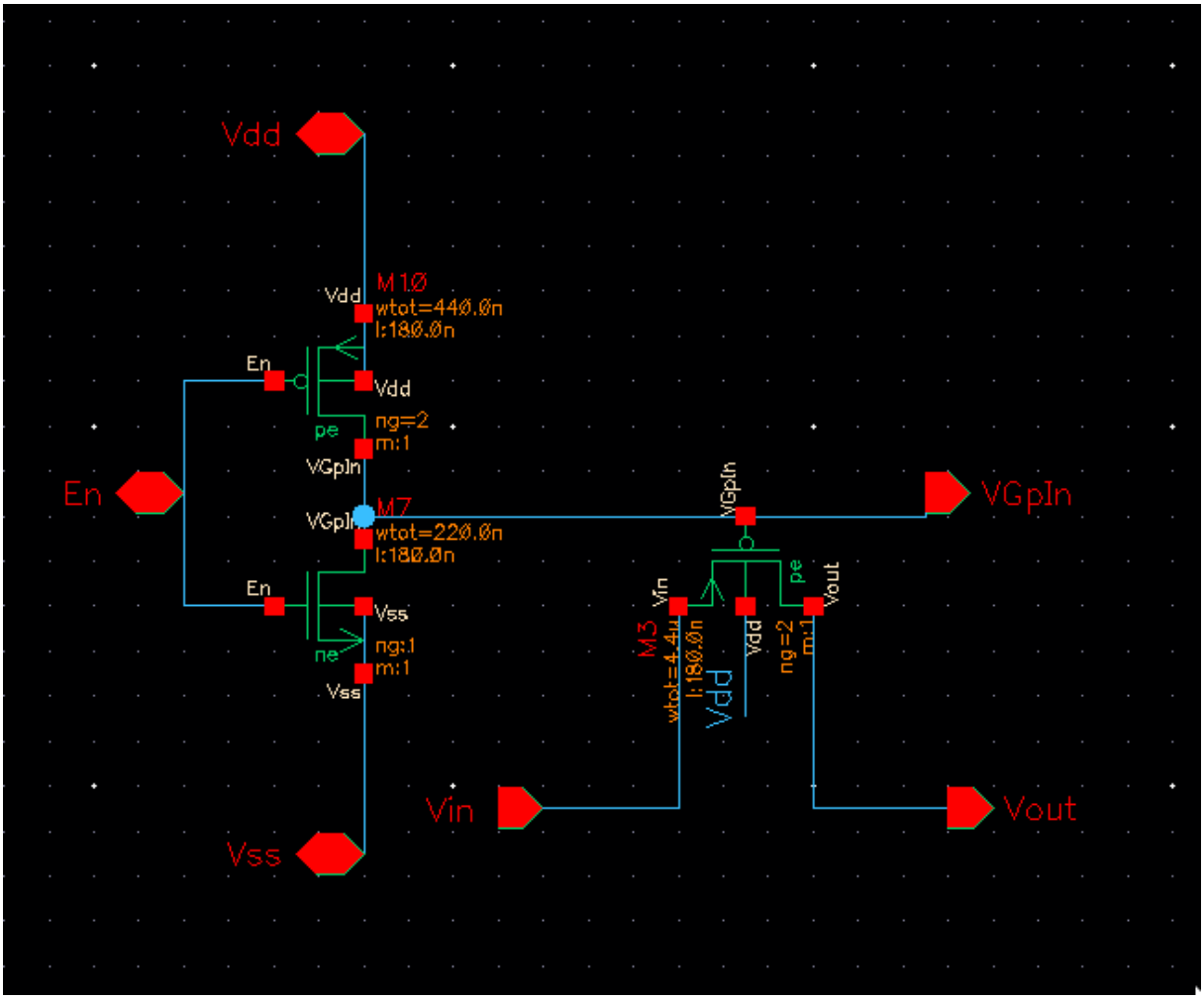

Figure 4.2.7: Input Switch

4.3 Logic

The logic circuitry controls when the switches commute, each switch must wait for the connected input, output, ground, and inter switches to turn off before turning itself on when it corresponds. To do this a logic was built that implements the logic functions shown in Eq.4.25. Where:

- $\frac{2}{3}$ and $\frac{1}{3}$ are true only when the conversion ratio is 2/3 and 1/3 respectively, and can only be true one at a time.
- V_i are the position voltages of the ring.
- F_i is a logic function that is true when each of the i-th capacitors is in the top position and all switches from the previous period that must turn off have effectively turn off.
- $S_{in_i}, S_{out_i}, S_{inter_i}, S_{gnd_i}$ are logic functions that are true when the corresponding switch is

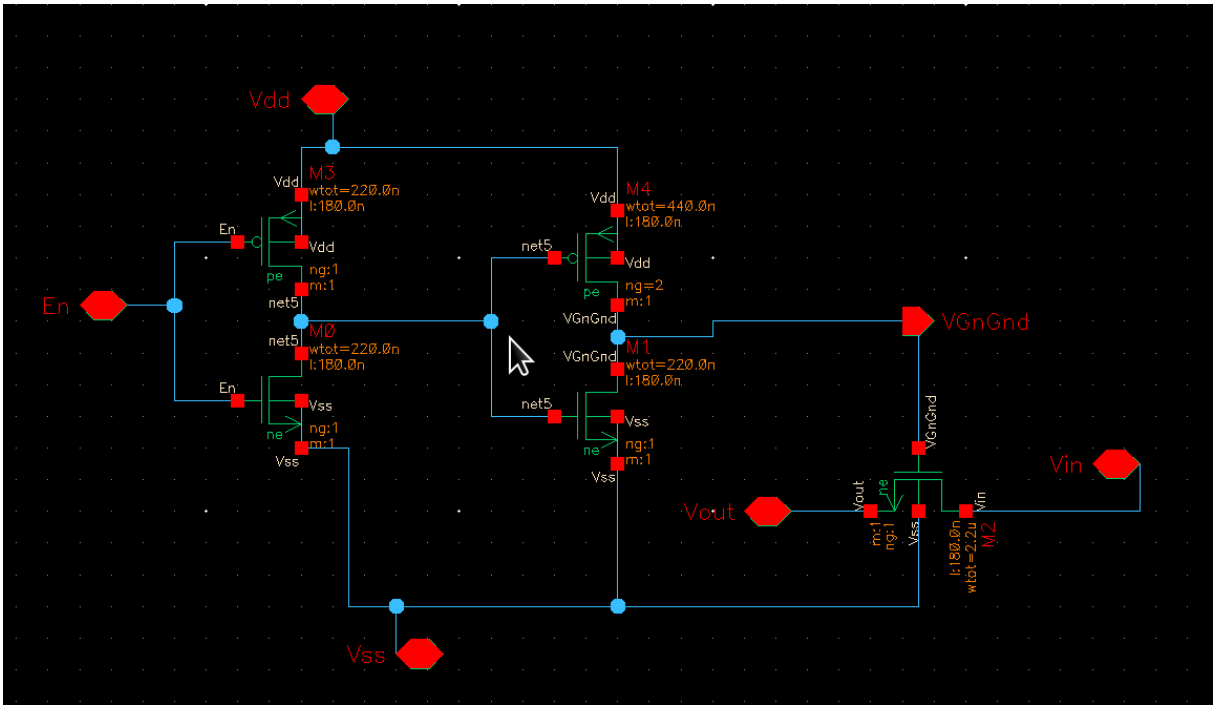

Figure 4.2.8: Ground Switch

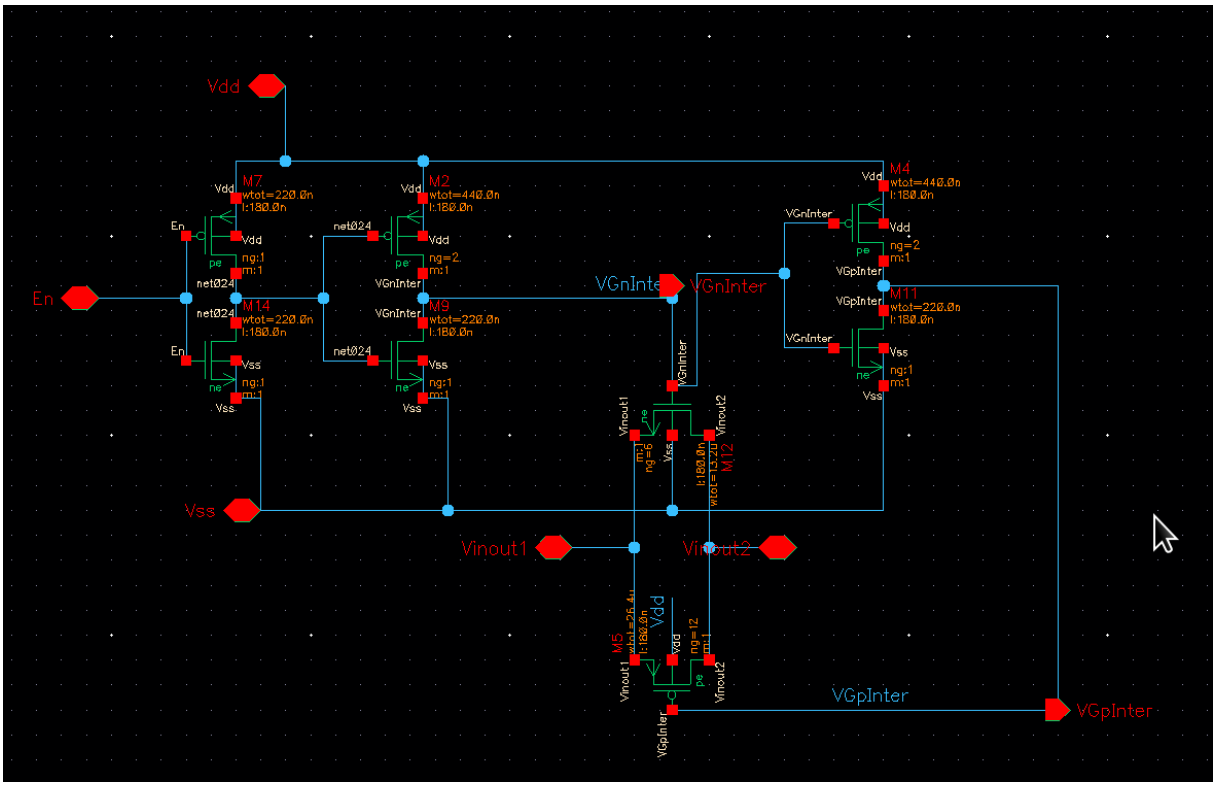

Figure 4.2.9: Inter Switch

on.

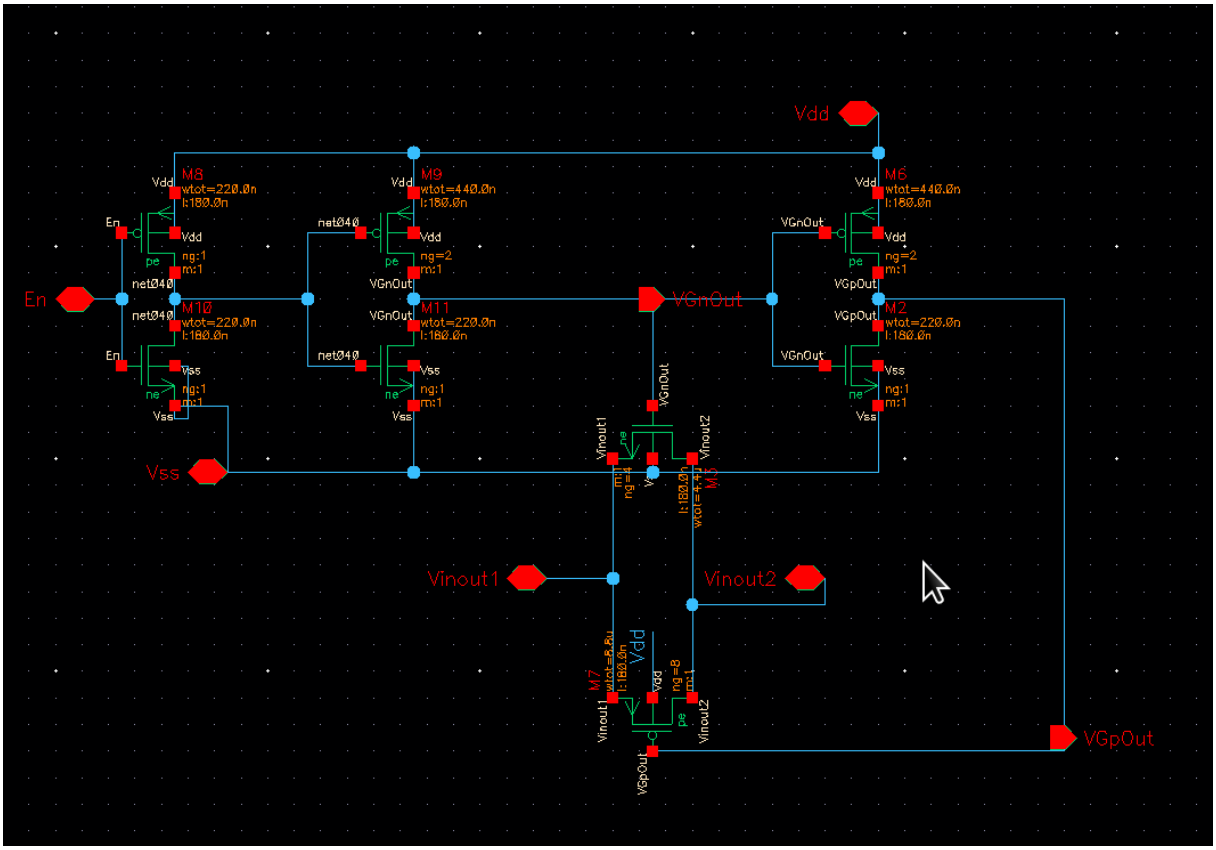

Figure 4.2.10: Output Switch

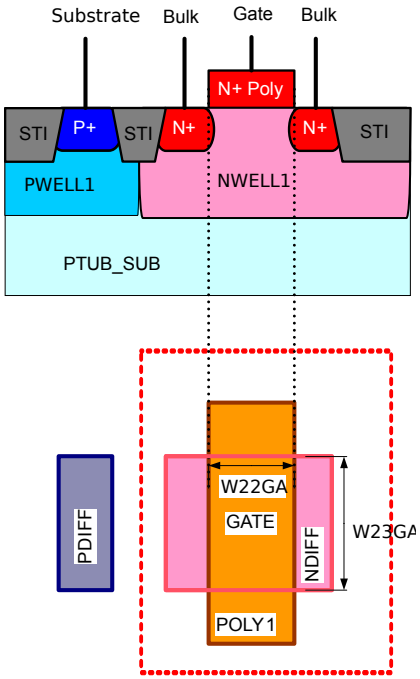

Figure 4.2.11: Varactor Mosfet used as Capacitor

$$\begin{cases} \frac{1}{3} = \overline{bit0}\ \overline{bit1} \\ \frac{2}{3} = \overline{bit0}\ xor\ \overline{bit1} \end{cases} \tag{4.24}$$

$$\begin{cases} F_i = V_i\ \overline{S_{gnd_i}}\ \overline{S_{in\frac{i+2}{3}}}\ \overline{S_{inter_i}} \left(\frac{2}{3}\ \overline{S_{out_i}} \ + \ \frac{1}{3}\ \overline{S_{out\frac{i+1}{3}}} \right), \quad i \in \{0,1,2\} \\ S_{inter\frac{i+2}{3}} \ = F_i + V_{\frac{i+1}{3}} \\ S_{in_i} \ = \ S_{gnd\frac{i+2}{3}} \ = F_i \\ S_{out_i} \ = \ \left[\frac{2}{3} V_{\frac{i+2}{3}} F_{\frac{i+2}{3}} + \frac{1}{3} V_{\frac{i+1}{3}} F_{\frac{i+1}{3}} \right] \overline{S_{out\frac{i+2}{3}}} \end{cases} \tag{4.25}$$

This logic functions exist for all of the N Phases of the converter.

4.4 Non-Overlapping Pulse Generator

Until now we have defined what is necessary to create a one-Phase converter, which is the block named 3CapRing from Fig.4.1.1. Each 3CapRing composes one Phase of the Converter and has as input 3 position voltages that determine the position of Capacitor Ring, in the 4 Phases example of Fig.4.1.1 there are in total 12 Position Voltages. These voltages are composed of 4 groups of non-overlapping pulses delayed T/N_{Phases}, a graphic is shown in Fig.4.4.1. These pulses are generated by the block in Fig.4.4.2, which is a circular ring of 12 level-sensitive latches. One third of these latches are preloaded with ones and two thirds are preloaded with zeros, synchronously. The even latches are connected to the clock signal and the odd latches are connected to the negated clock signal so that when the clock is high the even latches copy its input to its output and the odd latches maintain their value when the clock signal is low the reverse happens. So that when the clock is high the even latches propagate their input, and when the clock is low the odd latches propagate their input. In this way the group of ones advances two positions each clock cycle, each output of the 12 latches corresponds to the 12 Positions Voltages.

A simplified version of the Latch used appears in Fig.4.4.3, when the clock is high the second Switch is enabled and the second is disabled, so the input is disconnected from the output and the latch maintains its last value. When the clock is low, the first switch is enabled and the second disables, so the input is copied to the output.

The schematic of the actual Latch used is shown in Fig.4.4.4, here two functionalities are added. One is the possibility to set/preset the Latch's output by changing the inverters for nor gates. The other extra function is to implement clock gating in the latch, this is done by adding one extra switch which is only enabled when the Latch's output and the next Latch's output are different, indicating that this Latch must conmutate in the next cycle. The clock gating is implemented to reduce the clock power, as power is a restriction, with clock gating the power consumed by the clock is reduced by a factor of $2/N_{Phases}$, and as we have already seen, when frequency increases digital power produces a degradation of the efficiency.

The actual number of phases used was increased to $N = 12$ to further reduce output ripple, in the Fig.4.4.5 we see a simulation of 25 out of the 36 position voltages of the

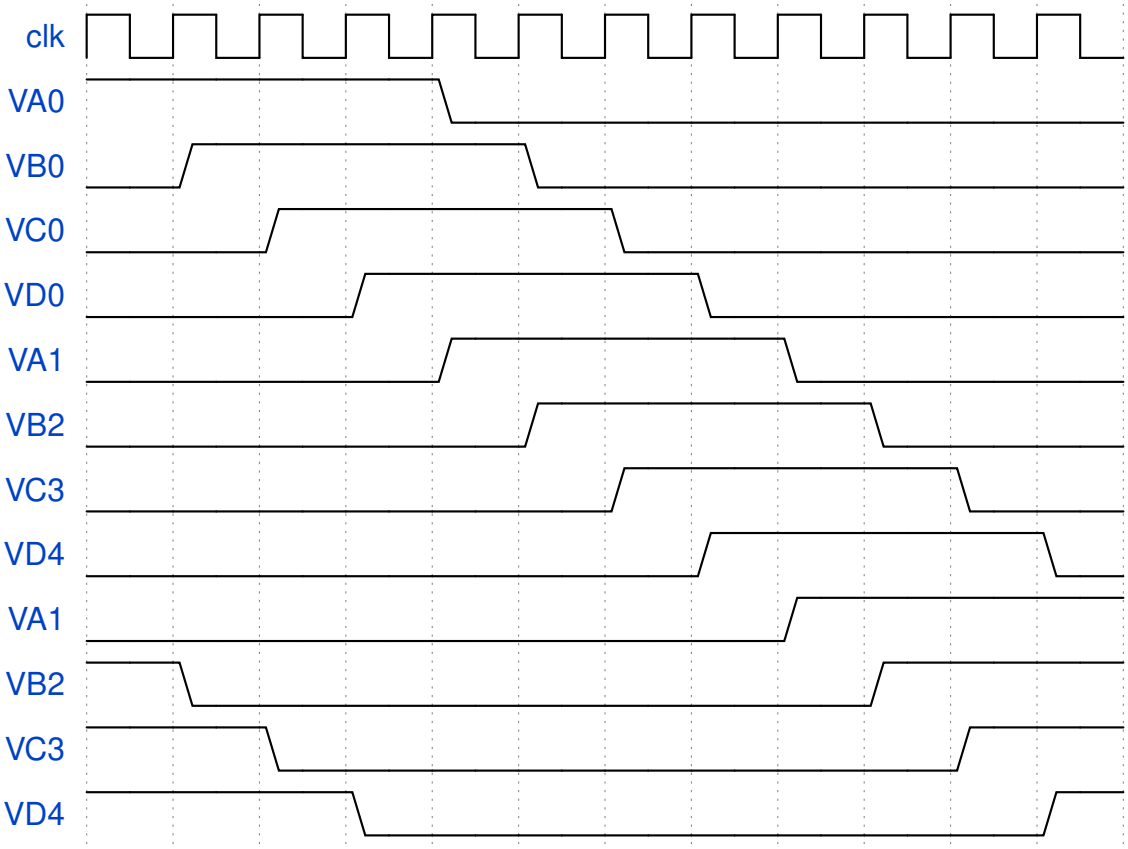

Figure 4.4.1: 4 Phases Non-Overlapping Pulses

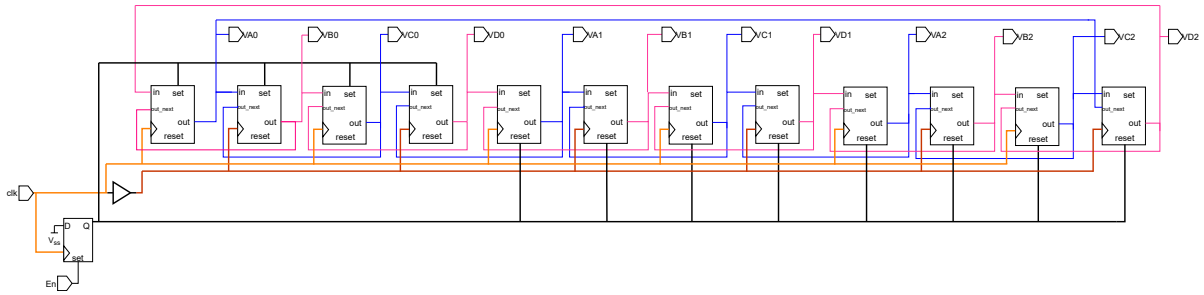

Figure 4.4.2: 4 Phases Non Overlapping Pulse Generator

12 Phases converter for a clock frequency of $f_{clk} = 100kHz$. The load is composed of 36 $C_L = 0.1fF$ for each of the outputs.

In Fig.4.4.6 the Power demand vs frequency of operation of the Non-Overlapping Pulse Generator is shown. The graph depicts the total power demand and the clock main inverter power demand, as we can see from the two curves, at frequencies below $10KHz$ the power demand is dominated by leakage currents, so the minimum power achievable is $P_{min} = 17nW$. While for frequencies above $100kHz$ the power demand is dominated by dynamic power, with the clock main inverter consuming almost half the power. The maximum frequency of operation was estimated to be approximately $f_{Max} = 500MHz$.

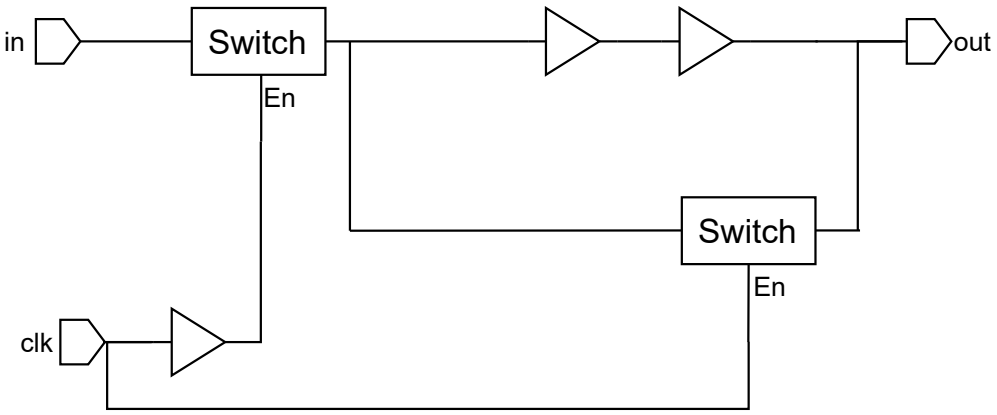

Figure 4.4.3: Simplified Latch

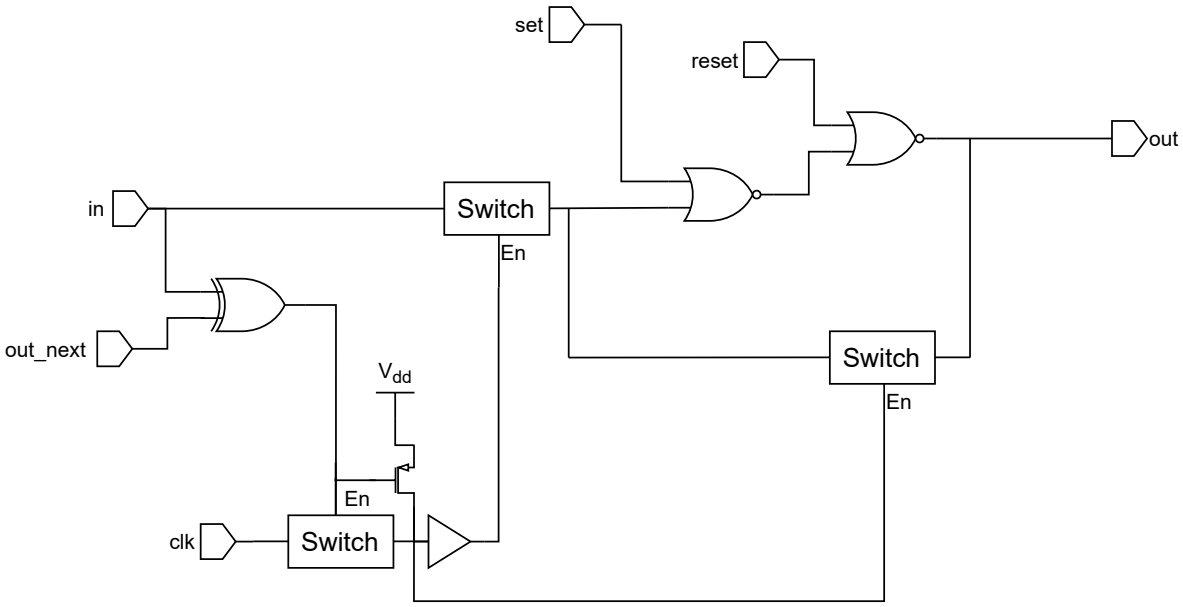

Figure 4.4.4: Latch with clock Gating

4.5 System Efficiency

In Fig.4.5.1 we see the measures of a first type out vs a simulated sweep of the intrinsic effiiency, with a load current from $150pA$ to $5mA$ with a switching frequency f_{sw} so as to maintain an output voltage of approximately $V_{out} = 0.5V$, in a 1/3 voltage conversion. The Figure shows the efficiency of the Open-Loop System excluding the oscillator, efficiencies are marked in orange, with the dashed line representing the intrinsic efficiency of the capacitor ring only. The full orange line represents the total open-loop efficiency. The other lines represent powers, being the highest red line the total power consumed by

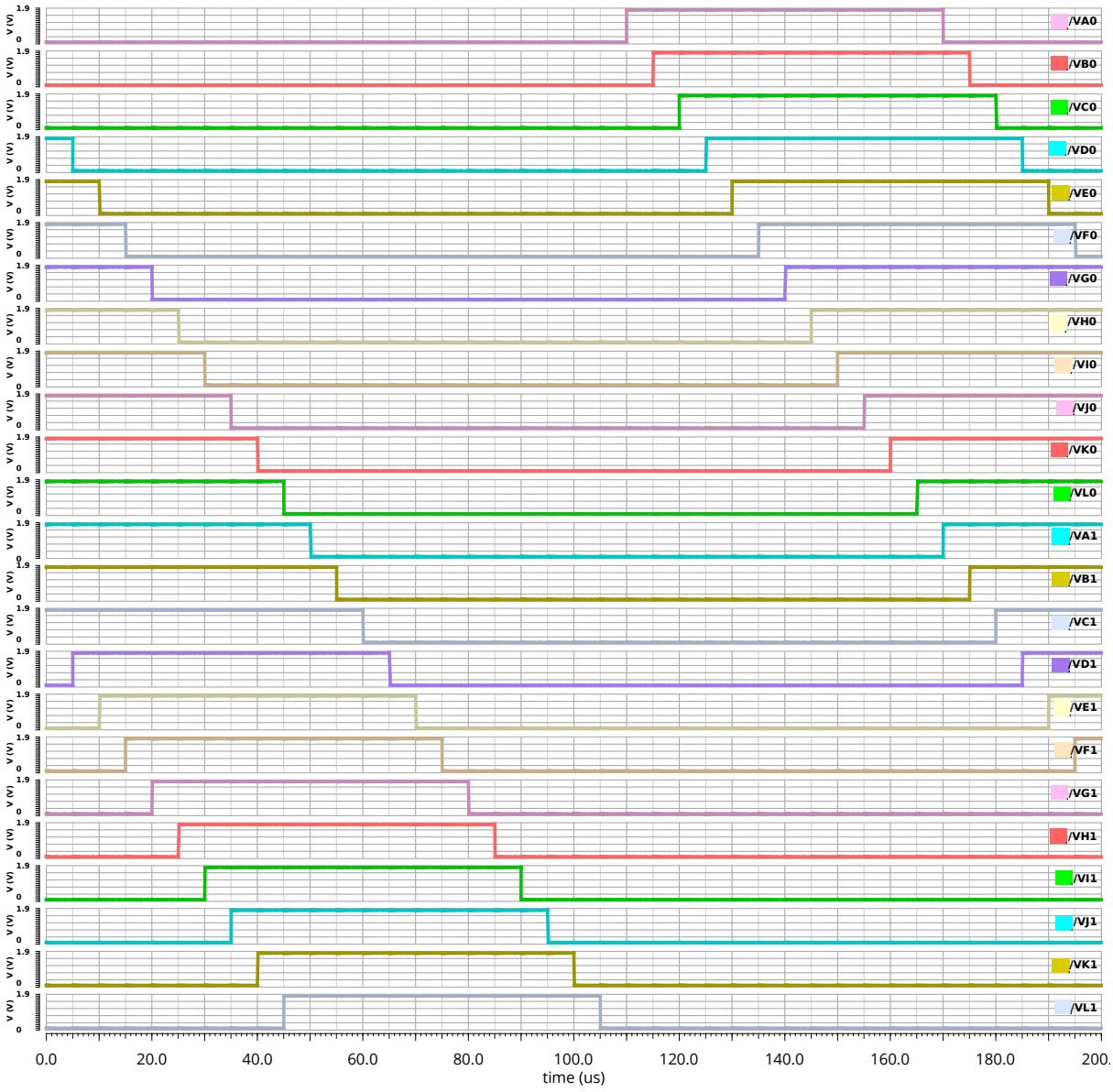

Figure 4.4.5: 12 Phases Non-Overlapping Pulse Generator Pulses

the converter P_{total}, the dashed black line is the input power Pin entering the capacitor ring, and the dotted blue line is the output power.
The clear blue lines with squares, stars, and triangles represent the Logic, Pulse Generator and Switches blocks power consumption respectively.

The difference between intrinsic and total efficiency is given by the power consumption of the Logic, Switches, and Pulse Generator blocks. The difference is significant, which would suggest that bigger capacitors are needed to improve the total efficiency, as bigger capacitors would increase output power, while only increasing input power of switches.
Intrinsic efficiency has a high pole at frequency $100MHz$ and a low pole at $1kHz$. The high-frequency pole is given by the dominant pole of the RC circuit composed of the 3

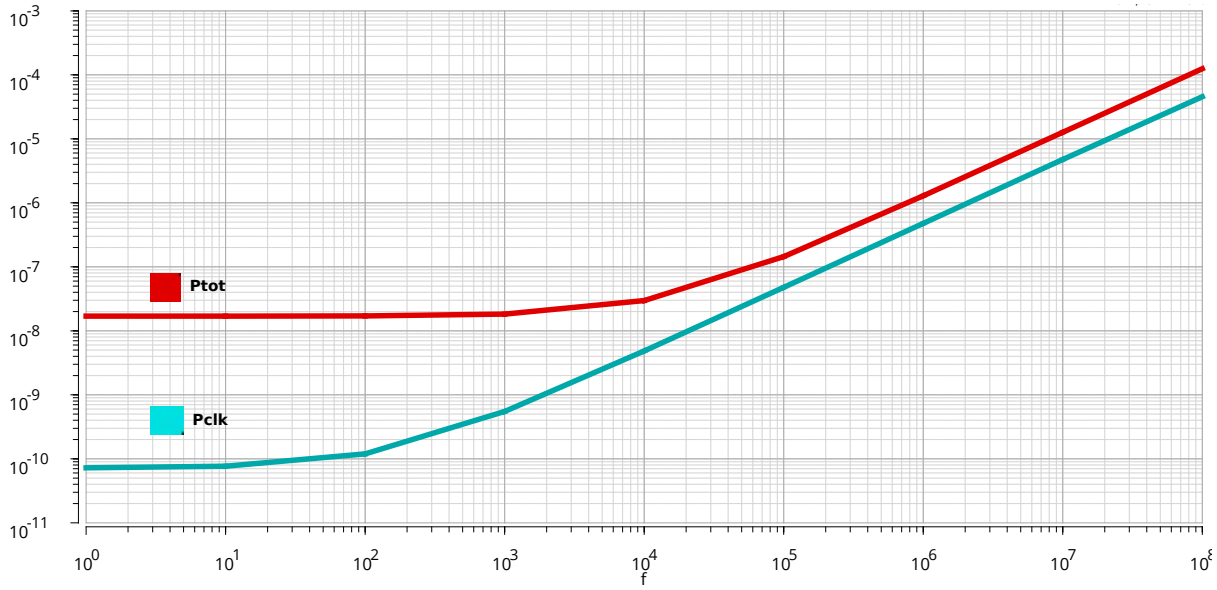

Figure 4.4.6: Non-Overlapping Pulse Generator Power vs Frequency

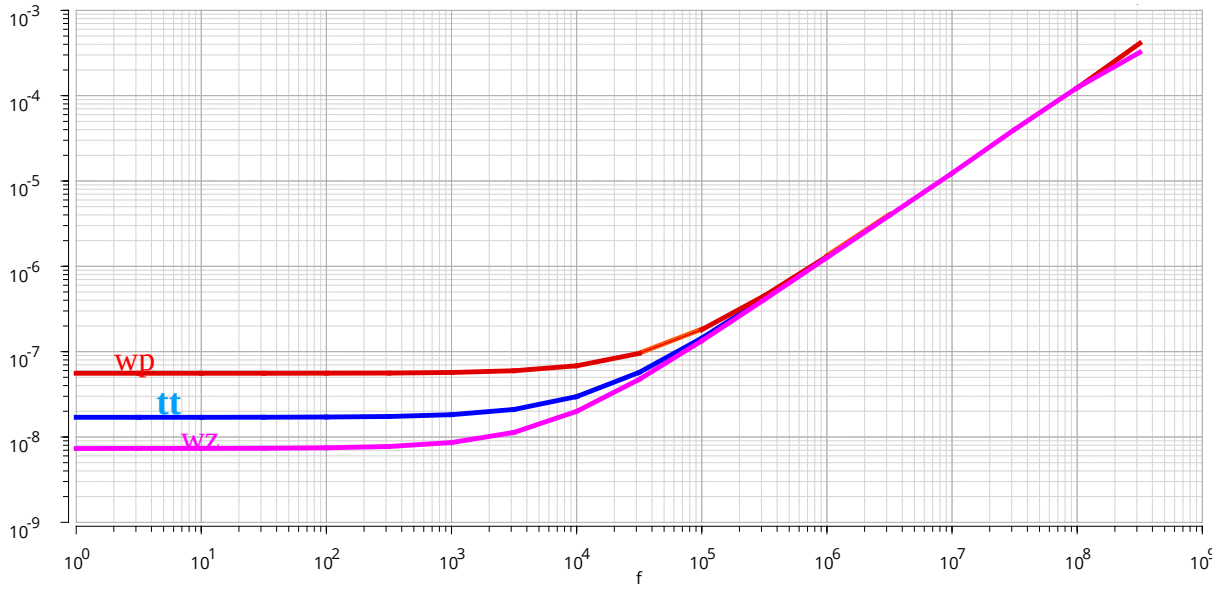

Figure 4.4.7: Non-Overlapping Pulse Generator Power vs Frequency Corners

capacitor ring and their switches. The low-frequency pole is caused by the power lost in the charging/discharging of top/bottom capacities.
The total efficiency shares the high-frequency pole of the intrinsic efficiency, but the low-frequency pole is the consequence of the Logic, Switches, and Pulse Generator blocks having non-proportional power consumption to frequencies, at low frequencies. As these blocks power becomes constant, but output power keeps decreasing, efficiency falls.

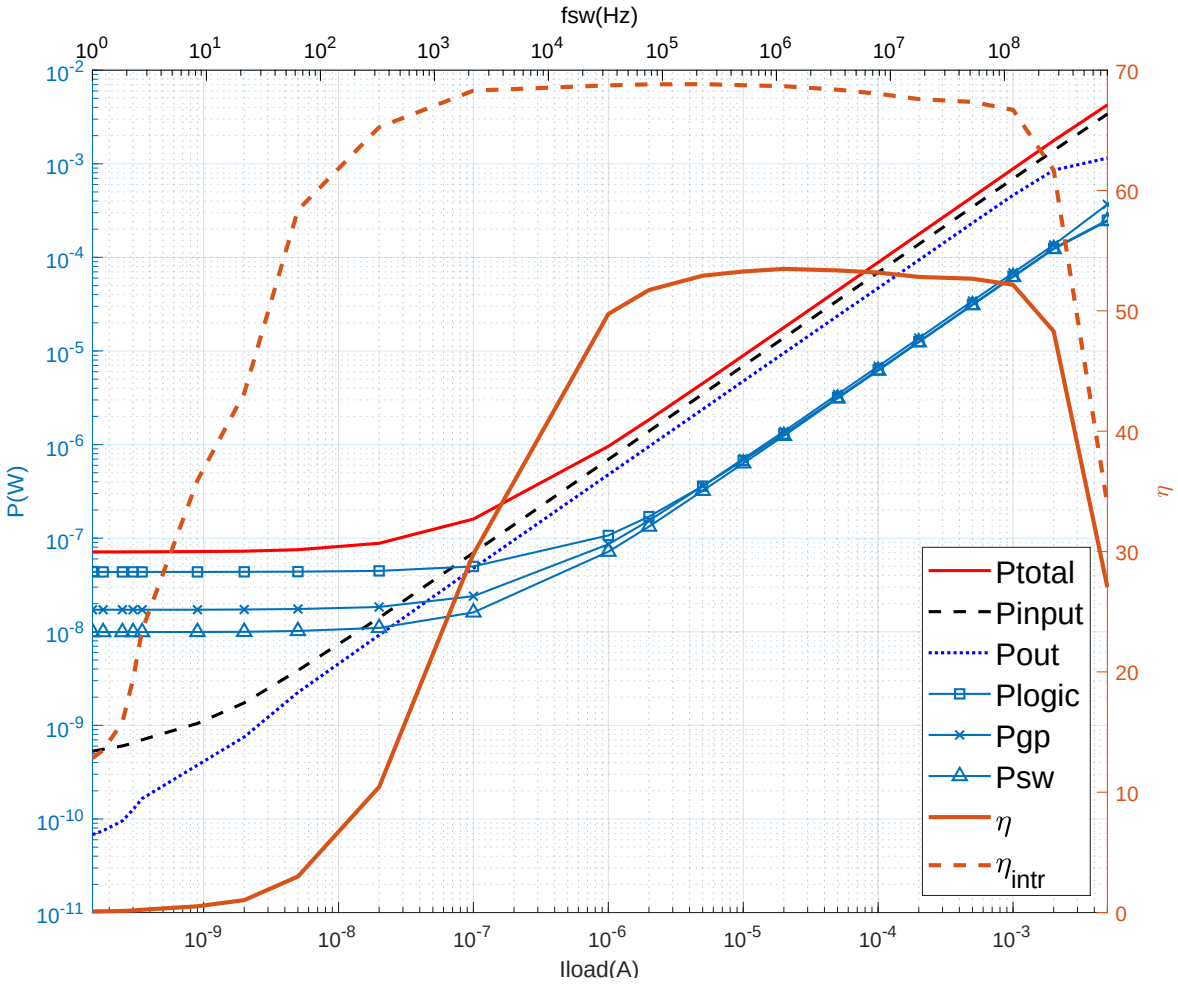

Figure 4.5.1: 12 Phases Open Loop System Intrinsic and Total Efficiency

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Chapter 5

Current Controlled Oscillator

5.1 Ring Oscillator

A Ring Oscillator is a CMOS-only composed electronic oscillator that occupies a very small area on-chip and can reach very high frequencies. It consists of a closed-loop of an odd number of inverters equal or greater than 3 [24].

$$A(s) = \frac{A_0}{\frac{s}{w_0}+1} \Rightarrow H_{ol}(s) = \frac{A_0^3}{(\frac{s}{w_0}+1)^3} \tag{5.1}$$

$$H_{cl}(s) = \frac{\frac{A_0^3}{(\frac{s}{w_0}+1)^3}}{1+\frac{A_0^3}{(\frac{s}{w_0}+1)^3}} = \frac{A_0^3}{\left(\frac{s}{w_0}+1\right)^3 + A_0^3} \tag{5.2}$$

$$s = \begin{cases} s_1 = -w_0(A_0+1) \\ s_{2,3} = w_0\left(A_0\frac{1\pm j\sqrt{3}}{2} - 1\right) \end{cases} \tag{5.3}$$

$$at\ A_0 = 2\ \exists\ limit\ cycle \Rightarrow s_{2,3} = \pm j\sqrt{3}w_0 \tag{5.4}$$

$$in\ general:\ f_{osc} = \pm jtg\left(\frac{2\pi}{n}\right)w_0 \tag{5.5}$$

$$where\ n\ is\ number\ of\ inverters \tag{5.6}$$

So the dynamic power of the inverter is:

$$P_D = nC_GV_{DD}^2 tg\left(\frac{2\pi}{n}\right)f_0 \leq C_GV_{DD}^2 w_o$$

So dynamic power is independent of the number of inverters as increasing the number of inverters reduces the frequency. But this frequency is fixed for a given Ring Oscillator.

5.2 Current Starved Ring Oscillator (CSRO)

A way to vary the oscillator frequency is to limit the current of the inverter as in a CSRO, see Fig.5.2.1. In Eq.5.8 we see the frequency and power for a CSRO.

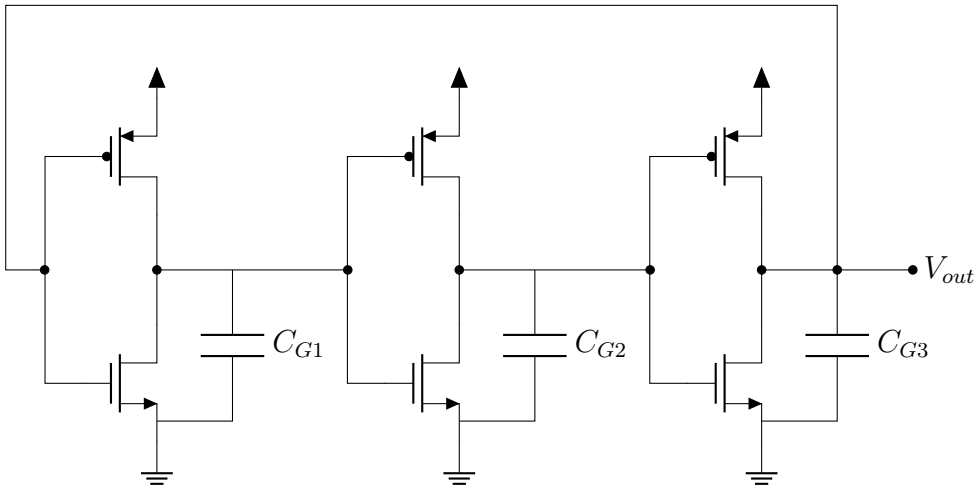


Figure 5.1.1: Simple 3 Inverter Ring Oscillator

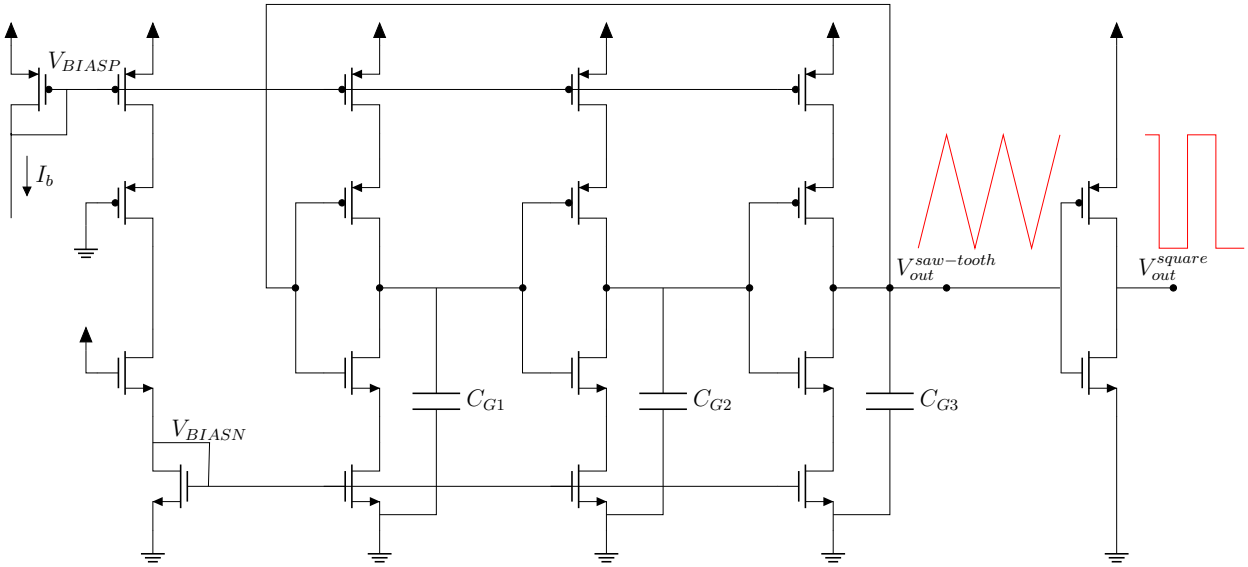


Figure 5.2.1: Current Starved Ring Oscillator

$$I_b = C_G V_{DD} f \times 2\#\ stages = C_G V_{DD} f \times 2n \tag{5.7}$$

$$f = \frac{I_b}{2nC_G V_{DD}} \Rightarrow I_b = 2nC_G V_{DD} f \Rightarrow P = 2C_G (nV_{DD})^2 f \tag{5.8}$$

But see also that Eq.5.1 is derived from operating at a DC point different from GND or V_{DD}, where both transistors are conducting, so a short circuit current is present, the power consumed by this current is called direct path power consumption. This current will be considerable at low frequencies, when the gate voltage takes values different from GND or V_{DD} during a considerable part of the period, in this case, the voltages will resemble a saw-tooth wave function. And total frequency will be less than that given by Eq.5.8.

$$f \leq \frac{I_b}{2nC_G V_{DD}} \tag{5.9}$$

$$f \leq \frac{P}{2C_G(nV_{DD})^2} \tag{5.10}$$

This would not be such a great problem as power would still scale with frequency as shown in Eq.5.10, but to obtain a square wave function voltage from that saw-tooth wave function voltage, the ring voltage will need to be passed through a non-current starved inverter, this inverter will exhibit great direct path power consumption. The result is a Ring with a total power that is not proportional to frequencies at low frequencies. This will greatly diminish the DC-DC efficiency as output power is proportional to frequency.

5.3 Cero Energy Per Cycle Ring Oscillator (CERO)

In order to keep the Converter efficiency from degrading oscillator power must scale with frequency. To do this for low frequencies direct path power consumption must be avoided, the only way to do this is to turn off one of the inverter's transistors before turning on the other, so as to never have a direct path from source to ground. Several strategies have been implemented to achieve this, [25], [26], [27], [28], [29], [30]. But in this system it was decided to use the work of [31], for its simplicity, low power consumption, proportional to frequency for all frequencies of operation, and extensive frequency range.

The oscillator schematic appears in Fig.5.3.1, it's composed of 3 stages of the delay cell, proposed in [31], in a loop, and two output buffers for the clock signal (CLK) and negated clock signal ($\overline{CLK}$). The delay cells use differential input and output signals, the signals are connected in the ring to invert the signal from one delay cell to the other.

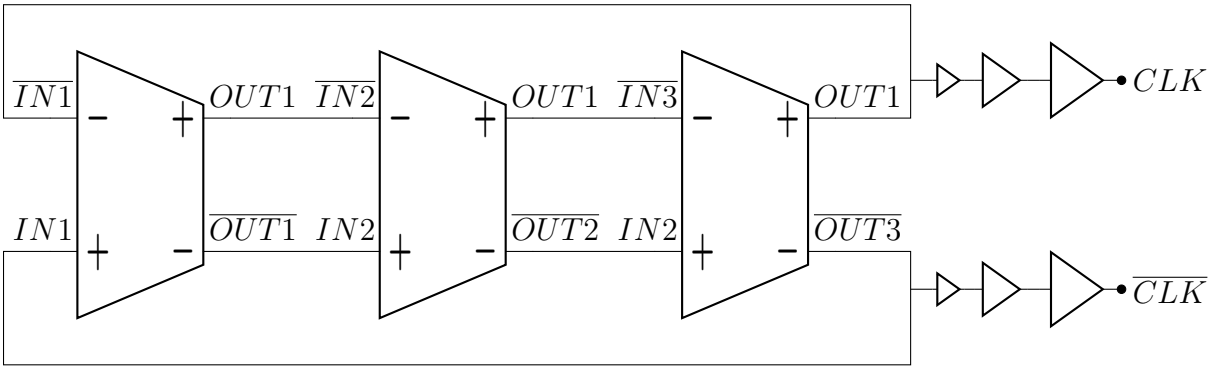


Figure 5.3.1: CERO Schematic.

The CERO cell is depicted in Fig.5.3.2. The cell is composed of two back-to-back inverters($M_{2A}, M_{3A}\&M_{2B}, M_{3B}$) in a latch configuration, in parallel with two Current Starved Inverters($M_{CPA}, M_{CNA}\&M_{CPB}, M_{CNB}$), with biased gate voltages V_{BIASN}, V_{BIASP},

which come from a current mirror as the one in 5.2.1. All of these inverters are stacked between two input inverters(M_{1A}, M_{4A}&M_{1B}, M_{4B}), while IN is high M_A transistors are isolated from V_{DD} and M_B transistors are isolated from ground, when IN is low the opposite happens.

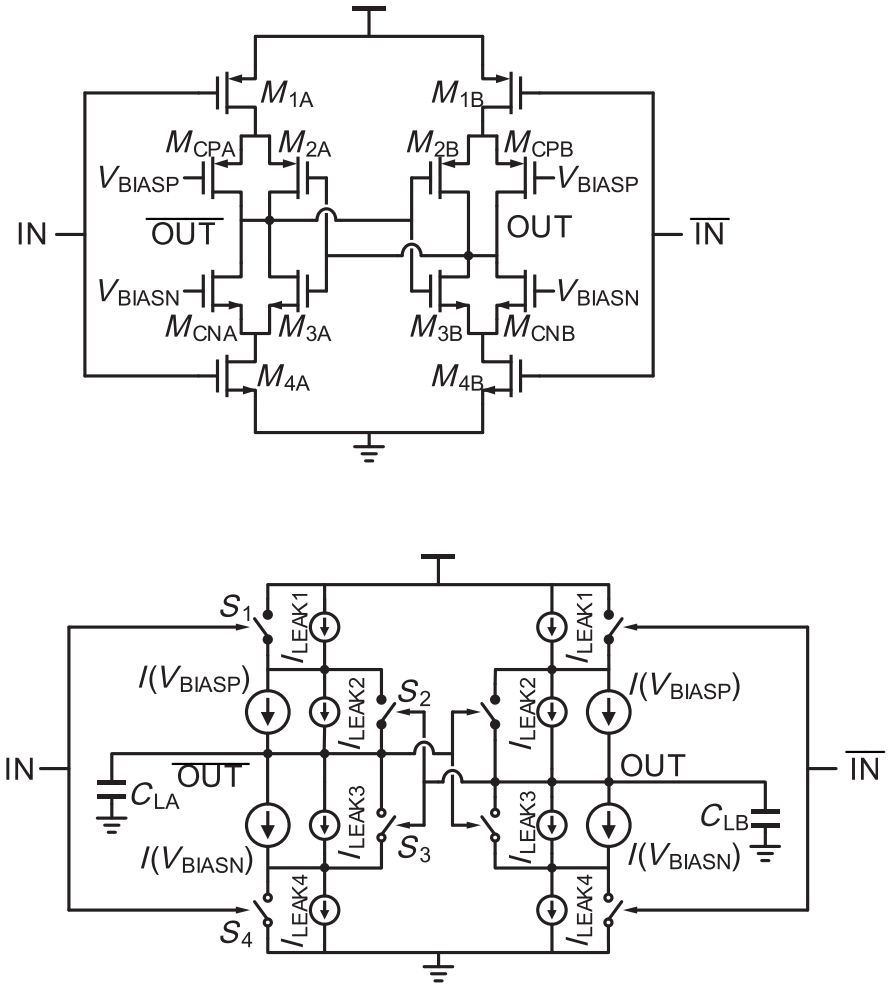


Figure 5.3.2: CERO Cell Schematic, image taken from [31].

The basic functionality exemplified for the first cell in Fig.5.3.3 and Fig.5.3.4 as follows: The latch inverters maintain the output while inputs don't change (Phase D). When inputs change (end Phase D beginning Phase A) only the path of Current Starved Inverter has both transistors turn on, so SCC is limited to their bias current. The voltages V_{BIASN}, V_{BIASP} are defined by the input current, the greater the input current the higher V_{BIASN}, the lower V_{BIASP} and the faster Phase A is.

After the inputs change (Phase A) the Current Starved Inverter begins to charge/discharge the output nodes slowly, when the output voltages approach threshold voltages the positive feedback of the latch type inverters makes the output commute fast (end Phase A beginning Phase B). Then Phase B and C are the same as Phases D and A with inverse voltages.

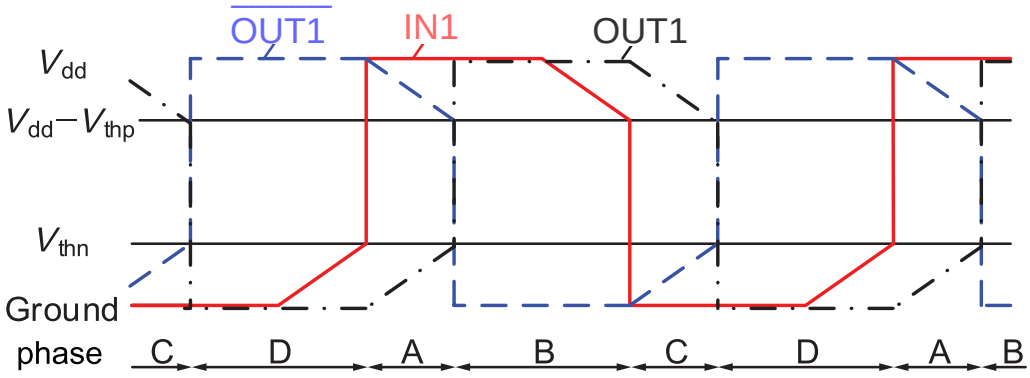


Figure 5.3.3: CERO Waveforms, image taken from [31].

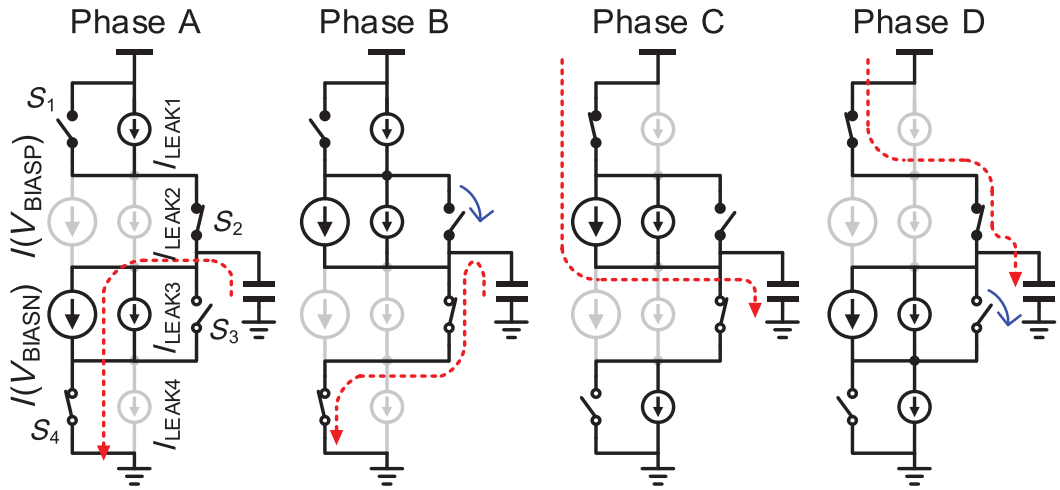


Figure 5.3.4: CERO Schematic by Phase, image taken from [31].

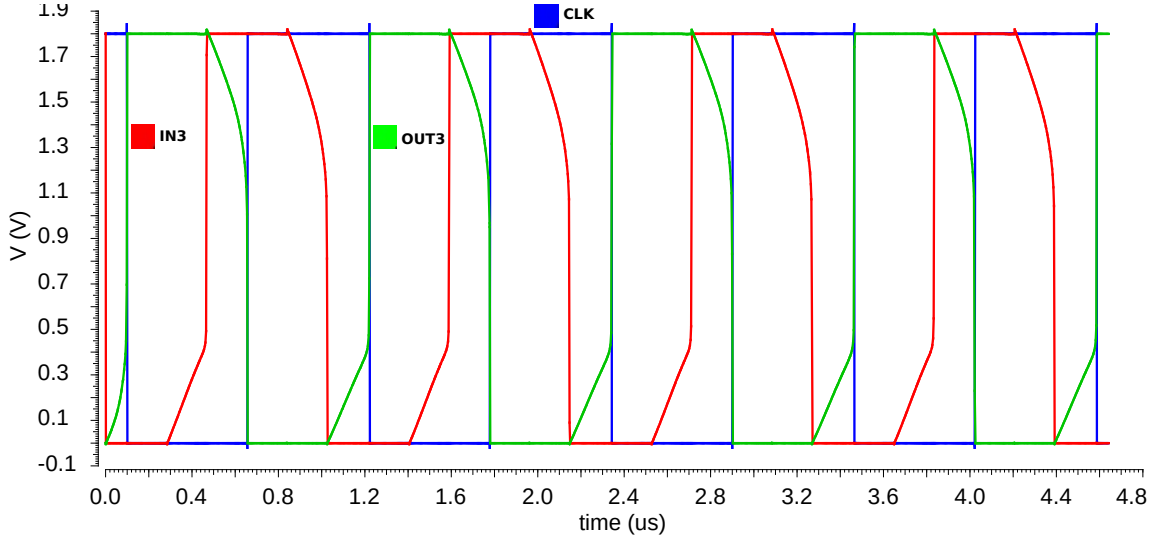


Figure 5.3.5: Waveforms for IN3(red), OUT3(green) and CLK(blue) at $f = 890kHz$

A simulation of power across frequency is shown in Fig.5.3.6, it can be seen that power is proportional to frequency for the entire range. The maximum frequency is obtained when $V_{BIASN} = V_{DD}, V_{BIASP} = 0$, obtaining maximum bias current and the Current Starved Inverter becomes regular inverters. Minimum frequency is obtained when $V_{BIASN} = 0, V_{BIASP} = V_{DD}$, in which case the Current Starved Inverters are always turned off, and the bias current is composed only of leakage currents. As the oscillator was designed with all minimum size transistors leakage currents are relevant so minimum frequency is in the order of hundreds of Hertz, for lower minimum frequencies smaller aspect ratios are needed; on the other side maximum frequencies can only improve slightly with other aspect ratios.

As we can see buffer power (yellow) is between one to half a decade below the total power (red), which is considerably less in low frequencies than for a CSRO, whose buffer power represents all the power consumption in low frequencies.

Corners are not graphed as simulation showed they don't present significant differences, either way the desired frequency is imposed in the oscillator by the feedback loop. Transistors where dimensioned with minimum width and length to minimize consumption. To obtain higher maximum frequencies or lower minimum frequencies, dimensions of transistors can be modified, but in the case of the converter it was not necessary.

$$\begin{cases} f_{min} = 680Hz & P_{min} = 680pW \\ f_{Max} = 235MHz & P_{min} = 150\mu W \end{cases} \tag{5.11}$$

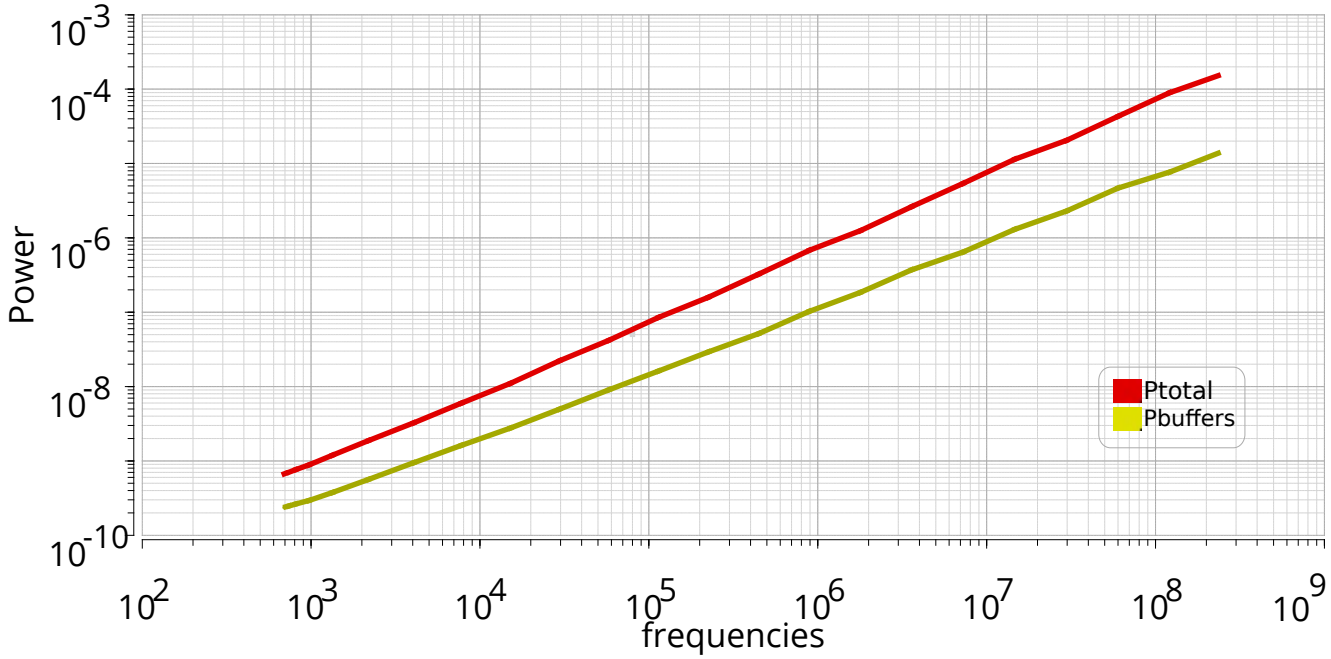


Figure 5.3.6: CERO Totaql Power (red) and Buffer Power (yellow) vs Frequency.

5.3.1 Overall Effect on System Efficiency

Fig.5.3.7 shows the simulated efficiency of the full Open Loop System including the CERO oscillator. The load current was sweeped from $10nA$ to $2.5mA$ with a switching frequency f_{sw} so as to maintain an output voltage of approximately $V_{out} = 0.5V$.

The efficiencies are marked in orange, with the dashed line representing the intrinsic efficiency of the capacitor ring only. The full orange line represents the total open-loop efficiency.

The other lines represent powers, being the highest red line the total power consumed by the converter P_{total}, the dashed black line is the input power Pin entering the capacitor ring, and the dotted blue line is the output power.

The clear blue lines with squares, stars, and triangles represent the Logic, Pulse Generator and Switches blocks power consumption respectively.

Finally, the violet line is the oscillator power consumption, this is the lowest of all the blocks for all frequencies, especially for low frequencies. This remarks the effects of the low frequencies, short circuit current cancellation, that the oscillator implements, that as it is not present in the Logic, Pulse Generator and Switches blocks their efficiencies are not proportional to frequencies for low frequencies/low loads.

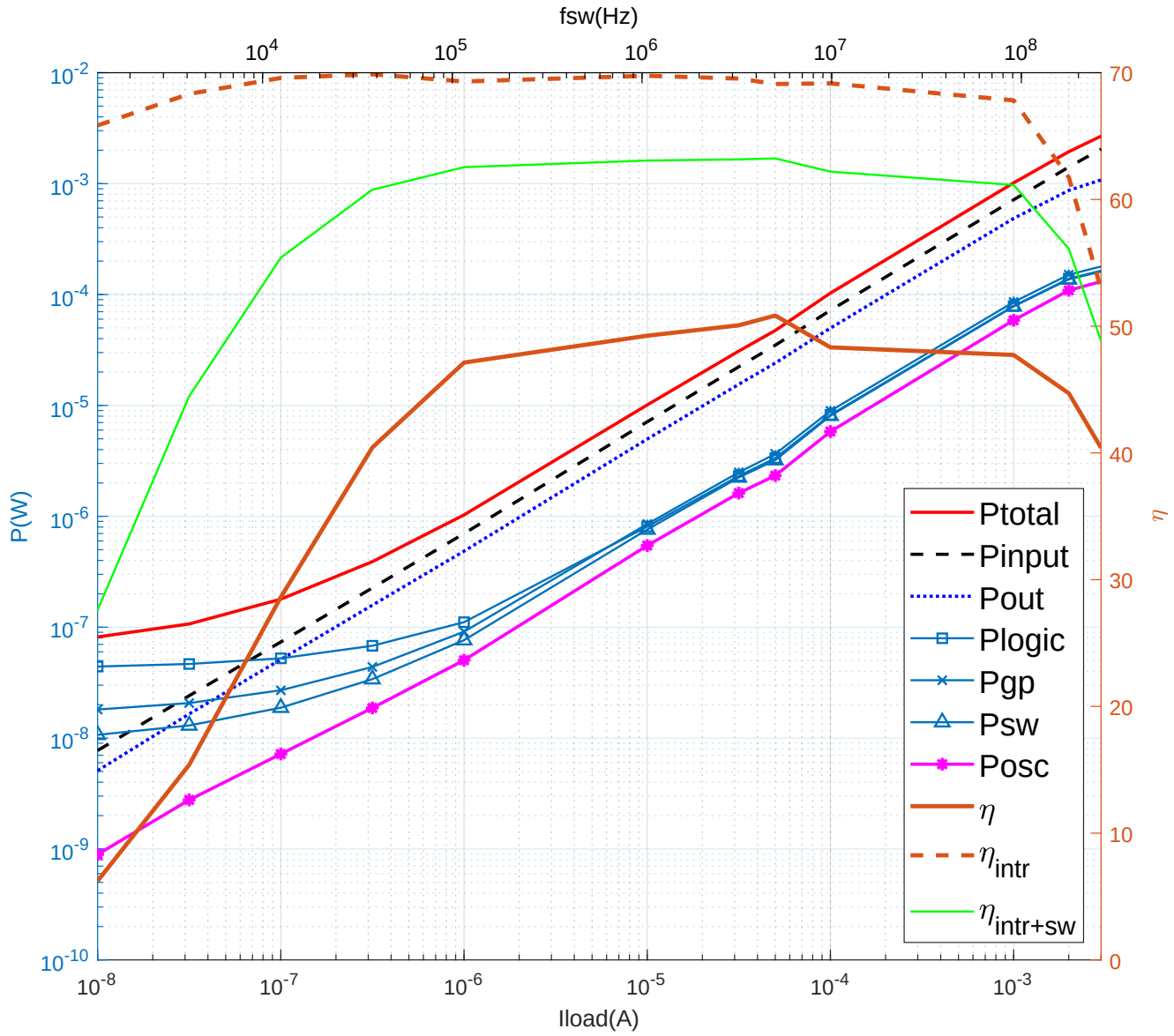


Figure 5.3.7: Open Loop System Efficiency including CERO oscillator.

Chapter 6

Non-Linear Loop

6.1 Comparator

Up until now, we have assumed the load is a constant current, in reality loads are at least partly compose of digital circuits, which consume current in short bursts with each clock edge. This can be seen as the load suddenly increasing dramatically, we can model this as a step function in the current load. For those phenomena you can add a non linear block in parallel to the linear block in order to compensate for this. For example we can add a comparator that measures the difference between output voltage and a reference voltage, if the output drops below the reference the comparator commutates and provokes a rapid response on the converter. For that we need a fast comparator, but a fast comparator will a higher static power consumption, therefore a trade-off presents itself between having a high power fast acting comparator or a lower power slower comparator.

To have a fast step response it is necessary to design a comparator as the one shown in Fig.6.1.1. The output voltage is controlled by the comparator's switching frequency, an increase in switching frequency induces an increase in the charge delivered to the output and therefore a rise in the output voltage. The switching frequency is determined by CCO, whose output frequency is linear with its input current, this current is the feedback variable used to perform control. The linear loop consists of a transconductor G_m and generates an output current proportional to the differential voltage $V_{REF} - V_{OUT}$, this loop functions continuously. Besides this linear control loop, a second control non-linear control loop is used to detect when the output drops below $V_{REF} - \delta V$. This voltage is sensed by a comparator and when it crosses zero the output voltage of the comparator commutes and a transistor is turned on so that the feedback current increases substantially provoking a sharp increase in switching frequency and therefore in charge delivered to the output.

The Comparator Desired Specs are the following:

- As low static power as possible, ideally in the order of tens of nano Ampers.
- Conmutation speed high enough so that if the input increases linearly, the output commutes before the input diverges more than $20mV$ from $VREF$. Then if the input varies as $\frac{\delta v_{in}}{\delta t}$ and the comparator has a delay of T_D, the equation :

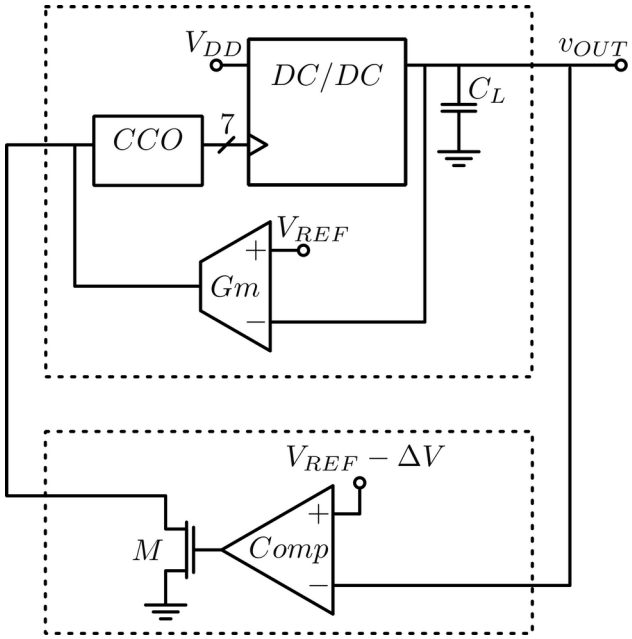


Figure 6.1.1: Block Diagram of Monolithic DC-DC Converter with double control loop.

$\frac{\delta v_{in}}{\delta t} T_D \leq 20mV$ must be met. For example if the V_{out} varies $1V/\mu s$, which corresponds to $I_L = 1mA$ load discharging a $C_L = 1nF$ load, we have that the Comparator Delay must be: $T_D \leq 20ns$.

- The load Capacitance is negligible, the actual load is a minimum inverter whose gate capacitance is $C_{gg} \leq 1fF$, this is followed by other inverters, Fig.6.2.1, and after them transistor M from Fig.6.1.1. But the real load capacitance is dominated by parasitic capacitance from the comparator's own transistors.

- Rail to Rail output as the output must be digital.

- Technology XFAB XT018 HV SOI CMOS (180 nm).
- $V_{dd} = 1.8V$.

To see how feasible are this specs, let us see what current is needed to charge $1fF$ from $0V$ to $1.8V$ at a speed that guarantees the output goes from 0 to V_{DD} before the input diverges more than $50mV$ from $VREF$, this implies a speed $1.8/0,05 = 36$ faster than the input. If the input varies $1V/us$ this means a speed of $36mV/\mu s$ and a current of $I = C_L \delta V_{out}/\delta t = (1fF)(36V/us) = 36nA$. Then we have a lower bound for the bias current $I_{bias} \geq 36nA$, this limit is only met if from the point where $V_{in} = V_{ref}$ all bias current is applied to the output, case that will never be met with a differential pair as the

pair will not be complete unbalanced from the start. Using Adaptive Bias Techniques [32] one could theoretically have lower standby bias currents, but simulations show that the delay imposed by the Adaptive Bias Block makes this strategy unviable.

6.2 Proposed Architecture: Zero Cross Comparator

Proposed Architecture is shown in Fig.6.2.1, this comparator is used to detect Zero Voltage Crosses. Although most continuous-time comparators use differential pairs, they have the disadvantage that full bias current is only obtained after the pair is fully unbalanced, this makes it slow to respond. A symmetrical OTA not only has this problem but also the charge time of nodes from the current mirrors makes the OTA slow.
The desired case is to have a minimum number of nodes that move with the input signal and need to be charged, this will mean a minimum number of transistors, which makes complex architectures unviable. In this way, the Zero Cross Comparator is ideal as all nodes are constant except the input and output. In place of a differential pair, two opposed mirrors are used, where a change in Vin provokes that the copy of the n-mirror is different from the p-mirror, and the output changes rapidly.
The main drawback from this comparator is that the input is an n-transistor source, this

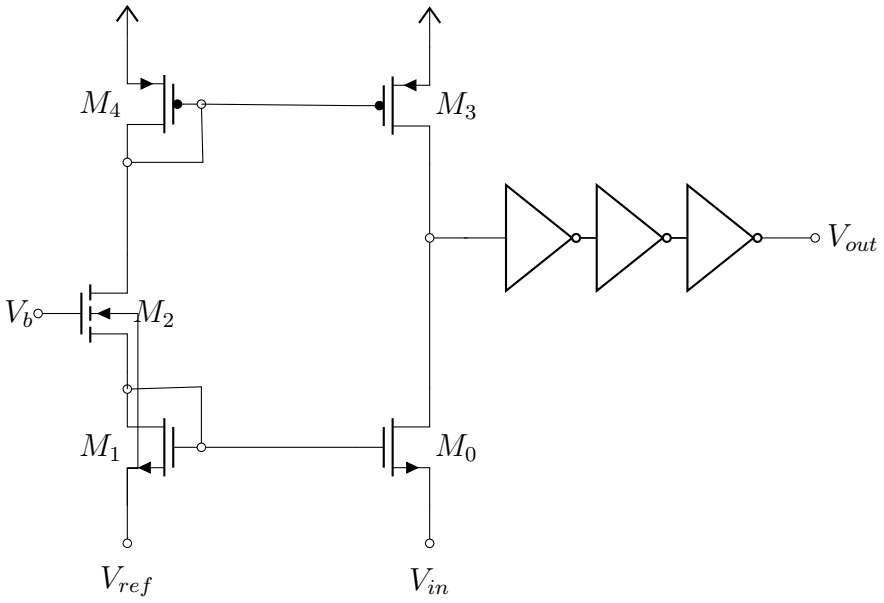


Figure 6.2.1: Proposed Comparator.

creates several problems:

- The input as well as V_{REF} must be able to draw the bias current
- The drain of transistor M_0, which is the output, can't drop below $V_{in}+V_{ds_{sat}} \underset{WI}{\approx} V_{in}$, equal to V_{REF} in equilibrium. The inverters correct this as a digital output is needed, however, this implies that in stand-by the inverter input can be $V_{ref} \in [0, V_{dd}]$, this

will mean great short circuit current power. To mitigate this the inverter is *Current Starved* and therefore slower, and short circuit power will still be a considerable part of total power.

- *ICMR* is severally limited. As the output is always between [V_{REF} and V_{DD} then if $V_{ref} > V_{dd}/2$ the inverters will never commute. this implies $ICMR_{max} = [0, V_{dd}/2]$, but as will be seen, in practice the $ICMR$ is even lower. This implies that the comparator can only be used in a 1/3 conversion ratio.

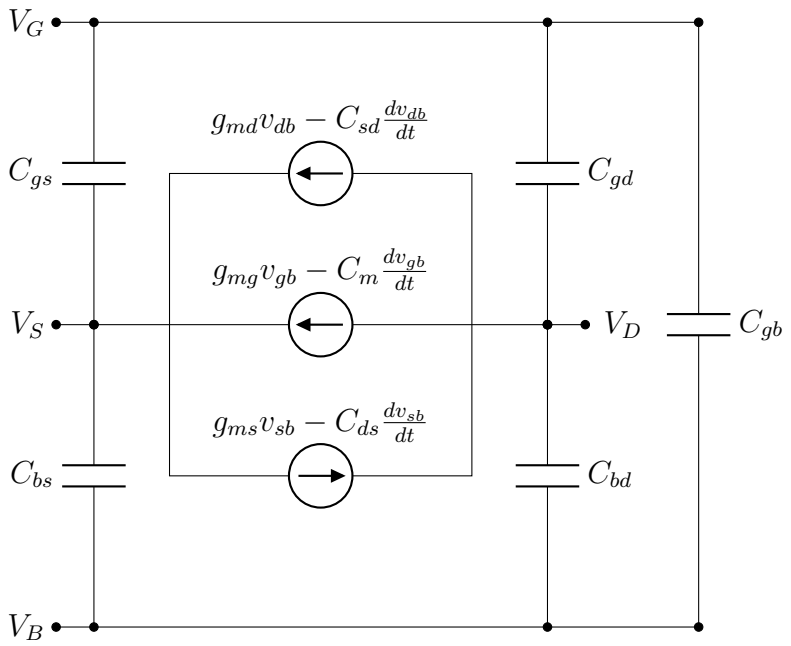


Figure 6.2.2: 4 Terminal Mosfet Small Signal Model [33].

6.3 Modeling

The behavior of the system is determined by transistor M_0, therefore it must be analyzed in detail. In Fig.6.2.2 the 4 Terminal Mosfet Model is presented, in our case, Bulk and Sourced are short-circuited so the model is as shown in Fig.6.3.1, where we assume the impedance seen by the gate of M_0 is negligible. The load connected to the drain of M_0 is the parallel of the gate capacitance of a minimum inverter $C_{G_{inv}}$, the drain capacitance of $M_3 : C_{dd_p}$ and the output resistance of $M_3 : r_{op}$. The ouput resistance of M_0 is included in the current source i_d

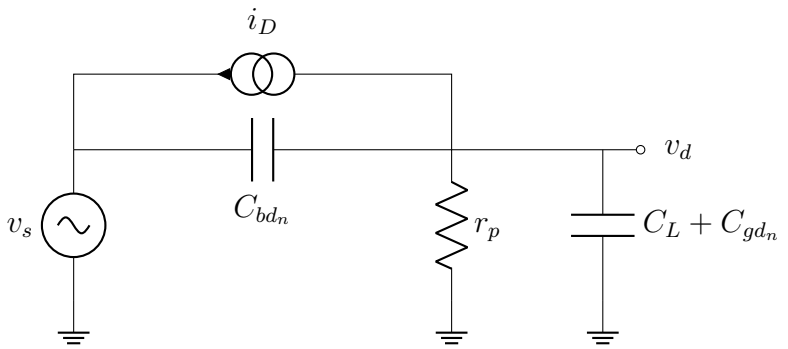


Figure 6.3.1: 3 Terminal Small Signal Model

$$\begin{cases} i_D = g_{md}(v_{out} - v_{in}) + C_{sd_n}\frac{\delta(v_{out}-v_{in})}{\delta t} - g_{mg}v_{in} + (C_{dg_n} - C_{gd_n})\frac{\delta v_{out}}{\delta t} \\ C_L = C_{G_{inv}} + C_{ov_n}W_n + C_{ov_p}W_p + C_{j_n}X_nW_n + C_{j_p}X_pW_p + \\ \qquad 2(C_{jswn}(X_n + W_n) + C_{jswp}(X_p + W_p)) + C_{dd_p} \\ C_{dd_p} = C_{sd_p} + C_{gd_p} + C_{bd_p} \end{cases} \tag{6.1}$$

Then assuming null initial conditions we can find the transfer function v_d/v_s:

$$\frac{V_d(s)}{V_s(s)} = G\frac{1 + s/z}{1 + s/p} \tag{6.2}$$

$$G = \frac{g_{md} + g_{mg}}{g_{md} + 1/r_p} \qquad z = \frac{g_{md} + g_{mg}}{C_{bd_n} + C_{sd_n}} \qquad p = \frac{g_{md} + 1/r_p}{C_{bd_n} + C_L + C_{sd_n} + C_{dg_n}} \tag{6.3}$$

As the Comparator's input is the output of a DC-DC Converter, it will decrease at a constant rate, proportional to the Converter load current, which will form the traditional saw-tooth signal of the ripple voltage:

$$V_{DC-DC_{out}} = v_s = -kt$$

y $V_s(s) = -k/s^2$ where $k = I_L/C_{DC-DC}$ and C_{DC-DC} is the output capacitance of the Converter. Then the Comparator output takes the form:

$$\begin{cases} V_{out}(s) = -\frac{k}{s^2}G\frac{1+s/z}{1+s/p} = -kG\left[\frac{1}{s^2} + \frac{1/z-1/p}{s}\frac{1/p-1/z}{p+s}\right] \\ v_{out}(t) = -kG\left[t + (1/z - 1/p)(1 - e^{-pt})\right] \end{cases} \tag{6.4}$$

The fastest output change is obtained by maximizing $G \times p = BW$. The transconductance equations are in Ec.6.5, obtained from the ***ACM Model*** developed in [33].

$$\begin{cases} g_{ms(d)} = u_n\frac{W_n}{L_n}nC_{ox}U_Tq_{s(d)} \\ g_{mg} = \frac{g_{ms}-g_{md}}{n} \\ q_{s(d)} = \frac{-Q_{s(d)}}{nC_{ox}V_t} \end{cases} \tag{6.5}$$

Then we have that:

$$G \times p = \frac{u_n \frac{W_n}{L_n} C_{ox} U_T (q_s + q_d(n-1))}{C_{bd_n} + C_L + C_{sd_n} + C_{dg_n}} \tag{6.6}$$

However, in order to take into account the power it is more reasonable to maximize $\frac{G \times p}{ID}$.

$$\frac{G \times p}{ID} = \frac{2(q_s + q_d(n-1))}{nU_T(q_s^2 - q_d^2 + 2(q_s - q_d))} \frac{1}{C_{bd_n} + C_L + C_{sd_n} + C_{dg_n}} \tag{6.7}$$

It is important to differentiate two cases, one is when v_{in} is below V_{REF}, in this case the output voltage follows the input voltage $V_{out} = v_d \approx v_{in}$. In this case M_0 is not saturated, q_s has values in order of q_d and the Capacitance that dominate the load are the intrinsic capacitance of $M_0 : C_{bd}, C_{sd}, C_{dg}$. These are the conditions when the output goes from low to high.

The other case is when $v_{in} > V_{ref}$, then the output voltage is high and $v_d \approx V_{dd}$. In this case $q_s \gg q_d$, and now the capacitance that dominates the load are the intrinsic capacitance of p-transistor $M_3 : C_{dd_p} = C_{sd_p} + C_{gd_p} + C_{bd_p}$ as this is the one not saturated. These are the conditions when the output goes from high to low.

In both cases, we have neglected the extrinsic capacitance and the inverter input capacitance in front of the intrinsic capacitance of a non-saturated Mosfet.

$$\begin{cases} \frac{G \times p}{ID} = \frac{2(q_s + q_d(n-1))}{nU_T(q_s^2 - q_d^2 + 2(q_s - q_d))} \frac{1}{C_{bd_n} + C_{sd_n} + C_{dg_n}} & v_{out} : 0 \to 1, \cancel{q_s \gg q_d}, C_{dd_n} \gg C_{dd_p} \\ \frac{G \times p}{ID} = \frac{2}{nU_T(q_s + 2)} \frac{1}{C_{sd_p} + C_{gd_p} + C_{bd_p}} & v_{out} : 1 \to 0, q_s \gg q_d, C_{dd_n} \ll C_{dd_p} \end{cases} \tag{6.8}$$

In the first case, neither $q_s \gg q_d$ or $q_s \ll q_d$ inversion levels maximize the $\frac{G \times p}{I_D}$. Capacitance are all proportional to $W_n \times L_n$, as they are proportional to C_{ox} when extrinsic capacitance are neglected. Therefore, inversions levels are ignored and minimum sizes are chosen for M_0. In the second case a weak inversion level is preferable and also all capacitance are proportional to $W_p \times L_p$, as bias currents will be quite low in this case also minimum sizes are chosen M_3.

A bias current of $I_{Bias} = 50nA$ is proposed, striving for low power.

In the Fig.6.3.2 we can see a transition from high to low and a transition from low to high, and the drain capacitance of M_0 and M_3 vs the total load capacitance $Ctotal$ (which includes intrinsic capacitance as well as the inverter capacitance) are shown.
Here we see that the intrinsic capacitance of M_3 dominates the transition from high to low and the intrinsic capacitance of M_0 dominates the transition from low to high. The main difference between these and the total capacitance is the inverter capacitance which is $C_{G_{inv}} \approx 0.635fF$.

In this case, the Comparator Fall Delay is $T_{Ddown} = 100ns$ and a Rise Delay $T_{Dup} = 76ns$, for an input signal which varies as $1V/\mu s$, as we have already seen an acceptable Delay for this input would be only $20ns$, so we are falling short of the mark. The voltage

differences between V_{in} and V_{REF} at the moment of commutation are $\delta V_{down} = 100mV$ and $\delta V_{up} = 75mV$. the objective was $\Delta V \leq 20mV$.

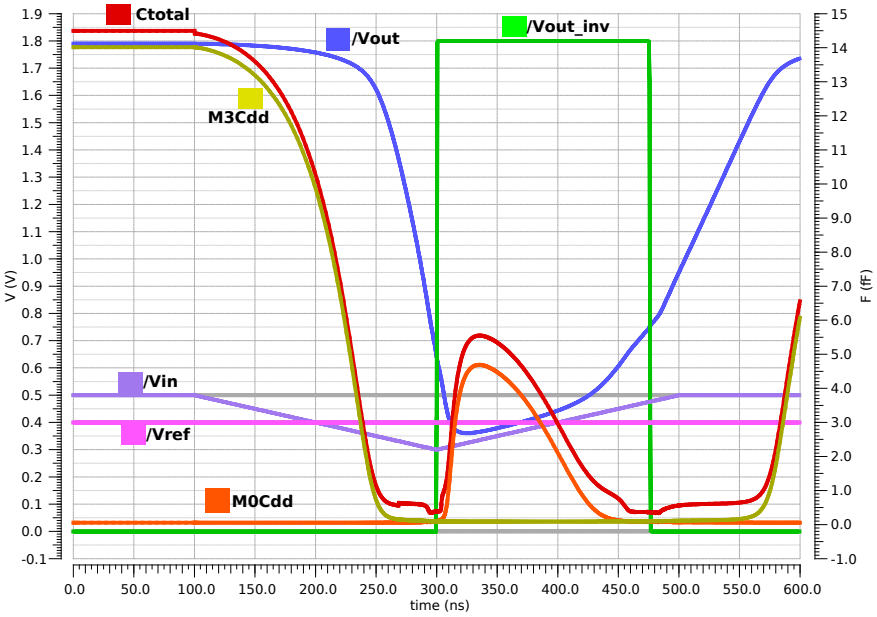


Figure 6.3.2: Transition of Comparator with n-transition capacitance M_0C_{dd}((orange) vs p-transistor capacitance M_3C_{dd} (yellow) and the total capacitance C_{total}(red).

The main problem with our model is that the transistor M_0 passes through all inversion levels in a transition, as shown in Fig.6.3.3. The model presented in Ec.6.2 is only valid when the capacitances do not vary with the output.
In Fig.6.3.4 the curves are shown again with markers showing the instant when the output changes behavior. From the point where V_{in} and V_{ref} cross, marked by the pointed vertical line, up to where the circular marker is, when the output slope changes, the intrinsic capacitance are changing. From the circular marker up to when the Comparator commutes (end of transition), the intrinsic capacitance and the total capacitance are constant.

Finally, let us see once again the transition showed in Fig.6.3.5, now with the Drain and Source of M_0 normalized levels of inversion, obtained from the simulator based on **BSIM4** models.
As we can see the levels of inversion are close to one in the Source, therefore transistors are in mid-inversion in Source. The Drain is also in mid-inversion when output is low and in weak inversion when output is high and there is saturation. As q_S is never much greater or lower than 1 we can't find an analytical expression for the inversion levels as a function of voltages from Eq.6.9. This, therefore, makes it difficult to find an analytical expression between output-input voltages.

$$\frac{V_P - V_{S(D)}}{U_T} = q_{s(d)} - 1 + ln(q_{s(d)}) \tag{6.9}$$

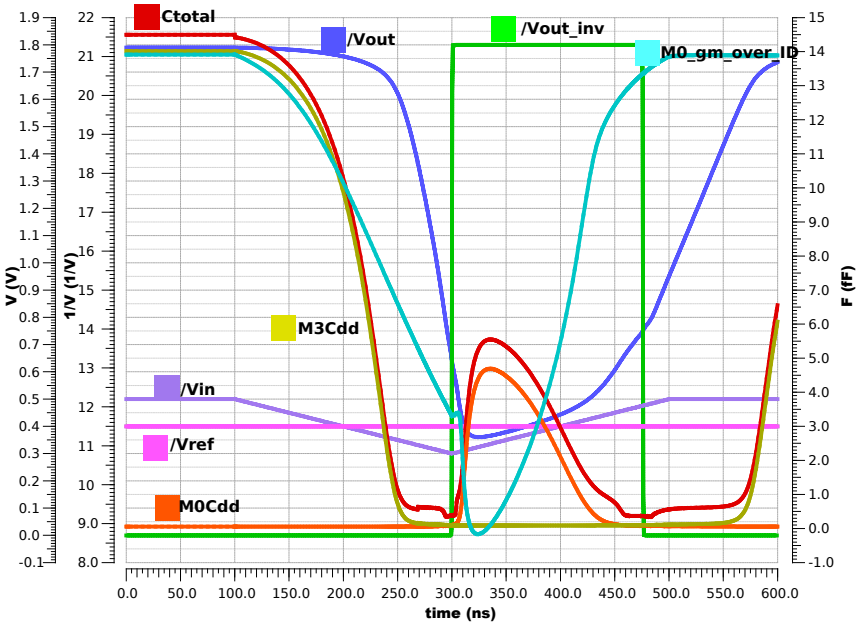


Figure 6.3.3: Comparator Transition with $\frac{gm}{ID}_{M_0}$ (sky-blue).

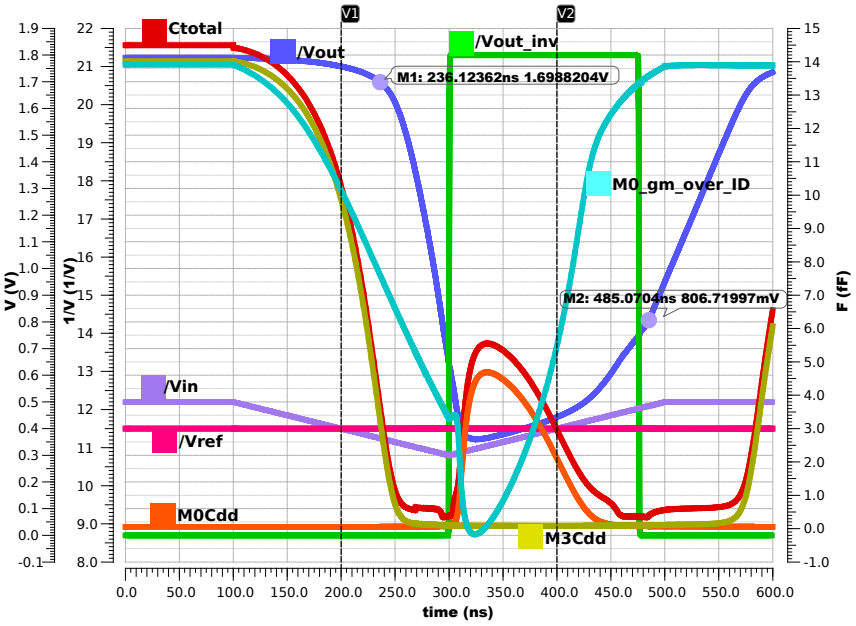


Figure 6.3.4: Comparators Transitions, markers point where capacitance behavior changes from constant to variable.

6.4 Results

In Fig.6.4.1 we see the Comparator Topology and in Fig.6.4.2 the Comparator with the inverters. The first two inverters are *Current Starved* as the output low of the Comparator is V_{REF}, this would provoke great short circuit currents in the first inverter if it was not *Current Starved*. The bias current of the Comparator and the bias current of the inverter

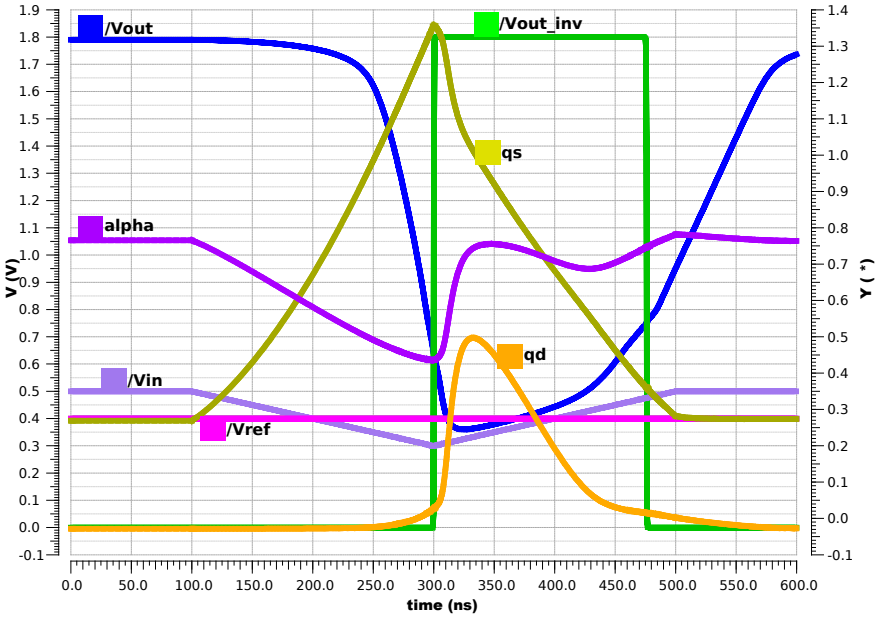


Figure 6.3.5: Transitions with inversion levels of M_0 : q_s, q_d and $\alpha = \frac{q_d+1}{q_s+1}$.

are regulated separately.

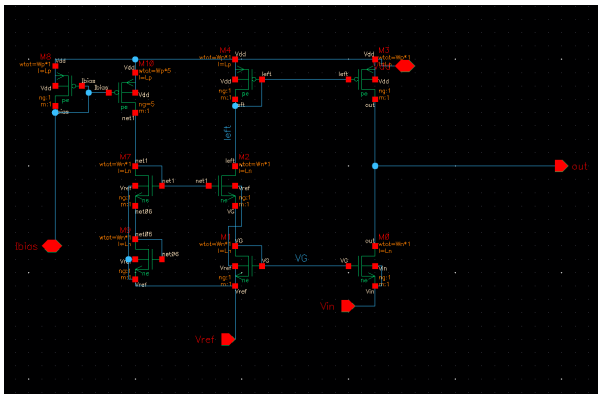


Figure 6.4.1: Comparator.

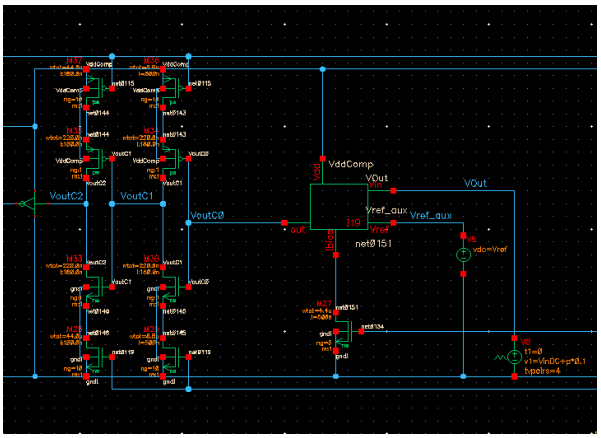


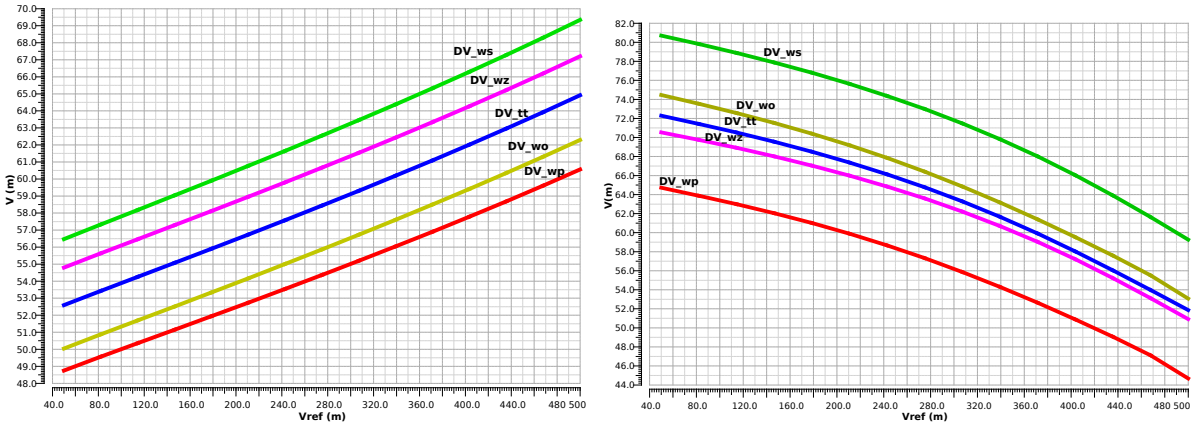
Figure 6.4.2: Conparator and Inverters.

In Fig.6.4.3 are shown the corners of Voltage Error, the difference between input and reference at the time of commutation. And in Fig.6.4.4 corners of Commutation Delay, which the time it takes to commutate after input crosses the reference. Fig.6.4.5 shows static and dynamic Power for tt and wp corners. Table 6.1 describe the corner types. All curves are for triangular input that goes from $V_{REF} + 100mV$ to $V_{REF} - 100mV$ with a slew rate of $1V/\mu s$. For each curve a sweep of $V_{REF} \in [0, 0.5]V$ was done, according to the Comparator $ICMR$. Theoretically, the $ICMR$ could go up to $V_{dd}/2 - V_{DSsat}^{M_0}$, as beyond this the inverter would not commute. Assuming weak inversion $V_{DSsat}^{M_0} \approx 100mV$) this gives as a $ICMR \in [0, 800mV]$. However, simulations show that inverters do not always

commute for voltages of $V_{ref} \geq 0.5V$.

Corner Type	**nMos**	**pMos**
tt:typical	normal	normal
wp:worst power	fast	fast
ws:worst speed	slow	slow
wo:worst one	fast	slow
wz:worst zero	slow	fast

Table 6.1: Corner Types.



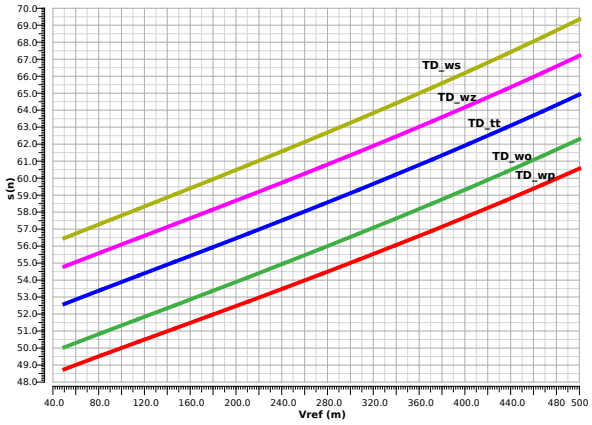
Commutation of high to low. Commutation of low to high.

Figure 6.4.3: Voltage difference between V_{in} y V_{ref} at commutation instant.

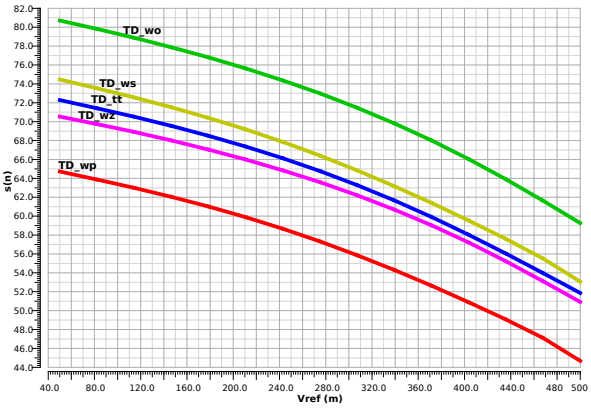
Something noteworthy is that the Delay Times and Error Voltages increase with V_{REF} when the comparator goes from high to low but decreases when the Comparator goes from low to high. This is because when going from high to low the drain voltage $v_d = v_{out}$ is Vdd before commuting, the transistor is saturated and the higher V_{REF} is the lower the V_{DS} voltage will be. On the other side in a low to high commutation $v_d \approx v_s = v_{in}$ and the time Delay is dominated by how big is the difference between the V_{REF} voltage and $V_{dd}/2$, where the commutation occurs, this difference decreases as V_{REF} increases.

In Fig.6.4.6 the Input Offset of the Comparator is plotted.

The step response was also simulated for a step from $V_{ref} - V_{step}/2$ to $V_{ref} + V_{step}/2$ in Fig.6.4.7, to observe behavior of more drastic change around the reference. In Fig.6.4.8 we see de Delays obtained for different levels of reference, all with $V_{step} = 50mV$. Note that not all curves from Fig.6.4.8 reach all values of V_{REF}, this is because in this case, the Comparator didn't commute, these cases correspond to wp and wz corners, which mean a less conductive nMos. As the signal is in practice compared by n-transistor M_0, in these corners the Comparator is less sensible.

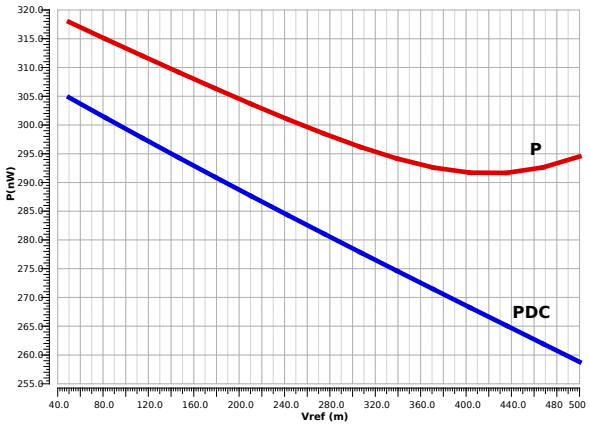


High to low commutation.

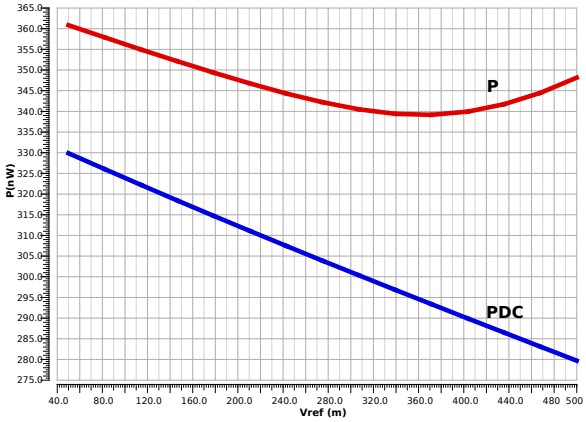


Low to high commutation.

Figure 6.4.4: Delay time T_D for each corner with input slope $1V/\mu s$.



Power for corner tt.



Power for corner wp.

Figure 6.4.5: Static and Dynamic(1MHz) Power.

Although this is the fastest continuous-time Comparator with low power demand, it does not meet the specs required in power or speed, besides having great ICMR limitations. The desired Delay Time was $T_D \leq 20ns$, but as seen in Fig.6.4.4 the Delay can be up to $80ns$, while the desired Voltage Error was $\delta V \leq 20mV$ can also be up to $80mV$.

It was decided not to increase the bias currents as power is already high. The desired dynamic power was $P \leq 100nW$, in Fig.6.4.5 we see power up to $300nW$. It is doubtful better power or speed can be obtained in this technology, besides increasing bias currents does not improve speed proportionally.

Better modeling of the intrinsic capacitance behavior at commutation is needed to obtain a model for the Comparator Delays.

It is also necessary to study the offset sources and modeling. The simulations pre-

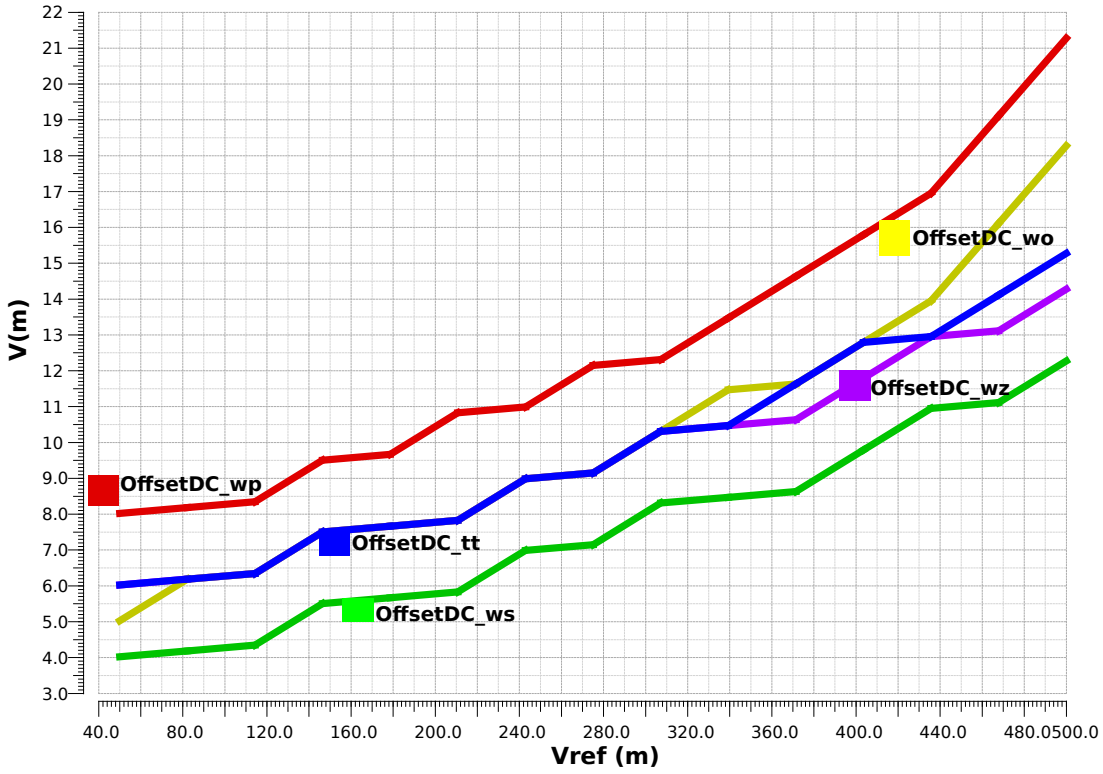


Figure 6.4.6: Input Offset from Comparator Histeresis Sweep.

sented do not take into account transistor mismatch, however, the Comparator already has an Offset of up to $20mV$.

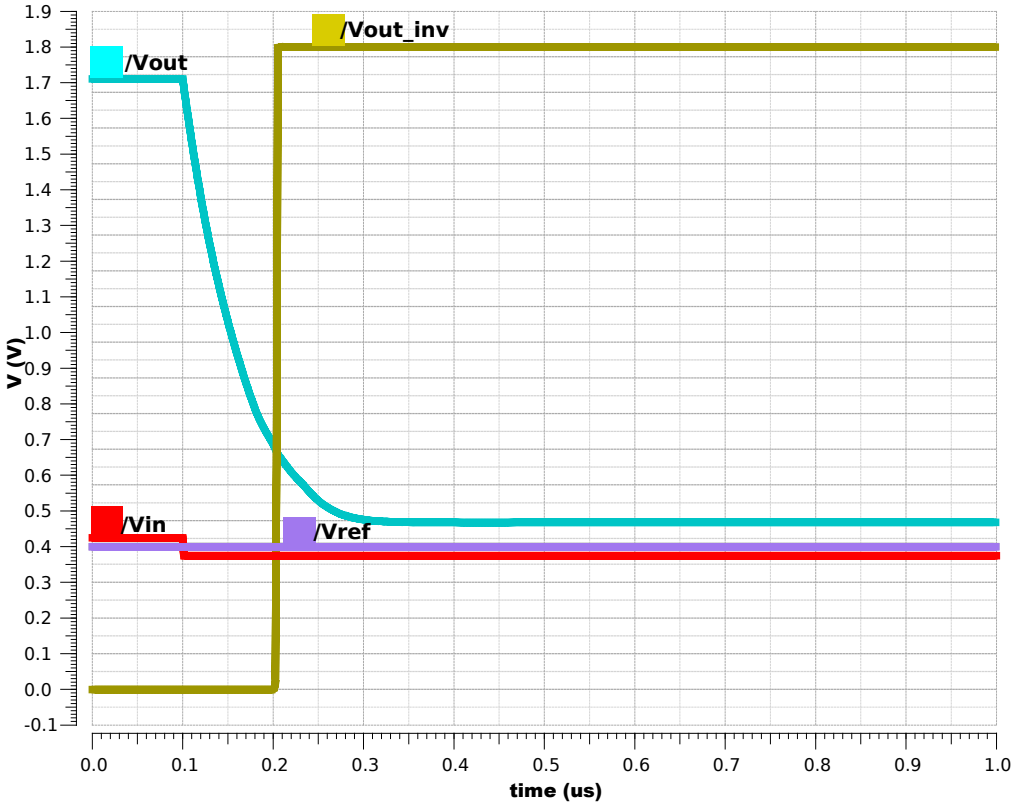
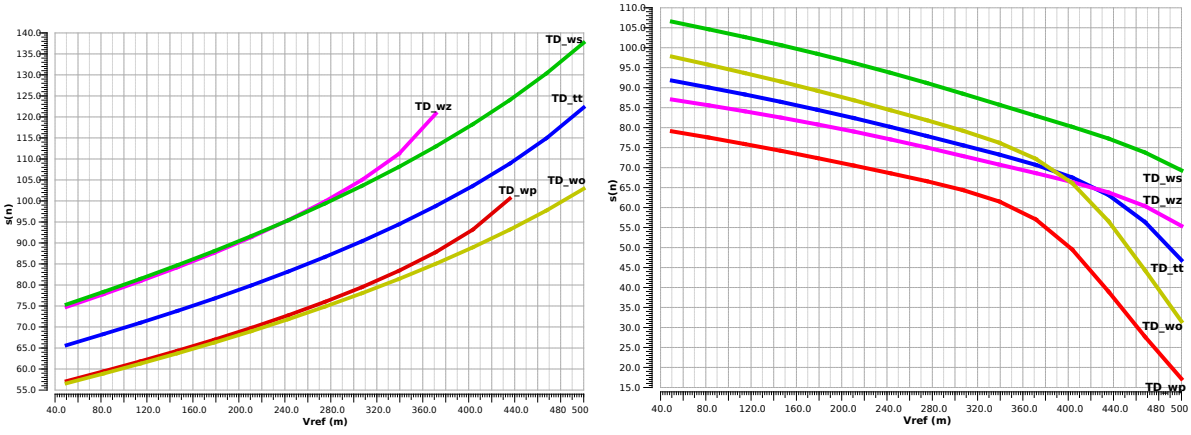


Figure 6.4.7: Step Response with Step $V_{step} = 50mV$ and $V_{ref} = 0.4V$.



High to low commutation. Low to High commutation.

Figure 6.4.8: Delay T_D for each corner, input step amplitude $25mV$.

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Chapter 7

Linear Loop

7.1 Model

According to Fig.6.1.1 we will model the Open Loop Converter as a non linear system: $\Psi(f_{sw}, I_L) = V_{out}$, whose inputs are the load current I_L and switching frequency f_{sw}, and the output is the output voltage V_{out}, as shown in Fig.7.1.1. Also in Fig.7.1.1 it is added a first order feed-back loop G, of gain k and pole p.

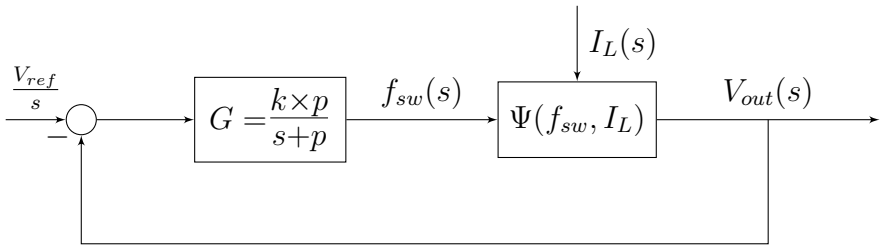

Figure 7.1.1: Linear Loop Block Diagram

As seen in 2.4, we can model the $\Psi(f_{sw}, I_L) = V_{out}$ Converter, operating in Slow Switching Limit (SSL), as an RC system like in Fig.7.1.2.

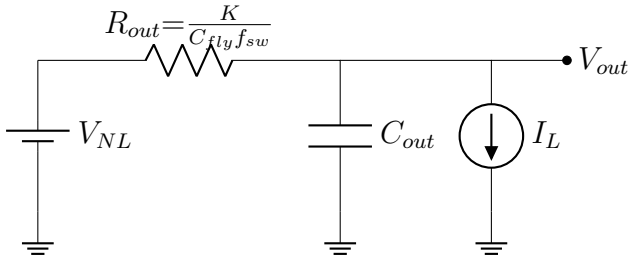

Figure 7.1.2: Output Resistence Promediated Model

Therefor we can write V_{out} as V_{NL} minus the voltage drop in R_{out}:

$$V_{out} = V_{NL} - R_{out} I_{out} = V_{NL} - R_{out}\left[C_{out}\dot{V_{out}} + I_L\right] \tag{7.1}$$

$$V_{out} = V_{NL} - \frac{K}{C_{fly} f_{sw}}\left(C_{out}\dot{V_{out}} + I_L(t)\right) \tag{7.2}$$

$$\tag{7.3}$$

Then we obtain the time derivative of V_{out} as:

$$\dot{V_{out}} = (V_{NL} - V_{out})\frac{f_{sw} C_{fly}}{K C_{out}} - \frac{I_L}{C_{out}} = g\left(V_{out}, f_{sw}, I_L\right) \tag{7.4}$$

We can analyze the problem as a function of the operating point $(\mathbf{V_{out}}, \mathbf{F_{sw}})$. Linealizing the equation around the operation point, and remembering that $\Delta V = (V_{NL} - V_{out})/2$:

$$\dot{V_{out}} = \frac{C_{fly}}{K C_{out}}\left[\Delta V/2 f_{sw} - \mathbf{F_{sw}} V_{out}\right] - \frac{I_L}{C_{out}} \tag{7.5}$$

Using the equation of the feed-back loop:

$$\frac{f_{sw}}{V_{ref} - V_{out}} = \frac{k.p}{s + p}$$

we can now write the state equations of the systems, with state variables V_{out} and f_{sw} :

$$\begin{cases} \dot{V_{out}} = \frac{C_{fly}}{K C_{out}}\left[\Delta V/2 f_{sw} - \mathbf{F_{sw}} V_{out}\right] - \frac{I_L}{C_{out}} \\ \dot{f_{sw}} = (V_{ref} - V_{out})\, kp - f_{sw} p \end{cases} \tag{7.6}$$

The complete lineal system matrix and vectors are shown in Eq.7.7 and 7.7.

$$\begin{cases} X = \begin{bmatrix} V_{out} \\ f_{sw} \end{bmatrix} & U = \begin{bmatrix} I_L \\ V_{ref} \end{bmatrix} \\ A = \begin{bmatrix} -\frac{\mathbf{F_{sw}} C_{fly}}{K C_{out}} & \frac{\Delta V C_{fly}}{2 K C_{out}} \\ -kp & -p \end{bmatrix} & B = \begin{bmatrix} 1/C_{out} & 0 \\ 0 & kp \end{bmatrix} \\ C = \begin{bmatrix} 1 & 0 \end{bmatrix} & D = \Theta \\ Y = V_{out} & \end{cases} \tag{7.7}$$

$$\begin{cases} A = \begin{bmatrix} -\frac{\mathbf{F_{sw}} C_{fly}}{K C_{out}} & \frac{\Delta V C_{fly}}{2 K C_{out}} \\ -kp & -p \end{bmatrix} = \begin{bmatrix} -\frac{1}{R_{out} C_{out}} & \frac{\Delta V}{2 R_{out} \mathbf{F_{sw}} C_{out}} \\ -kp & -p \end{bmatrix} \\ det\left[A - \lambda\right] = \begin{vmatrix} -\frac{1}{R_{out} C_{out}} - \lambda & \frac{\Delta V}{2 R_{out} \mathbf{F_{sw}} C_{out}} \\ -kp & -p - \lambda \end{vmatrix} \\ = \lambda^2 + \left[p + \frac{1}{R_{out} C_{out}}\right]\lambda + \frac{p}{R_{out} C_{out}}\left[1 + \frac{k \Delta V}{2 \mathbf{F_{sw}}}\right] \\ \approx \lambda^2 + \left[p + \frac{1}{R_{out} C_{out}}\right]\lambda + \frac{p}{R_{out} C_{out}} \end{cases} \tag{7.8}$$

As expected the poles are: p and $\frac{1}{R_{out}C_{out}}$.
The block G is compose of a miller transconductance:

$$G_m = \frac{i_{bias}}{V_{ref} - v_{out}} \tag{7.9}$$

and the CERO oscillator which can be assumed has no dynamic, so it is modeled as a constant gain block

$$G_{CERO} = \frac{f_{sw}}{i_{bias}} \tag{7.10}$$

so that

$$k = g_m \times G_{CERO} \tag{7.11}$$

Reordering the block diagram as in Fig.7.1.3 we can isolate the non-linearities Φ to the feedback loop, and apply the descriptive function method, to estimate the existence of limit cycles that will provoke oscillations. If The linear block G is assumed to filter all harmonics except the main one, both V_{out} and f_{sw} will be a simple tone, then we can define the non-linear block gain as

$$\Psi(j\omega_n) = \frac{V_{out}e^{j\theta_V}}{F_{sw}e^{j\theta_F}} \tag{7.12}$$

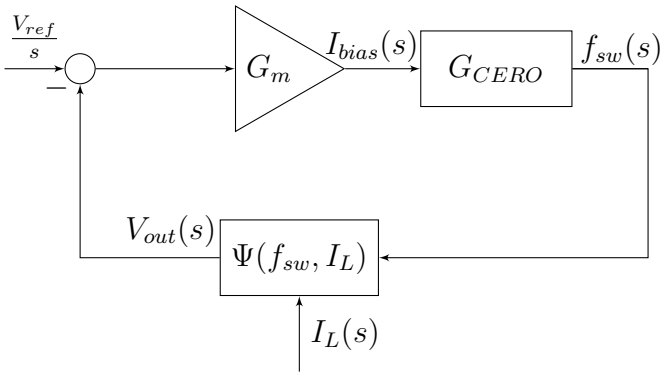

Figure 7.1.3: Linear Loop Block Diagram 2

Then we can write the Barkhausen Criterion as:

$$G(j\omega_n)\Phi(j\omega_n) + 1 = 0 \tag{7.13}$$

Using Eq.7.6 we can write the frequency to output voltage (lower block) gain as:

$$\frac{v_{out}}{f_{sw}} = \frac{\frac{\Delta V}{2F_{sw}}}{1 + R_{out}C_{out}s} \tag{7.14}$$

and the the feedback loop (upper block) as:

$$G(j\omega) = \frac{k \times p}{j\omega + p} = \frac{G_{CERO}(g_m \times p)}{j\omega + p} \tag{7.15}$$

then the Barkhausen module condition is:

$$\left\| \frac{\Delta V}{2F_{sw}(1 + j\omega R_{out}C_{out})} \right\| \left\| \frac{kp}{j\omega + p} \right\| = 1 \tag{7.16}$$

assuming the frequency is above the pole $p : \omega \gg p$, and taking R_{out} as:

$$R_{out} = k(N-1)/\mathbf{F_{sw}}C_{fly}$$

we can do the approximation:

$$1 \approx \frac{\Delta V k p}{2\mathbf{F_{sw}}\omega} \frac{1}{\sqrt{1 + \left(\frac{K(N-1)\omega}{\mathbf{F_{sw}}}\right)^2}} \tag{7.17}$$

$$0 = \omega^4 + \frac{\mathbf{F_{sw}}^2}{K^2(N-1)^2}\omega^2 - \frac{\Delta V^2 k^2 p^2}{4K^2(N-1)^2} \tag{7.18}$$

$$w^2 = \frac{\mathbf{F_{sw}}^2}{2K^2(N-1)^2}\left[1 \pm \sqrt{1 + \frac{\Delta V^2 k^2 p^2}{\mathbf{F_{sw}}^4}}\right] \tag{7.19}$$

There are two simplified solutions depending on the value of $\frac{\Delta V k p}{\mathbf{F_{sw}}^2}$:

$$\begin{cases} \frac{\Delta V k p}{\mathbf{F_{sw}}^2} \ll 1 \Rightarrow \sqrt{\Delta V k p} \ll \mathbf{F_{sw}} \\ \omega_{osc} \approx \frac{\mathbf{F_{sw}}}{K(N-1)} \end{cases} \tag{7.20}$$

$$\begin{cases} \frac{\Delta V k p}{\mathbf{F_{sw}}^2} \gg 1 \Rightarrow \sqrt{\Delta V k p} \gg \mathbf{F_{sw}} \\ \omega_{osc} \approx \frac{\sqrt{\Delta V k p/2}}{K(N-1)} \end{cases} \tag{7.21}$$

Giving the parameters values:

$$\begin{cases} \Delta V = 0.4V \\ k = 4.6 \times 10^9 Hz/V \\ p = 100Hz \\ K = 1/3 \\ N = 12 \\ \sqrt{\Delta V k p} \approx 430kHz \end{cases} \tag{7.22}$$

Where the $K = 2/3$ value from Eq.4.13 has been divided by 2 because the Pulse Generator Block creates two pulses for each period of the clock signal, given an effective frequency of twice the value of $\mathbf{F_{sw}}$.Assuming the condition of Eq.7.21 is true then we find that the oscillations frequency w_{osc} is independent of $\mathbf{F_{sw}}$, and takes a value:

$$f_{osc} \approx 3.3kHz \tag{7.23}$$

The actual value of $\mathbf{F_{sw}}$ is proportional to the load, and varies. But as long as condition 7.21 holds, the oscillation frequency is constant.

Note we haven't checked if the phase condition for the Barkhausen criterion is met, for low frequencies $\mathbf{F_{sw}}$ this is not necessary. As the module condition is independent of $\mathbf{F_{sw}}$, we can choose a $\mathbf{F_{sw}}$ so that the Barkhausen phase condition is met. This is simply done by selecting $\mathbf{F_{sw}}$ so that $\angle\Phi(j\omega_{osc})$, with pole $1/R_{out}C_{out}$, which varies with $\mathbf{F_{sw}}$, adds a phase $\theta = 180 - \angle G_m(j\omega_{osc})$ at frequency w_{osc}. This is why oscillations are always present for low enough switching frequencies, for higher frequencies when the condition from Eq.7.20 is met, the module and phase Barkhausen conditions cannot be met at the same time, as both vary with switching frequency $\mathbf{F_{sw}}$.

7.2 Implementation and Simulations

The actual circuit used for G_m is shown in Fig.7.2.3, polarized with an $I_{bias} = 100pA$. It's bode diagram in Fig.7.2.4, in the second one we see that phase for f_{osc}. In Fig.7.2.1 and Fig.7.2.2 we see how oscillations appear for $\mathbf{F_{sw}} \leq 40KHz$ approximately, and the oscillations are around $f_{osc} = 3.3kHz$.

Furthermore, we can calculate the phase added by $\angle\Phi(j\omega_{osc})$:

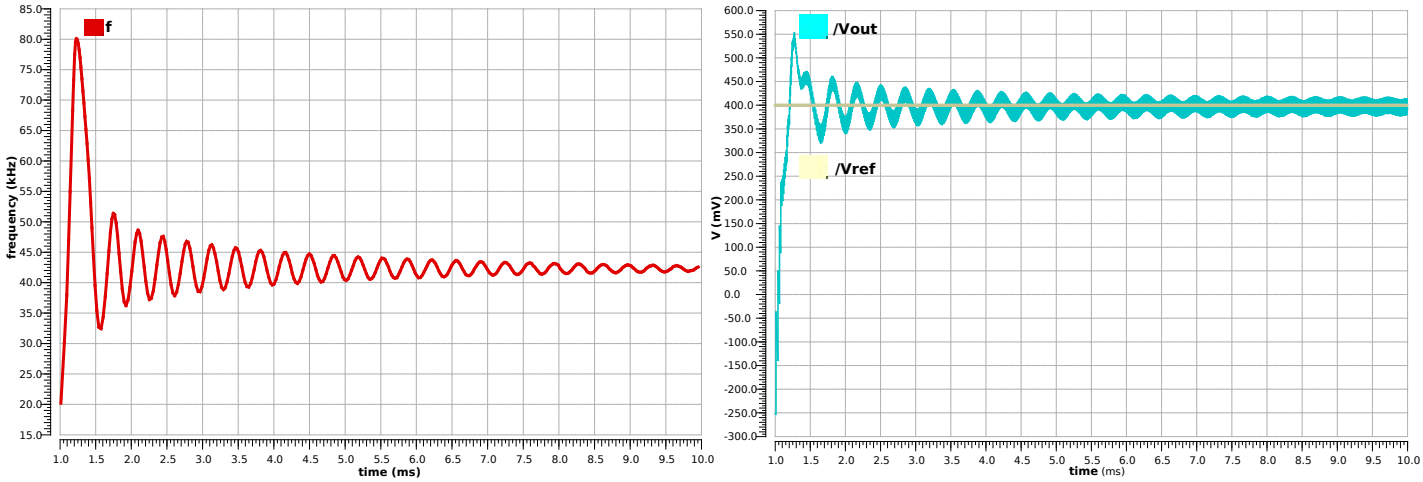

Figure 7.2.1: Graph F_{sw} and V_{out} for $I_L = 700nA$.

$$\angle\Phi(j\omega_{osc}) = Arctan\left(\omega_{osc}R_{out}C_{out}\right) = Arctan\left(\frac{\omega_{osc}K(N-1)C_{fly}}{F_{sw}C_{fly}}\right) \tag{7.24}$$

$$= Arctan\left(\frac{\omega_{osc}K(N-1)}{F_{sw}}\right) \approx Arctan\left(\frac{2\pi(3.3kHz)11/3}{40kHz}\right) \approx 1.086rad \approx 62.24^\circ \tag{7.25}$$

This phase added to the phase $\angle G(j\omega_{osc})$ shown in Fig.7.2.4, we obtain a total phase: $\angle\Phi(j\omega_{osc}) + \angle G(j\omega_{osc}) = 175.43^\circ$, approximately the Barkhausen condition. The total

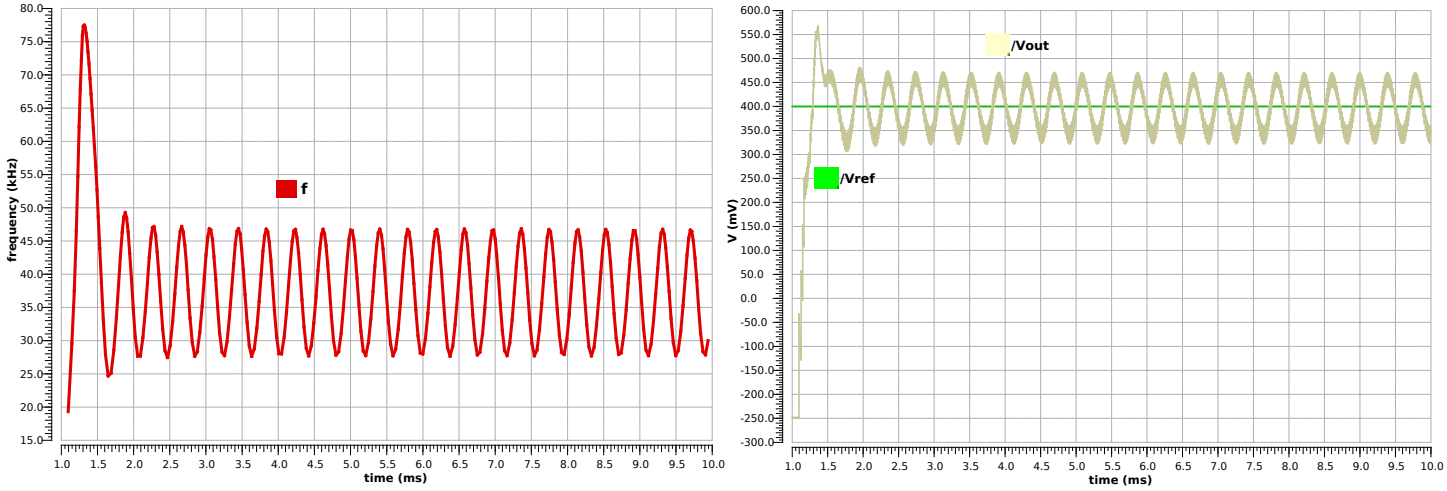

Figure 7.2.2: Graph F_{sw} and V_{out} for $I_L = 600nA$.

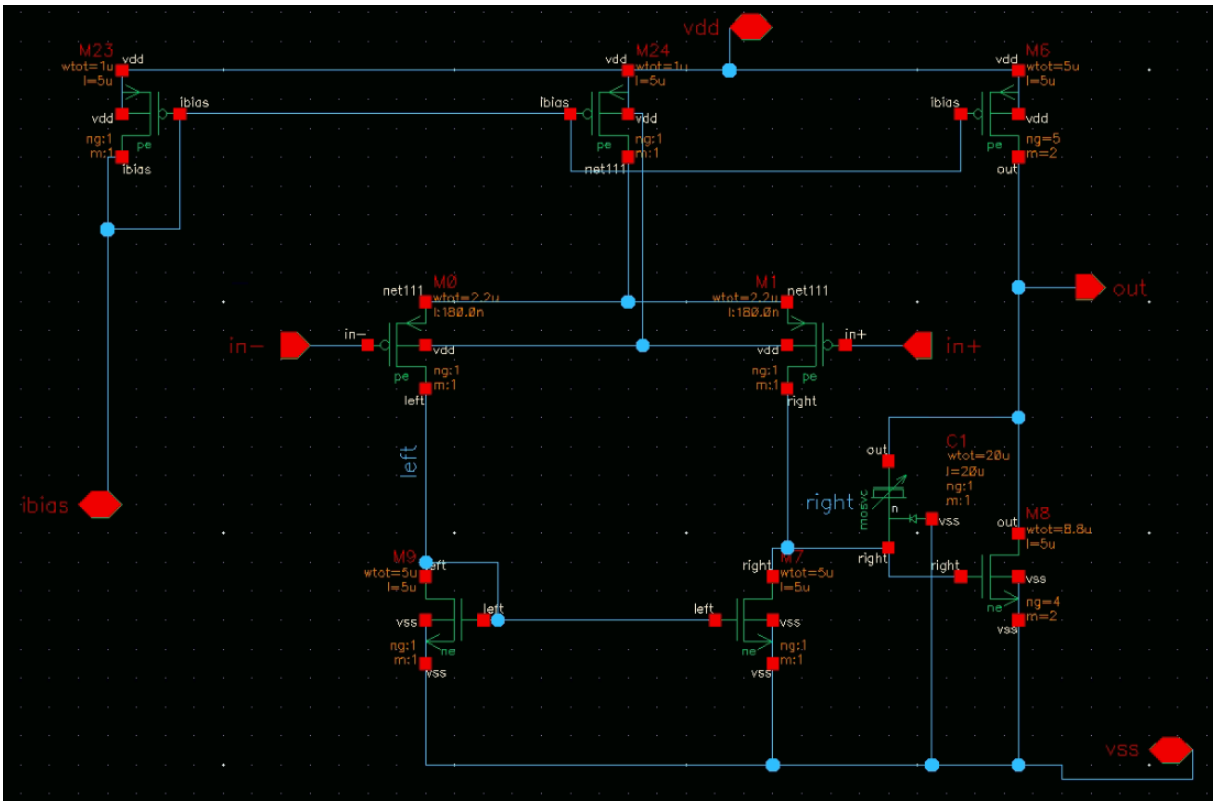

Figure 7.2.3: Trans-conductance G_m Miller Circuit.

$180°$ are obtained if $F_{sw} = 30kHz$.

Another drawback of the linear loop is that to filter the switching ripple and to be ultra-low power the G_m pole must be very low frequency, which makes the system slow to respond. The idea is that when a sharp step in load current happens the non-linear loop will actuate, this is true when a sharp increase in load current happens. But if

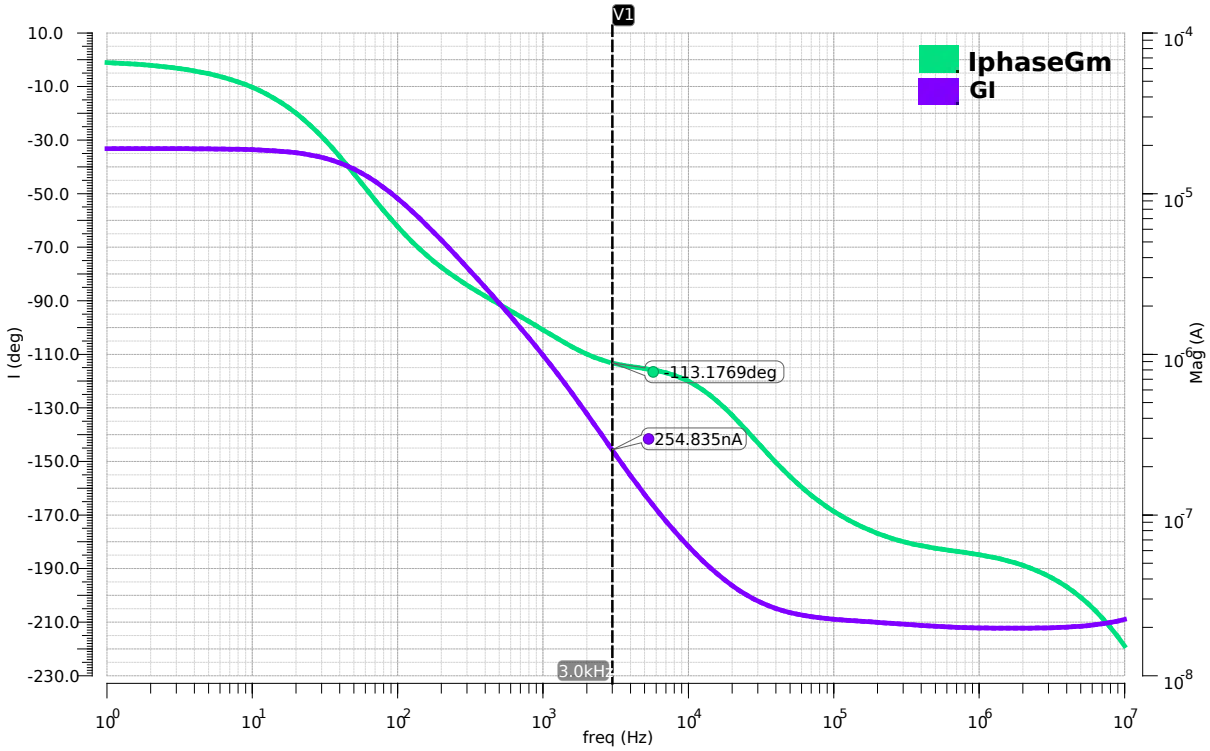

Figure 7.2.4: Trans-conductance G_m Bode Plot.

there is a sharp decrease in current load, and the non-linear loop was not functioning (bias current provided by the linear G_m), as at the end of a current pulse, then the G_m will be very slow to respond and the output voltage will increase up to the no-load voltage.

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Chapter 8

Conclusions

8.1 Efficiency

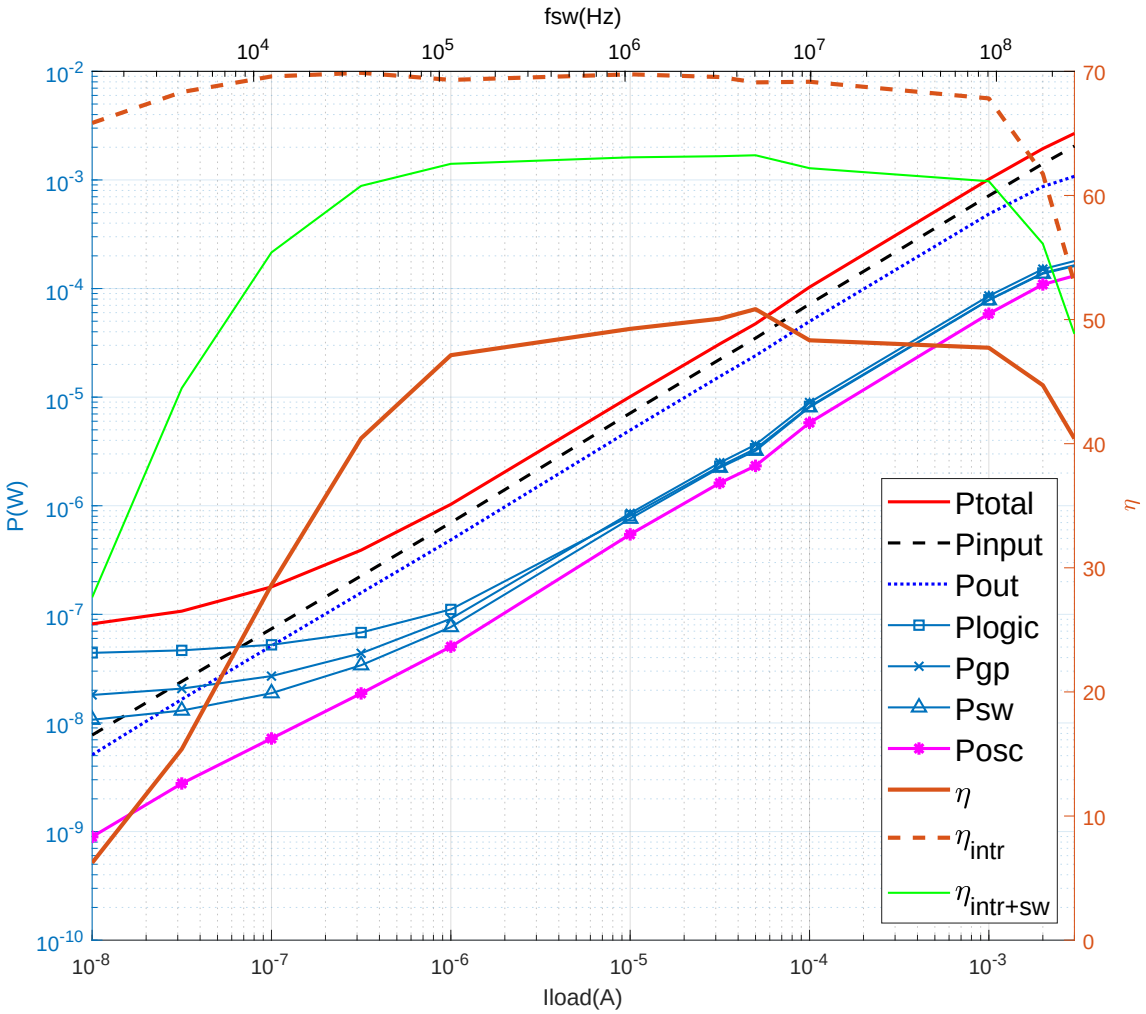

Figure 8.1.1: Total System Efficiency

In Fig.8.1.1 we see a total system efficiency and in Fig.E.0.1 the complete system layout occupying $0.24mm \times 0.56mm \approx 0.134mm^2$, giving a power density of approximately $P/A \approx 22mW/mm^2$. Although this work wasn't directed at achieving high power density, this power density is not low for low power oriented works, but works that are high power density oriented can achieve up to 40 times this power density [34], [35], [36].

Firstly in Fig.8.1.1 we see that the total system efficiency is always below 50%, this suggests bigger capacitors are needed in order to further reduce switching losses. If area constraints don't allow this another option is to reduce the number of phases, this reduces switching capacitance proportionally, the underside is that ripple voltage increases. In 3 the optimization suggested $N_{phases} = 6$ but N_{phases} was set to 12 to further reduce ripple in the case where the non-linear loop actuates and a great step in voltage can occur. Logic should be further optimized to reduce the number of gates.

The efficiency falls sharply for $I_L < 1\mu A$. This is due to the block whose power is not proportional to frequency/load at low frequencies/loads. Namely, the Logic, Non-Overlapping Pulse Generator, and Switches Buffers, that present leakage currents. In table 8.1 we see the dc power of these blocks, as the circuity was designed with minimum transistor length to reduce switching losses, the leakage losses are significant. To reach better low power efficiencies it's necessary to explore leakage reduction techniques that do not add considerable load capacitance in the digital circuits. The green line of Fig.8.1.1 $\eta_{intr+sw}$ represents the efficiency considering only intrinsic losses and switch driving losses, these losses are particular in that they are the only ones that scale proportionally with total output power. This means that for a given power density the total output power and area increases with the capacitor and switches size, but logic circuity remains the same, growing the converter proportionally would bring closer the total efficiency to the $\eta_{intr+sw}$. For ultra-low-power, this would only be valid if the leakage of the switches drivers is much greater than the other digital circuity leakage.

	P_{dc} **Leakage**
Non-Overlapping Pulse generator	$16.71nW$
Logic	$2.05nW \times N_{phases} = 24.60nW$
Switches Buffers	$0.464nW \times N_{phases} = 5.60nW$

Table 8.1: Main Leakage Sources

A possible optimization is to remove the non-overlapping pulse generator and obtain the non-overlapping pulses from the CERO oscillator with 12 stages as shown in Fig.8.1.2. Although this would multiply the oscillator leakage by more than 4 times, so it is not clear if the total power would be less for low power loads. Power for mid and high-power loads could probably be reduced.

Other strategies involve using multiple voltage domains, as developed in [37], [38] using 2 voltage domains: V_{high} to V_{mid} and V_{mid} to V_{low}, where V_{high},V_{mid} are V_{in},V_{out} for a step-down or V_{out},V_{in} for a step-up. The circuity is doubled, but as switching frequencies

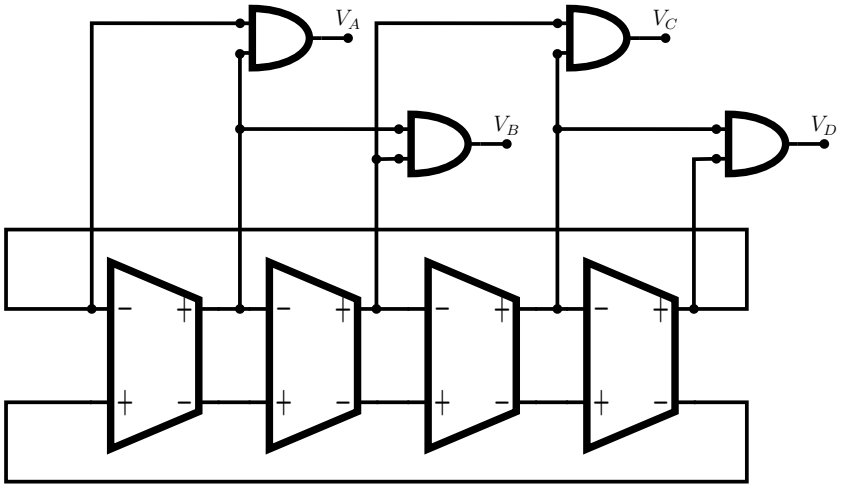

Figure 8.1.2: CERO Modified.

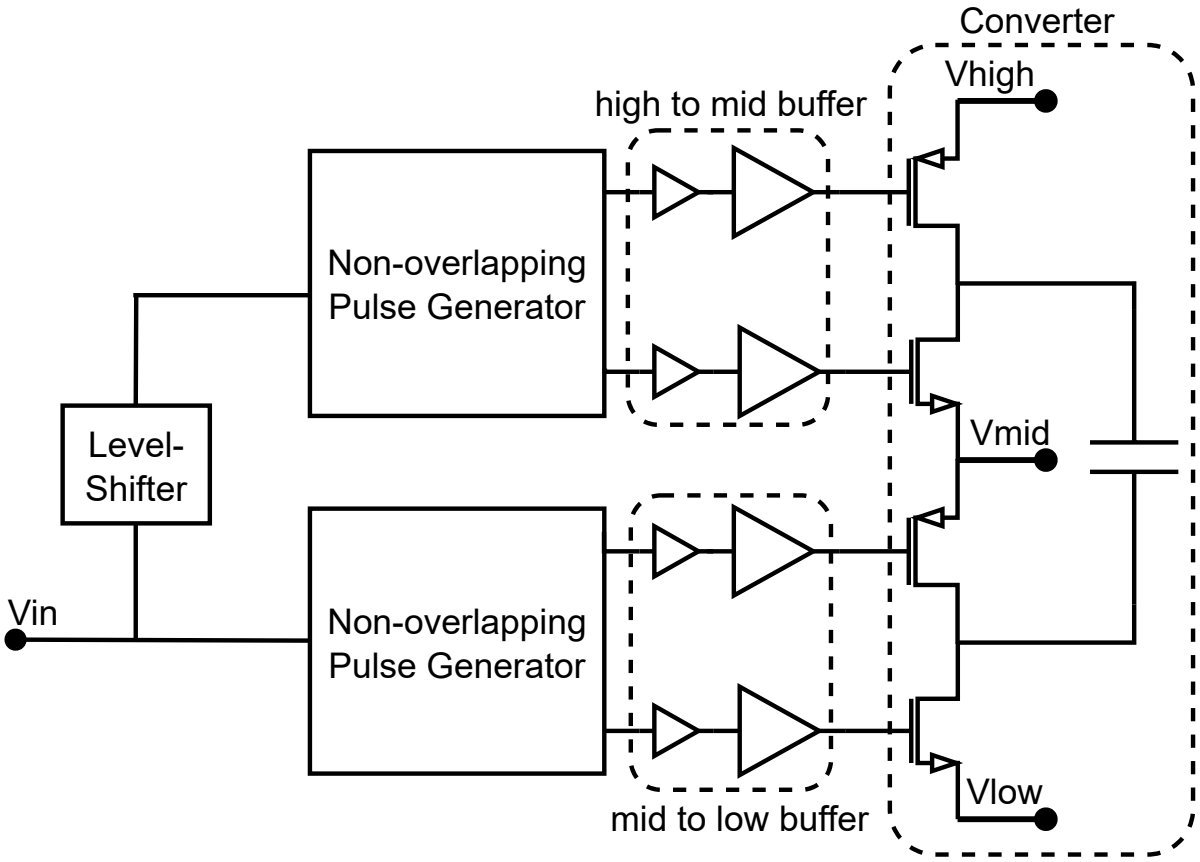

Figure 8.1.3: Multi-Voltage Domains Converter [37]

decrease with voltage square, the power is further reduced and leakage is also reduced. In the case of a step-up blocks can operate at a voltage below nominal to reduce power consumption by operating between V_{in} and ground.

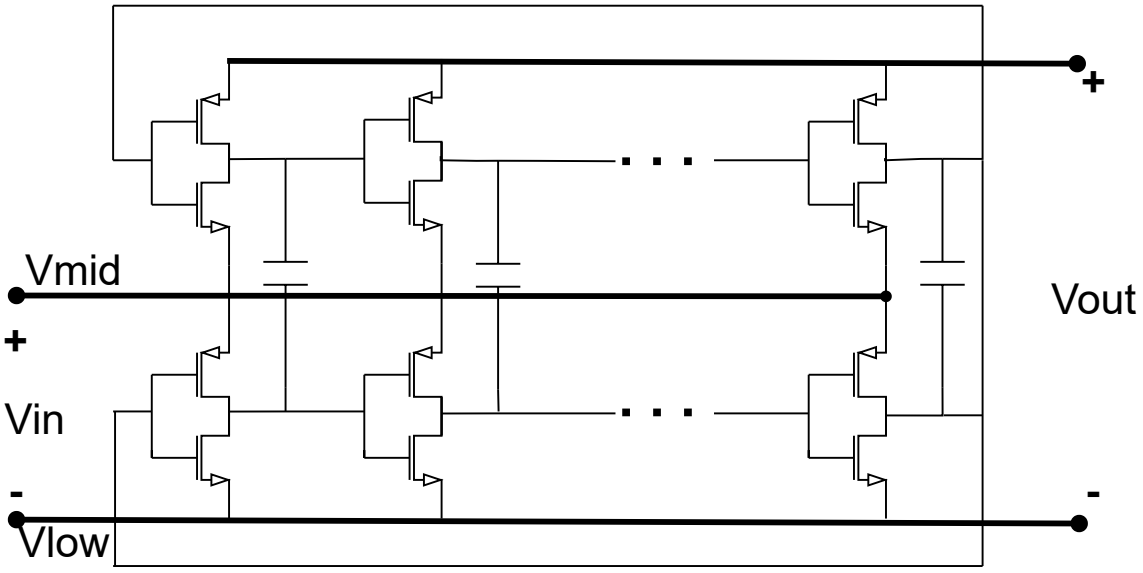

Figure 8.1.4: Proposed Self-Oscillating Converter in [38]

Going beyond just optimizing these blocks, some authors attempt to remove them altogether by implementing a self-oscillating converter [38], see Fig8.1.4, where a stacked ring oscillator is implemented to produce a voltage doubler, architectures such as this one or such as Cross Coupled Voltage Doublers [39] and Dickson architectures [40] are highly efficient, but are step-up only and have low output power capabilities. This wouldn't be a problem for ULP only systems.

8.2 Step Response

Maintaining low power efficiency and having fast step response are directly contra-posed to one another.

Comparator response time at an output power of: $\eta@P_{out} = 100nW$ maintaining high efficiency would imply

$$P_{static} < 10nW \Rightarrow Ibias < \frac{10nW}{1.8V} \approx 5.6nA$$

this would mean a response time for charging/discharging a minimum inverter of $C_g \approx 1fF$ of

$$t_{response} \approx \frac{(1.8V)(1fF)}{5.6nA} = 320ns$$

.

Output voltage variation at a load step of: $I_L = 1mA$ for

$$\begin{cases} C_{out} & = 1nF \\ I_L & = 1mA \\ v_{ripple} & < 50mV \end{cases} \tag{8.1}$$

$$\Rightarrow t_{50mV} = \frac{(50mV)(1nF)}{1mA} = 50ns \tag{8.2}$$

A Monolithic Converter that doesn't need an off-chip capacitor would need to respond fast to a load step, like the one given by a digital load. This means that comparators should have a minimum number of non-static nodes. Also, amplifying transistors should be common gate instead of common source, so that internal loads are minimized.

An alternative comparator strategy is presented by [41], in which an inverter bases comparator is used. In order to control that the inverter commutates at V_{ref}, it's supply voltage is set to be $2V_{ref}$. The error is temperature and technology dependent, but a relatively fast low power converter can be built.

In table 8.2 a chart with different papers is presented. The main architecture points of the converter are displayed, where the ones in orange or red represent undesirable aspects. It can be seen that at least one point has undesirable characteristics in each case.

Paper	Topology	On-Chip Cap	Off-Chip Cap	Frec Range	Clk Topology	Load Range	Tec Node + Extras	Peak Eff	Low Power Efficiency	
A Fully Integrated Switched-Capacitor BasedPMU with Adaptive Energy Harvesting Technique for Ultra-Low Power Sensing Applications(2013)	Phase-interleaved ladder-type SCN	1.03nF	No	340	Fixed frequency oscillator	12.8nW-20uW @61%Eff	180nm +MIM	63.80%	60.7%@12.8nW	intrinsic efficiency
A 60%-Efficiency 20nW-500 W Tri-Output FullyIntegrated Power Management Unit with Environmental Adaptation and Load-Proportional Biasing for IoT Systems(2016)	7-b Binary + 2:1 SC + 1:3 Dickson	3nF	No	50Hz-10MHz	NA	20nW-500uW @60%Eff	180nm +MIM	81%	60%@20nW	intrinsic efficiency?
An Ultra-Low Power Fully Integrated Energy Harvester Based on Self-Oscillating Switched-Capacitor Voltage Doubler(2014)	Self-oscillating voltage doubler	600pF	No	70Hz-19MHz	CERO like clk	2.4nW-840uW @70%Eff	180nm	75%	70%@2.4nW	intrinsic efficiency
A Dual-Mode DC/DC Converter for Ultra-Low-Voltage Microcontrollers(2012)	SCN with BB	200pF	No	20-120kHz	Vring<0.5V + 20MHz Ext clock	25nW-125uW	130nm +MIM	75%	63%@100nW 74%@400nW	total system efficiency
A 34 nA Quiescent Current Switched-Capacitor Step-down Converter with 1.2V output voltage and 0-5 A load current(2020)	unique Cfly SCN	300pF	20nF CL	NA	CERO like clk	3.6-6uW	180nm +MIM	>88%	88%@3uW	total system efficiency
This Work	Modular Converter	460pF	No	$1kHz - 20MHz$	CERO	$4nW - 400\mu W$	180nm SOI	70%	70%@1uW	intrinsic efficiency

Table 8.2: Comparison of key aspects in other works.

Finally it is worth noting that a model for, how to deduct the constrains and optimize a generic switched capacitor converter was developed, with which a first approach to

autotomizing the sizing of components can be obtained. Furthermore, the proposed closed loop model for control was shown to predict correctly the characteristics of the converter, and explained the appearance of sustained oscillations under an analog closed loop state.

Appendix A

Log-Sum-Exp form is convex:

Proof that Eq.3.39 is convex

$$f(tx + (1-t)y) = log\left(\sum e^{tx_i + (1-t)y_i}\right)$$

as all the terms are positive, the cross terms are positive so:

$$log\left(\sum e^{tx_i+(1-t)y_i}\right) \leq log\left(\sum e^{tx_i} \sum e^{(1-t)y_i}\right) \tag{A.1}$$

$$= tlog\left(\sum e^{x_i}\right) + (1-t)log\left(\sum e^{y_i}\right) \tag{A.2}$$

$$= tf(x) + (1-t)f(y) \tag{A.3}$$

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Appendix B

Proof of Eq.3.1

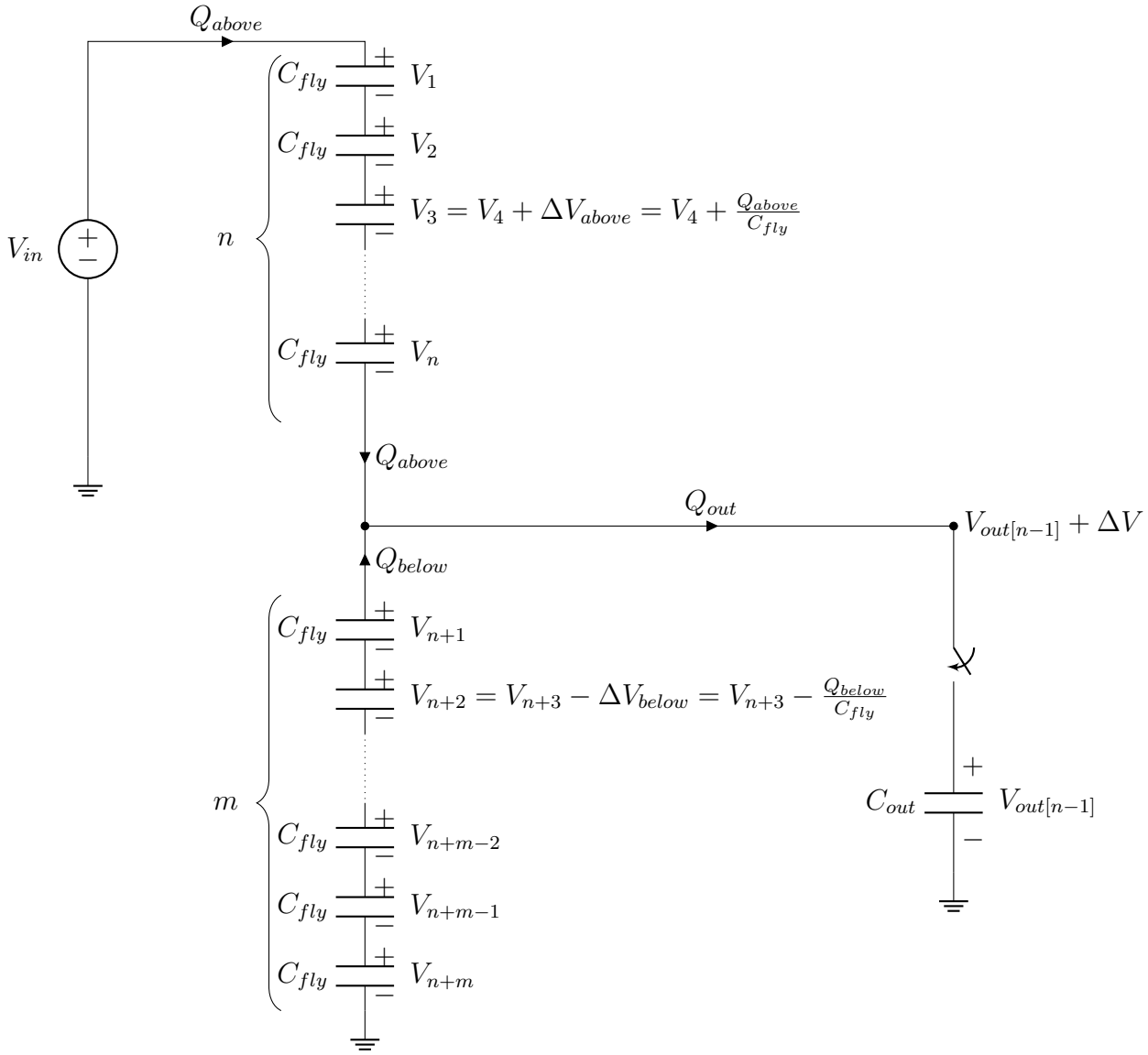

Figure B.0.1: Modular Converter Charge distribution

Modular Converter Charge distribution: Fig.B.0.1 shows a generic modular converter in steady state. Before the output switch is closed the output node V_{out} is above the load $V_{out}[n-1]$ voltage by a voltage ΔV. For a $n+m$ modular converter with no load output voltage $V_{in}\frac{m}{n+m}$ there are n capacitors above the output node and m capacitors below it. In each cycle the above capacitors are charge by the charge that goes to the load from above Q_{above}, likewise the below capacitors are discharged by the charge that goes to load from below Q_{below}. In steady state when a capacitor does a full cycle it will end up with the same charge they had at the beginning, therefor the result of charging a capacitor n times and discharging it m times must be null, then we obtain Eq.B.1. The output charge for one cycle is formed by $Q_{above}+Q_{below}$, so we can express Q_{out} as in Eq.B.2.

$$in\ steady\ state\ ther's\ charge\ conservation \Rightarrow nQ_{above} = mQ_{below} \tag{B.1}$$

$$Q_{out} = Q_{above} + Q_{below} = Q_{above}\left(1+\frac{n}{m}\right) \tag{B.2}$$

$$Q_{above} = Q_{out}\frac{m}{n+m} \tag{B.3}$$

$$Q_{below} = Q_{out}\frac{n}{n+m} \tag{B.4}$$

$$\tag{B.5}$$

$$\Delta V = m\frac{Qbelow}{C_{fly}} = n\frac{Qabove}{C_{fly}} = \frac{Q_{out}}{C_{fly}}\frac{nm}{n+m} \tag{B.6}$$

$$\Delta V_{above} = \frac{Q_{above}}{C_{fly}} = \frac{Q_{out}}{C_{fly}}\frac{m}{n+m} \tag{B.7}$$

$$-\Delta V_{below} = \frac{Q_{below}}{C_{fly}} = \frac{Q_{out}}{C_{fly}}\frac{n}{n+m} \tag{B.8}$$

$$\tag{B.9}$$

After a complete cycle, when the capacitor has done a full lap, the sum of all ΔV must be zero in steady state. At the same time the sum of all capacitor voltages must be equal to V_{in}, therefor we can express a each voltage as $V(i) = \frac{V_{in}}{n+m} + \Delta V(i)$, express in the most general form we obtain:

$$V(i) = \frac{V_{in}}{n+m} + Y(n-i)\frac{Q_{out}}{C_{fly}}\frac{i\times m}{n+m} + -Y(i-n)\frac{Q_{out}}{C_{fly}}\frac{(i-n)\times n}{n+m}, \quad i\in[1,n+m] \tag{B.10}$$

Where $Y(i)$ is the Heavyside step discrete function.

Appendix C

Python code SCC Optimization

```
from numpy import *
# X = (w,N,f,Cfly)
pi = 3.1416
K = 13.5
VDD = 1.8  # (V)
Vtn0 = 0.6  # (V)
Vtp0 = 0.67  # (V)
Lmin = 0.180  # (um)
fCTP = 1e-4  # (factor )
fCBP = 1e-4  # (F)
Cmosvc = 2.4e-15  # (F/um^2) esto esta raro porque este es mas grande que
    Cox
nn = 1.4525
np = 1.5185
muneff = 294  # (cm^2/Vs)
mupeff = 64  # (cm^2/Vs)
epsr = 3.9
eps0 = 8.854e-12
tox = 4.1e-9
#Cox = epsr * eps0 / tox * 1e-12  # (F/um^2)
Cox = 1.55e-15
Betan = 243e-6  # (A/V^2)
Betap = 53.5e-6  # (A/V^2)
#Ileak = 10e-9
Ileak = 10e-15

#Vout = 0.4#
#Vout = linspace(0.2, 0.5, 10)
Flag = 0
if Flag==1:
    Vout = linspace(0.2, 1.5, 200)
    VNL = zeros(len(Vout))
    DV = zeros(len(Vout))
    gds = zeros(len(Vout))
    gdsn = zeros(len(Vout))
    gdsp = zeros(len(Vout))

    j = 0;
```

```
    for vout in Vout:

        if vout >= 1.19:
            VNL[j] = VDD
        if 0.59 <= vout < 1.19:
            VNL[j] = 2 * VDD / 3
        if vout < 0.59:
            VNL[j] = VDD / 3
        DV[j] = 2 * (VNL[j] - vout)

        gdsn[j] = Betan * (VDD - Vtn0 - (nn -1) * vout - nn * DV[j] / 2) / Lmin
        if gdsn[j] < 0:
            gdsn[j] = 0
        gdsp[j] = 2 * Betap * (VNL[j] - Vtp0 - (np -1) * (VDD - VNL[j]) - np * DV[j] / 2) / Lmin
        if gdsp[j] < 0:
            gdsp[j] = 0

        gds[j] = gdsn[j] + gdsp[j]
        j = j + 1
else:
    Vout = 0.4
    if Vout >= 1.19:
        VNL = VDD
    if 0.59 <= Vout < 1.19:
        VNL = 2 * VDD / 3
    if Vout < 0.59:
        VNL = VDD / 3
    DV = 2 * (VNL - Vout)

    gdsn = Betan * (VDD - Vtn0 - (nn - 1) * Vout - nn * DV / 2) / Lmin
    if gdsn < 0:
        gdsn = 0
    gdsp = 2 * Betap * (VNL - Vtp0 - (np - 1) * (VDD - VNL) - np * DV / 2) / Lmin
    if gdsp < 0:
        gdsp = 0

    gds = gdsn + gdsp


IL = 1e-3
vripple = 50e-3
```

```
from cvxopt import matrix, log, exp, solvers
import variables as var
import numpy as np

# X = (w,N,f,Cfly)
# pi = 3.1416
# K = 13.5
# VDD = 1.8  # (V)
# Vtn0 = 0.6  # (V)
```

```
# Vtp0 = 0.67  # (V)
# Lmin = 0.180  # (um)
# fCTP = 1e-15  # (F)
# fCBP = 1e-15  # (F)
# Cmosvc = 2.4e-15  # (F/um^2) esto esta raro porque este es mas grande que Cox
# nn = 1.7
# np = 1.9
# muneff = 294  # (cm^2/Vs)
# mupeff = 64  # (cm^2/Vs)
# epsr = 3.9
# eps0 = 8.854e-12
# tox = 4.1e-9
# Cox = epsr * eps0 / tox * 1e-12  # (F/um^2)
# Betan = 243e-6  # (A/V^2)
# Betap = 53.5e-6  # (A/V^2)
#
# Vout = 0.4
# VNL = VDD / 3
# DV = VNL - Vout
# IL = 1e-3
# vripple = 10e-3
def get_max_power():
    F = matrix([[1., 0., 0., 0., -1., -1., 0., 1, 0, 0, 0, 0, 0],
                [1., 1., 0., -1., -1., 0., -1., 0, 1, 0, 0, 0, 0],
                [0., 0., -1., 0., 1., 0., 0., 0, 0, -1, 0, 1, 0],
                [0., 1., -1., 0., 1., 0., 0., 0, 0, 0, 1, 0, -1]])

    g = log(matrix([3 * var.K * var.Lmin, # Area SW
                    3 / var.Cmosvc, # Area cap
                    2 / 3 * var.IL / var.DV, 0.75 * var.DV / var.vripple,
                    3 * 4 * var.pi / var.gds,
                    0.22, 1, 1e-3, 1e-3, 1, 10e6, 1e-9, 10e-15]))
    K_cvx = [2, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1]
    W, N, f, Cfly = exp(solvers.gp(K_cvx, F, g)['x'])

    N = np.round(N)
    W = 0.22 * np.round(W / 0.22)
    # A = 1.3 * K * N * W * Lmin + 3 * N * Cfly / Cmosvc  # (um2)
    # sqrtA = A ** 0.5
    Pleak = var.VDD * var.Ileak * N
    Posc = 3.7e-13 * f
    Psw = 3 * var.K * 2 * f * var.VDD ** 2 * W * var.Lmin * var.Cox
    Pdv = Cfly * var.DV ** 2 * f
    Ptbp = N * f / 2 * Cfly * (var.fCTP + var.fCBP) * (2 * (var.VDD / 3 + var.DV / 2) ** 2 + (2 / 3 * var.VDD - var.DV / 2) ** 2)
    pT = Psw + Pdv + Ptbp + Posc + Pleak
    return pT
```

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Appendix D

Transfer function of 2:1 Converter

Charge conservation implies that the amount in both capacitors in series must equal the charge of both capacitors in parallel plus the charge delivered to the load, defining $T = 1/f_{sw}$:

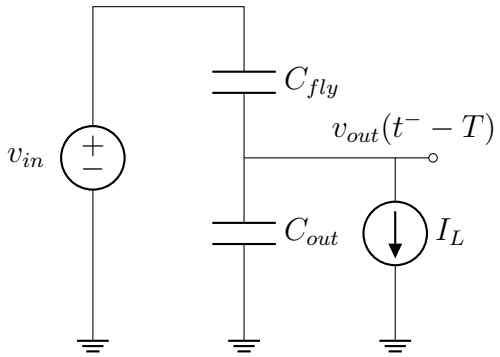


Figure D.0.1: subfigure
Series

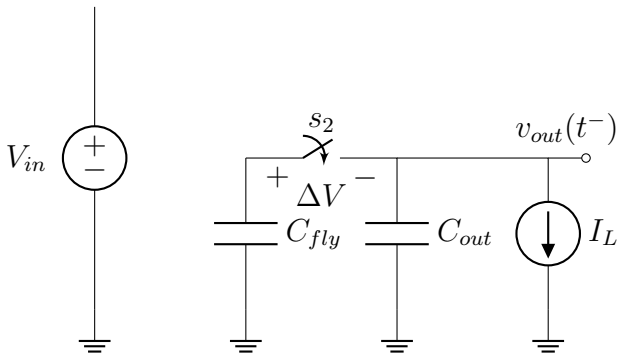
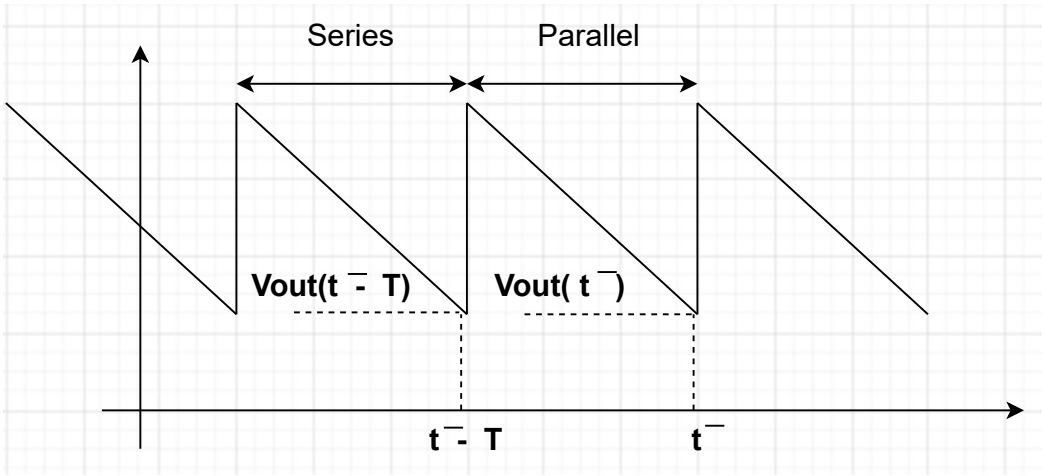


Figure D.0.2: subfigure
Parallel

Figure D.0.3: Series Parallel Converter



$$Q_{Cfly}(t^- - T) + Q_{Cout}(t^- - T) = \int_{t^- - T}^{t^-} i_L + Q_{Cfly}(t^-) + Q_{Cout}(t^-) \tag{D.1}$$

$$C_{fly}\left[v_{in}(t^- - T) - v_{out}(t^- - T)\right] + C_{out}v_{out}(t^- - T) = \int_{t^- - T}^{t^-} i_L(u)du + (C_{fly} + C_{out})v_{out}(t^-) \tag{D.2}$$

Taking Laplace Transform on both sides:

$$C_{fly}e^{-sT}\left[V_{in}(s) - V_{out}(s)\right] + C_{out}V_{out}(s)e^{-sT} = \frac{I_L(s)}{s}(1 - e^{-sT}) + (C_{fly} + C_{out})V_{out}(s) \tag{D.3}$$

$$V_{out}(s) = \frac{V_{in}(s)C_{dly}e^{-sT} - \frac{I_L(s)}{s}(1 - e^{-sT})}{(C_{fly} + C_{out}) + (C_{fly} - C_{out})e^{-sT}} \tag{D.4}$$

$$with \quad V_{in}(s) = V_{in}/s,\ I_L(s) = I_L/s \tag{D.5}$$

$$V_{out}(s) = \frac{V_{in}C_{fly}e^{-sT} - \frac{I_L}{s}(1 - e^{-sT})}{s\left[(C_{fly} + C_{out}) + (C_{fly} - C_{out})e^{-sT}\right]} \tag{D.6}$$

$$\lim_{t\to\infty} v_{out}(t) = \lim_{s\to 0} sV_{out}(s) = V_{in}\frac{C_{fly}}{2C_{fly}} - \frac{I_L T}{2C_{fly}} \tag{D.7}$$

The transform can also be expressed as:

$$V_{out}(s) = \frac{V_{in}C_{fly}e^{-sT} - \frac{I_L}{s}(1 - e^{-sT})}{s(C_{fly} + C_{out})}\frac{1}{\left(1 + \frac{C_{fly} - C_{out}}{C_{fly} + C_{out}}e^{-sT}\right)} \tag{D.8}$$

then the anti-transform is of the form:

$$v_{out}(t) = \sum_{n=0}^{\infty} \mathcal{L}^{-1}\left[\frac{V_{in}C_{fly}e^{-sT} - \frac{I_L}{s}(1 - e^{-sT})}{s(C_{fly} + C_{out})}\right](t - nT)\left(\frac{C_{fly} - C_{out}}{C_{fly} + C_{out}}\right)^n \tag{D.9}$$

$$\begin{aligned} v_{out}(t) = &\sum_{n=0}^{\infty}\left[\frac{C_{fly}}{C_{fly} + C_{out}}V_{in}Y(t - nT)\right]\left(\frac{C_{fly} - C_{out}}{C_{fly} + C_{out}}\right)^n \\ &-I_L\sum_{n=0}^{\infty}\left[\frac{[(t - nT)Y(t - nT) - (t - (n+1)T)Y(t - (n+1)T)]}{C_{fly} + C_{out}}\right]\left(\frac{C_{fly} - C_{out}}{C_{fly} + C_{out}}\right)^n \end{aligned} \tag{D.10}$$

In this type of function it is convenient to use $\mathcal{Z}$ Transform, doing a similar analysis with $i_L[n] = I_L T$ we obtain:

$$V_{out}[z] = \frac{z}{z-1}\left[\frac{C_{fly}V_{in} - zI_LT}{(C_{fly}+C_{out})z + C_{fly} - C_{out}}\right] \tag{D.11}$$

$$\lim_{n\to\infty} v_{out}[]n] = \lim_{z\to 1}(z-1)V_{out}[z] = V_{in}\frac{C_{fly}}{2C_{fly}} - \frac{I_LT}{2C_{fly}} \tag{D.12}$$

This transfer functions are valid as long as we operate in SSL.

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Appendix E

Layout

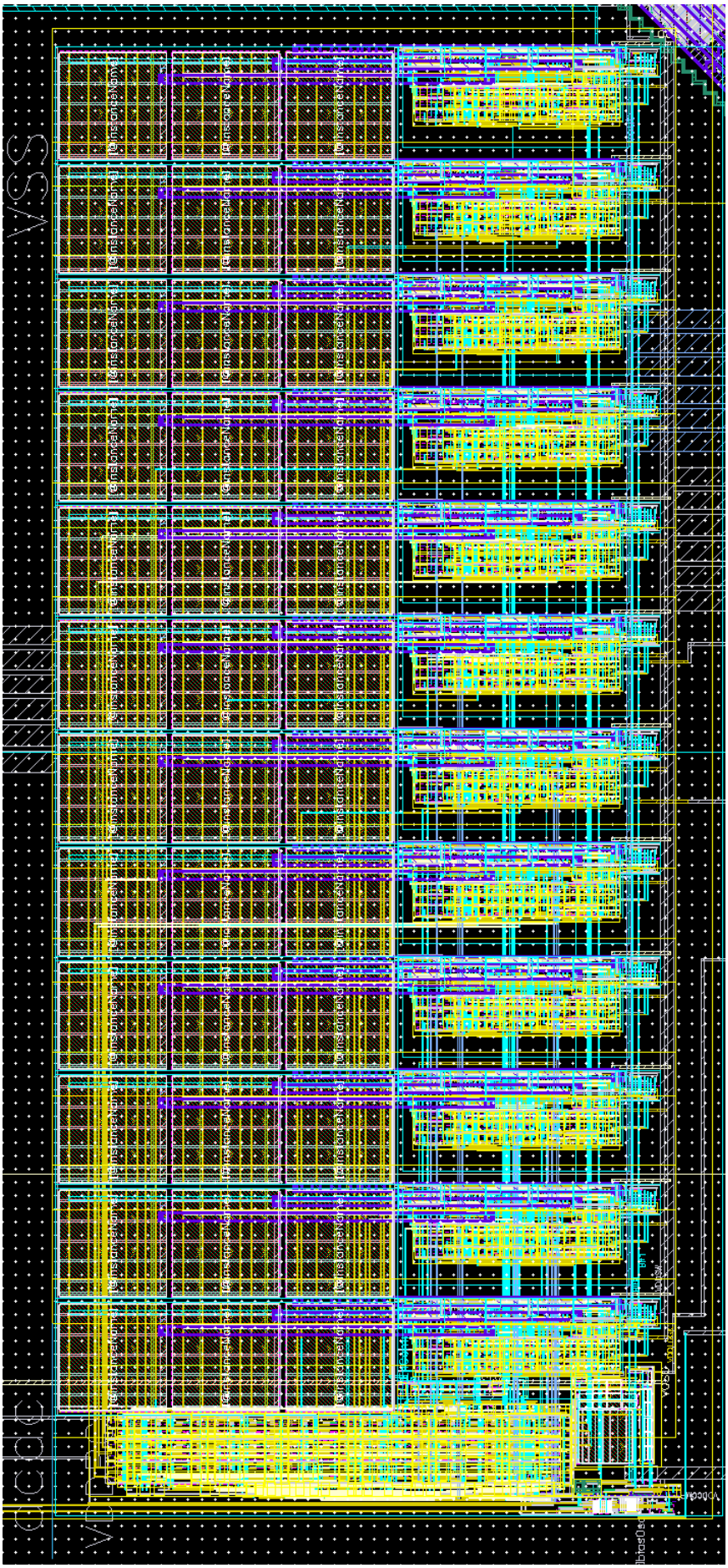

Figure E.0.1: Complete Layout $0.24mm \times 0.56mm \approx 0.134mm^2$

Bibliography

[1] G. Villar-Pique; H. Bergveld; E. Alarcon. Survey and benchmark of fully integrated switching power converters: Switched-capacitor versus inductive approach. *Power Electronics, IEEE*, 28:4156–4167, Sept 2013.

[2] Jieh-Tsorng Wu ; Kuen-Long Chang. Mos charge pumps for low-voltage operation. *IEEE Journal of Solid-State Circuits*, 33(4):1–6, 1998.

[3] Timothy McRae and Aleksandar Prodić. Design oriented analysis of switched capacitor dc–dc converters. *IEEE Open Journal of Power Electronics*, 1:2–13, 2020.

[4] Thomas N. Theis; H.-S. Philip Wong. The end of moore's law: A new beginning for information technology. *IEEE Journal of Computing in Science and Engineering*, 19:41–50, 2017.

[5] Leiserson C. E.; Thompson N. C.; Emer J. S.; Kuszmaul B. C.; Lampson B. W.; Sanchez D.; Schardl T. B. There's plenty of room at the top: What will drive computer performance after moore's law? *Science*, 368(6495), 2020.

[6] Bernard Aebischer; Lorenz M. Hilty. *The Energy Demand of ICT: A Historical Perspective and Current Methodological Challenges*. Springer, 2014.

[7] Eric Masanet; Arman Shehabi; Nuoa Lei1; Sarah Smith; Jonathan Koomey. Recalibrating global data center energy-use estimates. *Science*, 367(6481):984–986, 2020.

[8] Cambridge bitcoin electricity consumption index. https://cbeci.org/. Accessed: 2021-03-06.

[9] Michiel Van Breussegem, Tom; Steyaert. *CMOS Integrated Capacitive DC-DC Converters*. Springer, 2013.

[10] Sung-Mo "Steve" Kang. Presentation on theme: "ee222 high-speed low-power ics". 2017.

[11] *Design for testability of gated-clock FSMs*, March 1996.

[12] *Dynamic Voltage and Frequency Scaling based on Workload Decomposition*, Sug 2004.

[13] Yoann Pascal; Gael Pillonnet. Efficiency comparison of inductor-, capacitor-, and resonant-based converters fully integrated in cmos technology. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, 5:421–429, Sept 2015.

[14] *Energy Harvesting From Human and Machine Motion for Wireless Electronic Devices*, volume 96, Sept 2008.

[15] M.S. Makowski and D. Maksimovic. Performance limits of switched-capacitor dc-dc converters. In *Proceedings of PESC '95 - Power Electronics Specialist Conference*, volume 2, pages 1215–1221 vol.2, 1995.

[16] Michael D. Seeman and Seth R. Sanders. Analysis and optimization of switched-capacitor dc–dc converters. *IEEE Transactions on Power Electronics*, 23(2):841–851, 2008.

[17] R. D. Middlebrook and Slobodan Cuk. A general unified approach to modelling switching-converter power stages. In *1976 IEEE Power Electronics Specialists Conference*, pages 18–34, 1976.

[18] Robert C.N. Pilawa-Podgurski, David M. Giuliano, and David J. Perreault. Merged two-stage power converterarchitecture with softcharging switched-capacitor energy transfer. In *2008 IEEE Power Electronics Specialists Conference*, pages 4008–4015, 2008.

[19] Yutian Lei and Robert C.N. Pilawa-Podgurski. Analysis of switched-capacitor dc-dc converters in soft-charging operation. In *2013 IEEE 14th Workshop on Control and Modeling for Power Electronics (COMPEL)*, pages 1–7, 2013.

[20] Nicolas Butzen and Michel S. J. Steyaert. Design of soft-charging switched-capacitor dc–dc converters using stage outphasing and multiphase soft-charging. *IEEE Journal of Solid-State Circuits*, 52(12):3132–3141, 2017.

[21] Nicolas Butzen and Michiel Steyaert. Design of single-topology continuously scalable-conversion-ratio switched- capacitor dc–dc converters. *IEEE Journal of Solid-State Circuits*, 54(4):1039–1047, 2019.

[22] M. Seeman. *A Design Methodology for Switched-Capacitor DC-DC Conver- ters*. PhD thesis, Berkeley University of California, Department of Electrical Engineering and Computer Science, 2009.

[23] Andrija Stupar; Timothy McRae; Nenad Vukadinovic; Aleksandar Prodic; Josh A. Taylor. Multi-objective optimization and comparison of multi-level dc-dc converters using convex optimization methods. *IEEE*, 2016.

[24] Behzad Razavi. *Design of Analog CMOS Integrated Circuits*. Electrical Engineering Series. McGraw-Hill, 2001.

[25] M.-L. Sheu; T.-W. Lin; W.-H. Hsu. Wide frequency range voltage controlled ring oscillators based on transmission gates. *IEEE, Int. Symp. Circuits Syst. (ISCAS'05)*, pages 2731–2734, May 2005.

[26] I.-C. Hwang; C. Kim; S.-M. Kang. A cmos self-regulating vco with low supply sensitivity. *IEEE J. Solid-State Circuits*, 39(1):42–48, Jan 2004.

[27] X. Zhao; R. Chebli; M. Sawan. A wide tuning range voltagecontrolled ring oscillator dedicated to ultrasound transmitter. *16th Int. Conf. Microelectron. (ICM'04)*, page 313–316, Dec. 2004.

[28] N. Gupta. Voltage-controlled ring oscillator for low phase noise application. *Int. J. Comput. Appl*, 14(5):23–27, Jan. 2011.

[29] R. A. Nicodimus; S. Takagi; N. Fujii. Wide tuning range voltagecontrolled ring oscillator. *IEICE Trans. Electron*, R86-C(6):1085–1088, Jun. 2003.

[30] F. Veirano; P. Pérez; S. Besio; P. Castro; F. Silveira. Ultra low power pulse generator based on a ring oscillator with direct path current avoidance. *IEEE 4th Lat. Amer. Symp. Circuit and Syst. (LASCAS'13)*, pages 1–4, Feb. 2013.

[31] Inhee Lee IEEE Member; Dennis Sylvester IEEE Fellow; David Blaauw IEEE Fellow. A constant energy-per-cycle ring oscillator over a wide frequency range for wireless sensor nodes. *IEEE JOURNAL OF SOLID-STATE CIRCUITS*, 51(03):697–711, 2016.

[32] M.G. Degrauwe, J. Rijmenants, E.A. Vittoz, and H.J. De Man. Adaptive biasing cmos amplifiers. *IEEE Journal of Solid-State Circuits*, 17(3):522–528, 1982.

[33] Márcio Cherem Schneider and Carlos Galup-Montoro. *CMOS Analog Design Using All-Region MOSFET Modeling*. Cambridge University Press, 2010.

[34] Hanh-Phuc Le, Michael Seeman, Seth R. Sanders, Visvesh Sathe, Samuel Naffziger, and Elad Alon. A 32nm fully integrated reconfigurable switched-capacitor dc-dc converter delivering 0.55w/mm2 at 81In *2010 IEEE International Solid-State Circuits Conference - (ISSCC)*, pages 210–211, 2010.

[35] Hans Meyvaert, Tom Van Breussegem, and Michiel Steyaert. A monolithic 0.77w/mm2 power dense capacitive dc-dc step-down converter in 90nm bulk cmos. In *2011 Proceedings of the ESSCIRC (ESSCIRC)*, pages 483–486, 2011.

[36] Hanh-Phuc Le, Seth R. Sanders, and Elad Alon. Design techniques for fully integrated switched-capacitor dc-dc converters. *IEEE Journal of Solid-State Circuits*, 46(9):2120–2131, 2011.

[37] Leland Chang, Robert K. Montoye, Brian L. Ji, Alan J. Weger, Kevin G. Stawiasz, and Robert H. Dennard. A fully-integrated switched-capacitor 2 1 voltage converter with regulation capability and 90In *2010 Symposium on VLSI Circuits*, pages 55–56, 2010.

[38] Wanyeong Jung, Sechang Oh, Suyoung Bang, Yoonmyung Lee, Zhiyoong Foo, Gyouho Kim, Yiqun Zhang, Dennis Sylvester, and David Blaauw. An ultra-low power fully integrated energy harvester based on self-oscillating switched-capacitor voltage doubler. *IEEE Journal of Solid-State Circuits*, 49(12):2800–2811, 2014.

[39] K.Krishna Reddy and Patri Sreehari Rao. A dt-mos switched-capacitor based step-up dc/dc converter for energy harvesting applications. In *2020 IEEE International Symposium on Sustainable Energy, Signal Processing and Cyber Security (iSSSC)*, pages 1–5, 2020.

[40] Huan Peng, Nghia Tang, Youngoo Yang, and Deukhyoun Heo. Cmos startup charge pump with body bias and backward control for energy harvesting step-up converters. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 61(6):1618–1628, 2014.

[41] Edi Emanovic, Joseph Shor, and Drazen Jurisic. An inverter-based, ultra-low power, fully integrated, switched-capacitor dc-dc buck converter. In *ESSCIRC 2021 - IEEE 47th European Solid State Circuits Conference (ESSCIRC)*, pages 359–362, 2021.

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