## NanoWatt, sub-nS OTAs, with sub-10mV input offset, using series-

## parallel current copiers

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## Abstract:

In this paper, series-parallel (SP) current-division will be employed for the design of very low transconductance OTAs. From the theory and measurements, it will be shown that SP mirrors allow building current copiers with copy factors of thousands, without reducing matching or noise performance. SP mirrors will be applied to the design of OTAs ranging from 33pS to a few nS, with up to 1V linear range, consuming in the order of 100nW, and with a reduced area. An integrated 3.3s time-constant integrator will also be presented. Several design concerns will be revised: linearity, offset, noise, leakages; as well as layout techniques. A final comparative analysis concludes that SP-association of transistors allows the design of very efficient transconductors, for demanding applications in the field of implantable electronics among others.

#### I Introduction:

In recent years there has been considerable research effort in the development of integrated transconductance amplifiers (OTAs), with very small transconductance and improved linear range due mainly to their application in biomedical circuits and in neural networks. Several OTA topologies have been developed to achieve transconductances in the order of a few nA/V with a linear range up to 1V or more [1–10]. However, the use of complex OTA architectures also increases noise, mismatch offset, and transistor area, and results in design trade-offs [1].

In a classical symmetrical OTA, voltage to current conversion is carried out in the input differential pair while the other transistors just copy the current to the output. Although bias current can be extremely low [11], leading to an extremely low transconductance, a drawback in this case is the poor linearity as the input transistors operate in weak inversion. In weak inversion, the range of operation of the OTA is limited to 60-70mV at the input; for greater input voltages there is a considerable distortion in the circuit. It is possible to summarize the challenge presented by the design of very low transconductance OTAs for  $G_m$ -C filters as follows: to increase linear range while preserving low noise, low offset, and a reduced area and power consumption. In [12] a tutorial focused on classic linearization techniques for OTAs is presented, while in [1] an interesting comparative study of different linearized OTAs in the nS range is shown. Although many working principles and circuit topologies have been reported for very low transconductance OTAs, a rough classification may include:

-Those circuits that modify the differential pair performing the voltage-to-current conversion in such a way as to reduce the transconductance and increase its linear range. Techniques include classic or active source degeneration [12,13], bump transistors [4], bulk or floating gate driven MOS [1], among others.

-Those circuits that use current cancellation [5], or current division [3,14] to divide the OTA transconductance by a desired factor, but do not increase the input linear range.

-Circuits using voltage division techniques for the extension of the linear range [2,7].

Of course, techniques can be combined. Regarding their limitations: modified-differential pairs increase offset, noise, and are limited to a few nS in their transconductance; a further

transconductance reduction requires the use of some kind of division scheme. Current cancellation and voltage division also show, in general, significant input offset and noise. Simple division of the output current of a differential pair by a high ratio has been widely considered an expensive technique in terms of area. But the use of series–parallel division of current [3,14] in an OTA as in Fig.1, allows the implementation of an area efficient current divider. In this paper we will examine this circuit in detail, particularly with reference to offset.

In the rest of this section, series-parallel (SP) OTAs are introduced, as well as the current based ACM MOSFET model, essential for the analysis of SP association of transistors. In section II, it is shown, from both circuit analysis, and measurements, that SP association of transistors helps in the design of current mirrors, even with copy factor of thousands, and a low current mismatch. Section III contains several SP OTA design issues: linearity, noise, offset, and leakage current effects will be examined. Section IV shows the design and measurement results for several OTAs, and a 3.3s time-constant  $G_m$ -C integrator. At the end, a comparative study of this work and others in the field of very large time constant integrated  $G_m$ -C filters is presented.

## A - Series parallel OTA

For the NMOS current mirrors in Fig.1, N unit transistors  $M_u$  are placed in-series and inparallel to achieve an effective output transconductance  $G_m$ ,

$$G_m = g_{m1}/N^2 \tag{1}$$

 $g_{m1}$  is the gate transconductance of the transistors M<sub>1</sub>. Using this technique, a 33 pS transconductor with a ±150mV linear range has been previously demonstrated [14]. To enhance linearity, a modified differential input pair as shown in Fig.2 [13] can substitute M<sub>1</sub> in Fig.1. The effective transconductance  $g_{m\_eff}$  of the pair in Fig.2 to substitute  $g_{m1}$  in (1) is calculated by small signal analysis, assuming that transistors M<sub>4</sub> operate in the linear region, each behaving as a resistor of value 2*R*. Therefore:

$$g_{m_{eff}} = \frac{g_{m1}}{1 + ng_{m1}R}$$
(2)

n is the slope factor [15-16], slightly greater than unity and weakly dependent on the gate voltage.

The current copiers of Fig.1 are not only area-efficient because their area is proportional to the square root of the copy factor, but are also mismatch-efficient because they benefit from the improved matching of a large number of equal unit transistors. With the appropriate placement, the designer can apply the most usual matching rules to  $M_{2A}$ - $M_{2B}$ , and  $M_{2C}$ - $M_{2D}$ : common centroid geometry, and same surroundings; even while using copy factors as large as thousands if for example N=50 or N=100 are selected. To preserve mismatch benefits while using moderate copy factors, the current mirror in Fig.3 can be used.

## **B** - The ACM model

For the theoretical deductions and simulations, the one-equation-all-region MOSFET model of [15,16] is employed because it allows an accurate representation of the series-parallel association. In the ACM model, the drain current  $I_D$  is expressed as the difference between the forward ( $I_F$ ) and reverse ( $I_R$ ) components

$$I_{D} = I_{F} - I_{R} = I(V_{G}, V_{S}) - I(V_{G}, V_{D}) = I_{S}(i_{f} - i_{r})$$
(3)

$$I_{S} = \frac{1}{2} \mu C_{ox}^{'} n \phi_{t}^{2} \left( W/L \right)$$

$$\tag{4}$$

 $I_s$  is the specific current, which is proportional to the aspect ratio W/L of the transistor.  $V_G$ ,  $V_S$ , and  $V_D$  are the gate, source, and drain voltages, with reference to the substrate. Here,  $\mu$  is the effective mobility,  $\phi_t$  is the thermal voltage, and  $C'_{ox}$  is the gate oxide capacitance per unit area. Parameters  $i_f$  and  $i_r$  are the normalized forward and reverse currents, or inversion levels at source and drain, respectively. Note that, in the saturation region, the drain current is almost independent of  $V_D$ ; therefore,  $i_f >> i_r$  and  $I_D \cong I_F$ . On the other hand, if  $V_{DS}$  is low (linear region), then  $i_f \cong i_r$ . The inversion level  $i_f$  ( $i_r$ ) represents the normalized carrier charge density at the MOSFET source (drain)  $Q'_{IS}$ ,  $Q'_{ID}$ .

The small signal transconductances  $g_m, g_{ms}, g_{md}$  (gate, source, and drain transconductances) are given by [15,16]

$$g_{ms} = -\mu \frac{W}{L} Q_{IS} = \frac{2I_S}{\phi_t} \left( \sqrt{1 + i_f} - 1 \right)$$
(5)

$$g_{md} = -\mu \frac{W}{L} Q'_{ID} = \frac{2I_s}{\phi_t} \left( \sqrt{1 + i_r} - 1 \right)$$
(6)

$$g_m = \frac{\left(g_{ms} - g_{md}\right)}{n} \tag{7}$$

The other small signal parameters can also be given in terms of the inversion levels. See for example [15] for intrinsic capacitances, and [14] for linearity. Recently, noise [17] and mismatch [18] models have also been introduced in terms of the inversion levels.

From now on, for a given transistor  $M_X$  (either composite or not), its gate, source, drain transconductances, drain current, inversion level, threshold voltage standard deviation (SD), current factor SD, aspect ratio, and gate area will be noted by  $g_{mX}, g_{msX}, g_{mdX}, I_{DX}, i_{fX}, \sigma_{V_TX}^2, \sigma_{\beta X}^2, (W/L)_X, (WL)_X$ , respectively.

## II Series parallel current division/multiplication and mismatch.

It is widely recognized that the performance of most analog or even digital MOS circuits is limited by random mismatch between transistors. Matching can be modeled by the random variations in geometric, process, and/or device parameters. The approach most employed by designers is to consider only variations in the threshold voltage  $V_T$ , and the current factor  $\beta = \mu C'_{ox} W/L$ . Thus the threshold voltage and current factor of each one in a small -may be only two-, or large group of matched transistors, will not be exactly the same. In this work  $\Delta V_T$  and  $\Delta \beta$ , will note fluctuations measured with respect to the average threshold voltage  $\overline{V_T}$ , and average current factor  $\overline{\beta}$ , of the group of matched transistors. For each unit transistor M<sub>X</sub> in the group,  $V_{TX} = \overline{V_T} + \Delta V_{TX}$ ;  $\beta_X = \overline{\beta} + \Delta \beta_X$ . Fluctuations in  $V_T$ ,  $\beta$ , can be seen as random variations with a normal distribution and a SD given by [19, 20]:

$$\sigma_{V_T}^2 = \frac{A_{V_T}^2}{2WL}, \quad \frac{\sigma_{\beta}^2}{\beta^2} = \frac{A_{\beta}^2}{2WL}$$
(8)

In (8)  $A_{VT}$ ,  $A_{\beta}$ , are two technology parameters with typical values of  $A_{VT}$ =13-30mV.µm and  $A_{\beta}$ =2-4%.µm [20]. In analog design it is common to express mismatch in terms of  $\delta V_T$ ,  $\delta \beta$ , the difference between  $V_T$ ,  $\beta$ , of two adjacent transistors, thus  $\sigma_{\delta V_T}^2 = 2\sigma_{V_T}^2$ ,  $\sigma_{\delta\beta}^2 = 2\sigma_{\beta}^2$  [20].

Series-parallel association of MOS transistors [21], is a useful circuit technique and can be used to obtain improved matching between devices [22]. In Fig.4(a) two transistors  $M_{S(D)}$ , are series connected; the equivalent aspect ratio  $(W/L)_{eq}$  of the composite transistor is [21]:

$$\left(\frac{W}{L}\right)_{eq} = \frac{\left(W/L\right)_{S} \cdot \left(W/L\right)_{D}}{\left(W/L\right)_{S} + \left(W/L\right)_{D}}$$
(9)

Eq.(9) may be extended to complex combinations of unit transistors to obtain different equivalent transistor geometries. For example, Fig.4(c) shows measured drain current vs. drain voltage for two equivalent transistors: a single unit sized  $(W/L)_u = 4\mu m/10\mu m$ , and a  $10\times10$  array of the same transistor (Fig.4(b)). The two plots are similar, but note in the upper detail that the drain-source impedance  $r_{ds}$  is much higher in the case of the composite transistor. As a rule of thumb, the output conductance of a given composite transistor will be inversely proportional to the equivalent channel length [16, 21].

The copy factor M in a current mirror is calculated as the ratio between the aspect ratios of transistors, even if  $M_A$ ,  $M_B$  are two transistor arrays. Using (9), in the mirror of Fig.3:

$$\frac{I_{In}}{I_{Out}} = \frac{S.P}{R.Q} = M \tag{10}$$

where P, R, Q, and S are the number of unit transistors in series or in parallel in each branch.

Classic current mirrors with a copy factor M>>1 - as in Fig.5(a) - are very sensitive to mismatch offset because at the output there is a single transistor M<sub>B</sub>, with a reduced area that according to (8) presents high variations  $\Delta\beta_{Bj}$ ,  $\Delta V_{TB}$ , in its threshold voltage and current factor. On the other branch, fluctuations  $\Delta\beta_{aj}$ ,  $\Delta V_{Taj}$  (see fig.5(a)) have less impact on the output current because they are non-correlated so their effect is averaged. The composite transistors of Fig.5(b), and Fig.5(c), can be used to implement a current mirror with a copy factor  $M=N^2$ , but using the same number of unit transistors at both input and output branches of the mirror. A better matching and a reduction in random offset are expected if usual layout matching rules are followed, because a large number of unit transistors have been matched together. In this way, common centroid layout geometry is possible, even for matching composite transistors with very different aspect ratios.

#### A Mismatch calculation in a SP mirror.

Even with a careful layout, fluctuations  $\Delta \beta_{a(b)ij}$ ,  $\Delta V_{Ta(b)ij}$ , of each unit transistor  $M_{a(b)_{i,j}}$  in Fig.3 produce an output current error term  $\Delta I_{Out}$ ; thus  $I_{Out} = I_{In}/M + \Delta I_{Out}$ . The designer who normally has an equation for mismatch between identical unit transistors- requires a formula to estimate the standard deviation of  $I_{Out}$ . The calculation is immediate when using (8), if the model in (8) is series-parallel consistent, because the composite transistors  $M_A$ ,  $M_B$ , have an area *RS*, and *PQ* times respectively larger than the unit transistor. In effect, assuming known values for the SD in current factor and threshold voltage of composite transistors  $M_A$ ,  $M_B$  of Fig.3:

$$\sigma_{I_{Out}}^{2} = \frac{g_{mB}^{2} I_{In}^{2}}{g_{mA}^{2}} \left( \frac{\sigma_{\beta}^{2}}{\beta^{2}} \right)_{A} + I_{Out}^{2} \left( \frac{\sigma_{\beta}^{2}}{\beta^{2}} \right)_{B} + \frac{g_{mB}^{2} I_{In}^{2}}{g_{mA}^{2}} \cdot \sigma_{V_{T}A}^{2} + g_{mB}^{2} \cdot \sigma_{V_{T}B}^{2}$$
(11)

Eq.(11) has been derived propagating to  $I_{Out}$ , the effect of non-correlated fluctuations  $\Delta \beta_A$ ,  $\Delta V_{TA}$ ,  $\Delta \beta_B$ ,  $\Delta V_{TB}$ . Using (8) in (11):

$$\left(\frac{\sigma_{I_{Out}}^2}{I_{Out}^2}\right) = \left(\frac{1}{RS} + \frac{1}{PQ}\right) \left[\left(\frac{\sigma_{\beta}^2}{\beta^2}\right)_u + \frac{g_{mB}^2}{I_{Out}^2} \left(\sigma_{V_T}^2\right)_u\right]$$
(12)

 $(\sigma_{\beta}^2/\beta^2)_u$ ,  $(\sigma_{\nu_{\tau}}^2)_u$ , are the SD of threshold voltage and current factor for unit transistors. This equation relating the mismatch of a SP mirror to that of unit transistors is general; a careful derivation of (12) that does not assume the model in (8) is presented in the appendix. The designer can use any mismatch model to calculate  $(\sigma_{\beta}^2/\beta^2)_{\mu}$ ,  $(\sigma_{\nu_{\tau}}^2)_{\mu}$  in (12). In the example of Fig.5, three different topologies for a current mirror to perform a M:1 current copy are shown. For a 100:1 copy, the circuit in Fig.5(a) requires 101 unit transistors, the one in Fig.5(b) only 20, and 200 are required for the circuit in Fig.5(c). standard deviation From (12),the in output current fluctuation is  $(\sigma_{I_{out}}^2/I_{Out}^2)_{(a)} \approx 5(\sigma_{I_{out}}^2/I_{Out}^2)_{(b)} \approx 50(\sigma_{I_{out}}^2/I_{Out}^2)_{(c)}$ . In Fig.6 calculated and measured  $I_{out}$ ,  $\sigma_{Iout}^2/I_{out}^2$  in terms of the input current are shown for a 100:1 NMOS current mirror with the topologies of Fig.5(a) and Fig.5(c) (N=10). The  $\sigma_{lout}^2$  value was obtained from 10 samples of the circuit of the same batch in 0.8µm technology. Unit transistors were sized

 $(W/L)_u = 4\mu m/12\mu m$ , and previously adjusted values for the target technology  $A_{VT} = .03 V \mu m$ ,  $A_{\beta} = .02 \mu m$ , were used for theoretical offset calculation with (8) and (12). A major conclusion is that  $\sigma_{Iout}^2/I_{Out}^2$  has been substantially reduced in SP mirrors.

#### III On the design of SP very low transconductors

To complete the design of the SP OTAs, some other circuit properties should be studied.

### A Linearity

Linearity in Fig.1 can be calculated in terms of the inversion level  $i_{f1}$  of the input differential pair. The expression is [14]:

$$V_{Lin} = 2n\phi_t \sqrt{\frac{6\alpha(1+i_{f1})^{\frac{3}{2}}}{3(1+i_{f1})^{\frac{1}{2}} - 1}}$$
(13)

where  $V_{Lin}$  is the input linear range defined in terms of an acceptable error  $\alpha$ . Linearity is further extended in the case of the input topology in Fig.2 [13] or others ([4] for example).

# **B** Offset in the OTA:

The input pair  $M_1$ , PMOS current mirror transistors  $M_3$ , and SP current dividers (12), contribute to offset in the OTA of Fig.1. Summing their input referred contribution:

$$\sigma_{V_{off}}^{2} = 2 \left[ \left( \sigma_{V_{T}}^{2} \right)_{1} + \frac{I_{D1}^{2}}{g_{m1}^{2}} \left( \frac{\sigma_{\beta}^{2}}{\beta^{2}} \right)_{1} \right] + \frac{4I_{D1}^{2}}{N \cdot g_{m1}^{2}} \left[ \frac{g_{m2B}^{2}}{I_{D2B}^{2}} \left( \sigma_{V_{T}}^{2} \right)_{u} + \left( \frac{\sigma_{\beta}^{2}}{\beta^{2}} \right)_{u} \right] + \frac{2I_{D1}^{2}}{g_{m1}^{2}} \left[ \frac{g_{m3}^{2}}{I_{D3}^{2}} \left( \sigma_{V_{T}}^{2} \right)_{3} + \left( \frac{\sigma_{\beta}^{2}}{\beta^{2}} \right)_{3} \right]$$

$$(14)$$

In the case of the linearized pair in Fig.2, transistors  $M_4$  do not introduce offset because  $M_4$  source-drain voltage is zero at  $V_{in}=0$ . But an extra offset is introduced by the current mirror  $M_5$  and the effect of fluctuations in  $M_{1A(B)}$  is slightly different. A new expression for offset is derived with a small signal analysis:

$$\sigma_{V_{in}}^{2} = 2 \left[ \left( \sigma_{V_{T}}^{2} \right)_{1} + \frac{I_{D1}^{2}}{g_{m1}^{2}} \left( \frac{\sigma_{\beta}^{2}}{\beta^{2}} \right)_{1} \right] + \frac{4I_{D1}^{2}}{N \cdot g_{m_{-}eff}^{2}} \left[ \frac{g_{m2B}^{2}}{I_{D2B}^{2}} \left( \sigma_{V_{T}}^{2} \right)_{u} + \left( \frac{\sigma_{\beta}^{2}}{\beta^{2}} \right)_{u} \right] + \dots$$

$$\dots + 2 \frac{I_{D1}^{2}}{g_{m_{-}eff}^{2}} \left[ \frac{g_{m3}^{2}}{I_{D3}^{2}} \left( \sigma_{V_{T}}^{2} \right)_{3} + \left( \frac{\sigma_{\beta}^{2}}{\beta^{2}} \right)_{3} \right] + 2 \left[ \frac{g_{m5}^{2}}{g_{m_{-}eff}^{2}} \left( \sigma_{V_{T}}^{2} \right)_{5} + \frac{I_{D5}^{2}}{g_{m_{-}eff}^{2}} \left( \frac{\sigma_{\beta}^{2}}{\beta^{2}} \right)_{5} \right]$$

$$(15)$$

Expressions (14), (15), can be extended to generic series-parallel current division of Fig.3 changing N by  $\sqrt{SP/RQ}$ .

## **C** Noise Analysis

Using the consistent thermal and flicker noise models of [17], the output current noise of the mirror in Fig.3 is calculated:

$$\frac{S_{I_{Out}h}}{I_{Out}^2} \approx 2nk_B T\left(\frac{g_{mB}}{I_{Out}}\right)\left(\frac{1}{I_{In}} + \frac{1}{I_{Out}}\right)$$
(16)

$$\frac{S_{I_{Out}\frac{1}{f}}}{I_{Out}^{2}} = \frac{q^{2}N_{otN}}{nC_{OX}^{'2}(WL)_{u}} \left(\frac{1}{RS} + \frac{1}{PQ}\right) \cdot \frac{g_{mB}^{2}}{I_{out}^{2}} \cdot \frac{1}{f}$$
(17)

 $S_{I_{Out}th}, S_{I_{Out}\frac{1}{f}}$ , are thermal and flicker noise Power Spectral Densities (PSD),  $k_B$  is the Boltzmann's constant, *T* is the absolute temperature,  $N_{otN(P)}$  are technology parameters for the flicker noise, *q* is the electron charge. Note that the output noise (like offset) does not significantly increase when using large SP current dividers. The input referred noise can be calculated for the OTA in Fig.1 using (16, 17). It is assumed that M >> 1 and that  $M_{2B(D)}, M_3$  are in weak inversion. Thermal  $-v_{input_t}^2$ , and flicker  $-v_{input_f}^2$  - input referred noise in the OTA are:

$$v_{input\_th}^2(f) \approx \frac{4nk_BT}{G_m}\eta$$
<sup>(18)</sup>

$$v_{input_{f}}^{2}(f) \approx \frac{2nk_{B}T}{N^{*}C_{ox}^{'}} \left[ \frac{N_{otP}}{(WL)_{1}} + \eta^{2} \left( \frac{2N_{otN}}{N(WL)_{u}} + \frac{N_{otP}}{(WL)_{3}} \right) \right] \frac{1}{f}$$
(19)

The factor  $\eta = (\sqrt{1 + i_{f1}} + 1)$ , and  $(WL)_1, (WL)_u, (WL)_3$ , are the gate area of M<sub>1</sub>, M<sub>u</sub>, and M<sub>3</sub>, respectively. Expressions (18), (19) are very similar to that obtained for a simple

symmetrical OTA, but here we are paying a price in noise for the linearization represented by the factor  $\eta$ . As in (15), these expressions can be extended to calculate input noise in OTAs using the pair of Fig.2.

## **D** - What is the minimum effective G<sub>m</sub> possible with this technique?

The output branch in Fig.1 may be biased with a current as low as a few pA or less; the only limitation being the sum of the leakage current at the source (drain) of each series transistor in  $M_{2B(D)}$ . In the target technology - as well as others examined - leakages in p-doped diffusions are much higher than those in an n-doped diffusion. For this reason all the presented OTAs include a PMOS differential pair, and NMOS series-parallel current mirrors. From manufacturer's data, estimated leakage current in a single source(drain) was  $I_{leak}$ =3fA for a 4µm x 2µm n+ diffusion. The selected design criterion is that the leakages should be at least 10 times less than the bias current in the output branch of the current mirror:

$$\sum I_{leak} = N.I_{leak} < \frac{I_{D1}}{10N^2}$$
(20)

which imposes a limit on the minimum achievable transconductance  $G_{mmin}$ . A 15pS value (equivalent to a 60G $\Omega$  resistor) was estimated for N=100 and  $(g_m/I_D)_1 = 5$  at the input pair, that is -although reasonable- an arbitrary worst case condition. A non-arbitrary limit for the minimum achievable transconductance should be examined according to specific restrictions in area, power consumption, and linear range (for example if no restrictions apply, the bias current can be selected as low as necessary to achieve an extremely low transconductance in detriment to the linear range). Using (4) it is possible re-write (20):

$$G_{m\min}^{3/2} > 10.(g_m/I_D)_1^{3/2}.I_{leak}.\sqrt{I_{D1}}$$
(21)

Consider the design of a transconductor with a specified minimum input linear range. Because in a differential pair the linear range is a function of the inversion level (13), the latter is fixed. A fixed  $i_{fl}$  in the moderate or strong inversion region (for an enhanced linearity), limits the minimum bias current because an arbitrary large transistor cannot be realized. Thus, examining (21), the minimum  $G_m$  value is a function of the circuit topology, desired linear range, and available transistor area.

#### IV Designed OTAs and layout techniques.

Several low and very low transconductance OTAs named  $G_{m1}$  to  $G_{m4}$ , were fabricated for test purposes. The basic design methodology is that proposed in [14] where the designer starts with a required transconductance  $G_m$  and linear range  $V_{Lin}$ . Non idealities like noise and offset are addressed using (14) to (19) depending on the topology of the input pair.

 $G_{m1}$  is a 35pS, 160mV linear range OTA. It uses a  $g_{m1}$ =170nS differential input pair in the configuration of Fig.1, with an  $N^2$ =4900 division factor.  $G_{m2}$ =2.35nS requires also a 160mV linear range so the differential pair of  $G_{m1}$  is reused with a 9:1 division factor obtained with the topology of Fig.3 using P=8, Q=2, R=1, S=18.  $G_{m3}$ ,  $G_{m4}$  are both 500mV linear range OTAs with transconductances of 2.6nS, and 90pS respectively. A differential pair, like in Fig.2 with  $g_{m_eff}$  = 69nS is employed with 28:1, and 784:1 division factors. In the former P,Q,R,S = 28,1,5,5 and the latter employs 28 parallel transistors copying to 28 series transistors in the current divider. Table I resumes several design characteristics of the OTAs.

#### A Layout techniques

A careful layout plays a central role in obtaining a reduced mismatch. The layout structure used for matched transistors, whether differential pair or series-parallel current mirrors, was in all cases the same: a large row of equal sized transistors placed together at minimum distance, and then connected with metal wires. The layout technique can be seen in Fig.7, corresponding to  $G_{m2}$ . Particular care was taken to ensure that :

- When matching two arrays  $M_A$ ,  $M_B$ , of transistors, if one unit transistor of the row corresponds to  $M_A$ , their neighbors correspond to  $M_B$ . If more than two arrays are being matched together, unit transistors are also interleaved.

- Current flow direction is always the same in unit transistors and the usual dummy structures at row ends were incorporated. Symmetry between adjacent transistors is preserved as much as possible even in the layout of the metal wires. This can be observed in the magnified zone of Fig.7 showing NMOS unit transistors of the 4900 division factor SP mirror.

- No minimum size transistors are employed. Minimum allowed distance is preserved between unit transistors.

The row structure has the following advantages:

- A minimum extra space is used since only two dummies are required to obtain the same surroundings for all unit transistors. The gate-to-silicon area ratio is between 10 to 20% for  $G_{m1}$  to  $G_{m4}$ .
- Layout blocks are easily re-usable since transistor rows can be employed in current mirrors with widely different copy factors, or in a differential pair whether linearized or not, just by changing metal wire connections.
- When matching transistor arrays, common centroid geometry is preserved if each array contains the same number of interleaved unit transistors, regardless of the way they are connected.

## **B** Measurement results:

Several measured characteristics of  $G_{m1}$  to  $G_{m4}$  are summarized in Table 2, while in Figs.8, 9 the measured transfer function of  $G_{m3}$ , and  $G_{m4}$  is shown. Linearity  $V_{Lin}$  was measured for a 5% error [14]. The reduced input offset of the OTAs, obtained with a moderate area and nano-power consumption even for  $G_{m6}$  of 89nS with a ±500mV linear range, should be highlighted. Ten circuit samples from the same batch were used to calculate  $\sigma_{Voff}$  in Table 2. The transfer functions of  $G_{m1}$ , and  $G_{m3}$  were directly measured using an HP4155 semiconductor parameter analyzer, while the transfer functions of  $G_{m2}$ , and  $G_{m4}$ , and noise measurements employ the technique described in [11]. Noise figures correspond to the input referred rms voltage integrated in the band from .3 to 10Hz where OTAs are intended to operate.

A 3.3s time constant integrator, using  $G_{m6}$  and a 50pF capacitor was also fabricated. The integrator occupies a  $0.2mm^2$  area. An independently powered unit gain buffer was also incorporated to drive the output pad. The plot of Fig.10 shows the measured transient response of the circuit to a large  $1V_{pp}$  square wave at the input. The plot in Fig.11 shows the frequency response of a low pass filter based on the integrator. The 3dB decay was measured at 0.302 Hz.

### V A comparative survey

As indicated in the introduction, several very low transconductors and large time constant  $G_m$ -C filters have been reported. In [4], Sharpeskar et al combine at the input, gate degeneration, bulk driven transistors, and the so called bump transistor technique, to achieve a transconductor of 10nS with a linear range of ±1.7V, a less than 20mV input offset and a 1µW power consumption. In [1] several 10nS, sub-µW OTAs using different input pair linearization techniques are compared; unfortunately no offset measurements are presented. These OTAs require the addition of some kind of division technique –like the one here presented- to achieve few Hz or sub-Hz range  $G_m$ -C filters. Techniques may include voltage attenuation [2,7], capacitor scaling [9,23], or current division/cancellation [3,5]. Table 3 gives some previously reported very large time constant integrators and filters, all of them incorporating some kind of division scheme. Although the comparative study is difficult because linearity, noise, and particularly, offset, are not always measured in the same way, it is possible to conclude that the technique here presented is very efficient regarding mismatch, power consumption, and noise, without a significant overhead in silicon area.

### **VI Conclusions:**

A general expression was introduced, to estimate mismatch offset in series-parallel current mirrors. Extremely large current multiplication (division) factors can be obtained by means of SP mirrors, without a significant loss in terms of area, offset, or noise. Series-parallel division of current was applied in symmetrical OTAs to achieve very low transconductances with extended linear range. Sample OTAs ranging from 35pS to 2.8nS, and a 3.3s time constant  $G_m$ -C integrator were designed, fabricated, and tested. The designed circuits demonstrate a very good trade-off in terms of occupied area, power consumption, linearity, noise, and input offset. All the OTAs consume around 100nW power, and have a measured input referred offset standard deviation of less than 10mV.

## Appendix

In this appendix, small signal analysis is carried out for  $V_T$ ,  $\beta$  fluctuations in all individual transistors of the circuit in Fig.3. Firstly, consider in Fig.12, a composed transistor  $M_X$  formed by a large number *P* of series-stacked unit transistors  $M_{ui}$ .  $\Delta V_{Ti}$ ,  $\Delta \beta_i$  fluctuations on unit transistors affect the drain current  $I_{Di}$  and their node voltages. For each  $M_{ui}$  it is possible to write:

$$\Delta I_{Di} = \frac{\partial I_{Di}}{\partial V_{Ti}} \Delta V_{Ti} + \frac{I_{Di}}{\beta_i} \Delta \beta_i + \frac{\partial I_{Di}}{\partial V_{Si}} \Delta V_{Si} + \frac{\partial I_{Di}}{\partial V_{Di}} \Delta V_{S(i-1)}$$
$$= -g_{m_i} \Delta V_{Ti} + \frac{I_D}{\beta_i} \Delta \beta_i - g_{ms_i} \Delta V_{Si} + g_{md_i} \Delta V_{S(i-1)}$$
(22)

where  $g_{m_i}, g_{ms_i}, g_{md_i}$  are gate, source, and drain transconductances of M<sub>ui</sub>, respectively. (22) has been derived for a generic transistor but  $\Delta I_{Di} = \Delta I_D$  is constant, because the transistors are series connected. Also, because transistors are series connected  $Q'_{ID_i} = Q'_{IS_{(i-1)}}$  then  $g_{ms_{(i-1)}} = g_{md_i}$  from (4), (5). Summing (22) for all the series transistors:

$$P\Delta I_D = \sum_{i=1}^{P} I_D \frac{\Delta \beta_i}{\beta} - \sum_{i=1}^{P} g_{m_i} \Delta V_{Ti}$$
(23)

Assuming that  $\Delta V_{Ti}, \Delta \beta_i$  are non-correlated, and that  $\sigma_{\beta_i}^2, \sigma_{V_Ti}^2$  do not depend on *-i*- we obtain:

$$\sigma_{\Delta I_D}^2 = \frac{I_D^2}{P} \cdot \left(\frac{\sigma_{\beta}^2}{\beta^2}\right)_u + \frac{\left(\sigma_{V_T}^2\right)_u}{P^2} \cdot \sum_{i=1}^P g_{m_i}^2 \approx \frac{I_D^2}{P} \cdot \left(\frac{\sigma_{\beta}^2}{\beta^2}\right)_u + \frac{g_{mX}^2}{P} \left(\sigma_{V_T}^2\right)_u$$
(24)

The result of the sum in (24) is not exact, it uses  $\sum_{i=1}^{P} g_{m_i}^2 \approx P \cdot g_{mX}^2$ . This approximation assumes  $P = \infty$  differential-length series transistors, and the integration procedure, and approximations in [24]:

$$\sum_{i=1}^{P} g_{m_{i}}^{2} \approx \frac{P}{L} \int_{0}^{L} g_{m}^{2}(x) dx = \frac{P \cdot \mu W I_{D} C_{ox}^{'}}{nL} \int_{Q_{IS}^{'}}^{Q_{ID}} \frac{1}{n C_{ox}^{'} \phi_{l} - Q_{I}^{'}} dQ_{I}^{'} \approx P \cdot g_{mB}$$
(25)

If a  $P \times Q$  transistor array like the M<sub>B</sub> in Fig.3 is now introduced, fluctuations are calculated summing (24) for the parallel branches;  $g_{mB} = Q.g_{mX}$  and drain current is Q times larger:

$$\sigma_{I_D}^2 = \frac{I_D^2}{PQ} \cdot \left(\frac{\sigma_{\beta}^2}{\beta^2}\right)_u + \frac{g_{mB}^2}{PQ} \left(\sigma_{V_T}^2\right)_u$$
(26)

Drain current is fixed in M<sub>A</sub> of Fig.3, so eq.(26) could be better expressed in this case, as a fluctuation in  $V_G$ :

$$\sigma_{V_G}^2 = \frac{I_{in}^2}{g_{mA}^2 \cdot RS} \cdot \left(\frac{\sigma_{\beta}^2}{\beta^2}\right)_u + \frac{1}{RS} \left(\sigma_{V_T}^2\right)_u$$
(27)

This  $V_G$  fluctuation is then propagated to the output through M<sub>B</sub>. Also, (26) should be summed to calculate total output current SD in Fig.3.

$$\frac{\sigma_{I_{Out}}^2}{I_{out}^2} = \frac{g_{mB}^2 I_{in}^2}{g_{mA}^2 PQ} \left(\frac{\sigma_{\beta}^2}{\beta^2}\right)_u + \frac{g_{mB}^2}{PQ} \left(\sigma_{V_T}^2\right)_u + \frac{I_{in}^2}{RS} \left(\frac{\sigma_{\beta}^2}{\beta^2}\right)_u + \frac{g_{mB}^2}{RS} \left(\sigma_{V_T}^2\right)_u$$
(28)

Because M<sub>A</sub>, M<sub>B</sub> have the same specific current then  $g_{mA}/I_{In} = g_{mB}/I_{Out}$  [20]. It follows that:

$$\left(\frac{\sigma_{I_{Out}}^2}{I_{Out}^2}\right) = \left(\frac{1}{RS} + \frac{1}{PQ}\right) \left[\left(\frac{\sigma_{\beta}^2}{\beta^2}\right)_u + \frac{g_{mB}^2}{I_{Out}^2} \left(\sigma_{V_T}^2\right)_u\right]$$
(29)

It should be pointed out that the derivation of (29) does not assume a specific mismatch model for the MOS transistor. Either another expression for  $(\sigma_{\beta}^2/\beta^2)_u$ ,  $(\sigma_{\nu_T}^2)_u$  can be used instead of (8), or the development in the appendix can be extended to a mismatch model that considers fluctuations in other transistor parameters such as those proposed in the references [25, 26].

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#### Figure & Table Captions:

**Fig.1:** PMOS-input symmetrical OTA with series-parallel current division to reduce transconductance without loss in linear range.

**Fig.2:** Active linearization of a differential pair to enhance linearity;  $I_A - I_B = g_{m_e eff} (V_{in}^+ - V_{in}^-).$ 

**Fig.3:** Generic SP current mirror.  $P \times Q$  unit transistors M<sub>b</sub>, and  $R \times S$  unit transistors M<sub>a</sub>, are series-parallel connected at the output and input branch respectively. Unit transistors are identical  $M_a \equiv M_b = M_u$  to achieve an effective copy factor M = S.P/Q.R. Each M<sub>a</sub>, M<sub>b</sub> in a generic position  $i_{,j}$  in the array show a fluctuation  $\Delta \beta_{a(b)ij}$ ,  $\Delta V_{Ta(b)ij}$  resulting in a current mismatch  $\Delta I_{Out}$ .

**Fig.4:** (a) Two series-connected transistors and their equivalent. (b) A single  $M_u$  transistor is equivalent to a 10×10  $M_u$  array. (c) Measured  $I_D$ - $V_D$  curves at different gate voltage  $V_G$  for single  $M_u$  sized  $(W/L)_u = 4\mu m/12\mu m$ , and a 10×10  $M_u$  array. At the top, saturation region is magnified for  $V_G$ =4V to observe the change in  $r_{ds}$ .

**Fig.5:** Three *M*:1 current copiers. (a) Classic: *M* unit transistors in parallel, copy to a single unit transistor M<sub>B</sub>. (b)  $N = \sqrt{M}$  parallel transistors, copy to *N* series-stacked ones. (c) *M* parallel unit transistors, copy to a  $N \times N$  array. All unit transistors M<sub>a</sub>=M<sub>b</sub>=M<sub>u</sub> are sized  $(W/L)_u$ .

**Fig.6:** Calculated and measured  $I_{out}$ ,  $\sigma_{Iout}^2/I_{out}^2$  in terms of the input current are shown for a 100:1 NMOS current mirror with the topologies of Fig.5(a) (*M*=100) and Fig.5(c) (*M*=100, *N*=10).  $\sigma_{Iout}^2$  value was obtained from 10 samples of the circuit of the same batch.

Fig.7: Layout picture of G<sub>m2</sub>.

Fig.8: Measured transfer characteristic of G<sub>m3</sub>.

Fig.9: Measured transfer characteristic of G<sub>m4</sub>.

Fig.10: Measured transient response of a 3.3s time-constant integrator with a large  $1V_{pp}$  square wave at the input.

Fig.11: Measured transfer function of the 3.3s time constant integrator.

Fig.12: A number –*P*- of series-stacked unit transistors.

**Table 1:** Several design characteristics of fabricated SP OTAs: input pair transconductance,

 division factor, divider unit transistor size, area, and power consumption.

**Table 2:** Several characteristics of fabricated OTAs: transconductance predicted-measured, measured linearity, predicted-measured input offset SD, maximum measured offset (10 circuit samples), predicted – measured input referred noise in the band from .3 - 10Hz.

**Table 3:** A comparative table of several reported division techniques used in very low transconductance OTAs, and large time constant  $G_m$ -C filters.



Fig.1







Fig.3



Fig.4





Fig.5



Fig.6



Fig.7



Fig.8



Fig.9



Fig.10



Fig.11



Fig.12

| ΟΤΑ             | G <sub>m_pair</sub> [nS] | M (P-Q-R-S)      | W <sub>u</sub> /L <sub>u</sub> [μm/μm] | Area [mm <sup>2</sup> ] | Power [nW] |
|-----------------|--------------------------|------------------|--|-------------------------|------------|
| G <sub>m1</sub> | 174                      | 72 (2-8-1-18)    | 4/4                                    | 0.04                    | 116        |
| G <sub>m2</sub> | 174                      | 4900 (70-1-1-70) | 4/8                                    | 0.09                    | 113        |
| G <sub>m3</sub> | 69                       | 28 (5-5-1-28)    | 4/12                                   | 0.15                    | 118        |
| G <sub>m4</sub> | 69                       | 784 (28-1-1-28)  | 4/12                                   | 0.15                    | 113        |

# Table.1

| ΟΤΑ             | Transc.       | Linearity[mV] | Offset [mV] | Offset <sub>max</sub> [mV] | Noise [µV <sub>rms</sub> ] |
|-----------------|---------------|---------------|-------------|----------------------------|----------------------------|
| G <sub>m1</sub> | 2.4nS - 2.6nS | ±160          | 8.0 - 4.4   | 8.3                        | 48 - 89                    |
| G <sub>m2</sub> | 35pS - 33pS   | ±160          | 5.4 - 2.1   | 4.0                        | 193 –160                   |
| G <sub>m3</sub> | 2.4nS - 2.8nS | ±550          | 8.8 - 9.1   | 21                         | 56 - 108                   |
| G <sub>m4</sub> | 89pS - 100pS  | ±500          | 9.0 - 6.8   | 12                         | 190 – na                   |

# Table.2

| Technique         | Ref.      | <b>Division Factor</b> | Offset           | Comments   |
|-------------------|-----------|------------------------|------------------|--|
|                   |           | & Time contant.        |                  |  |
| SP Current        | This work | 70 to 4900             | 2 to 9mV         | Low input noise, good linearity,                 |
| Division          |           | 3.3s                   | SD               | nW power.  |
| Voltage           | [2]       | Up to 10000            | Very             | Poor linearity, small silicon area, nW           |
| Division          |           | 10s                    | large.           | power.   |
| SP Current        | [3]       | 2200                   | 130mV            | Large offset probably due to non-                |
| Division          |           | 0.7s                   |                  | symmetrical SP copy.                             |
| Capacitive        | [6]       | 1.2                    | ~20mV            | 4 <sup>th</sup> order, .1-5Hz tunnable band-pass |
| Scaling & Others. |           | 1.28                   |                  | filter. ~25µW power.                             |
| Current           | [5]       | 1000                   | $40 \text{mV}^*$ | 10pF capacitors employed.                        |
| Div./Canc.        | _         | 100ms                  |                  | *random offset + 80mV systematic.                |

# Table.3