Consistent Noise Models for Analysis and Design of CMOS Circuits

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***Abstract*—Simple, physics-based MOSFET noise models, valid over the linear, saturation, and subthreshold operation regions are presented. The consistency of the models representing series–par- allel associations of transistors is verified. Simple formulas for hand analysis using the inversion level concept are developed. The proportionality between the flicker noise corner frequency and the transistor transition frequency is proved and experimentally verified under wide bias conditions. Application of the noise models to a low-noise design is shown.**

***Index Terms*— $1/f$ noise, compact modeling, low-noise design, MOSFET, noise.**

I. Introduction

MOSFET flicker or $1/f$ noise has been extensively studid because it dominates low-frequency noise and there is an increasing need to accurately design low-noise analog circuits in CMOS technology. There is still a controversy regarding the origin of MOSFET flicker noise, but recent studies [1]–[4] point toward an explanation of $1/f$ noise based on the carrier number fluctuation theory. Since physics-based $1/f$ models of noise are usually either too complicated or not general enough for cir- cuit analysis and design [5], analog designers prefer empirical or SPICE models. In this paper, we show that noise models for- mulated in terms of the inversion level concept [6], [7] can rec- oncile the accuracy and consistency of a physics-based approach with the simplicity necessary in design.

First, the consistency of noise models regarding the represen- tation of series–parallel associations of transistors is examined. A new one-equation physics-based model of the long-channel MOSFET flicker noise [4], [19], that encompasses all MOSFET operating regions, is then rewritten using the inversion level con- cept. Simple design formulas for the different operating regions are developed for flicker, and thermal noise. The proportionality of the flicker noise corner frequency with the transistor transi- tion frequency is proved and experimentally verified under wide bias conditions ranging from subthreshold to strong inversion. Finally, a design example consisting of a low-noise micropower low-pass filter–amplifier (dc 20–Hz Gain 40) is shown. The

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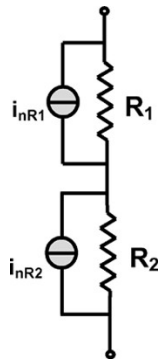

Fig. 1. Circuit for the calculation of the total noise produced by two resistors in series.

expressions for flicker and thermal noise, and corner frequency presented here constitute a compact and consistent set of equa- tions, very useful for design purposes.

II. Consistency of Noise Models

We define a noise model to be consistent regarding series or parallel associations if the composition of the noise contributions from the individual series (or parallel) elements is the same as the noise from the series (or parallel) equivalent. Obviously, the thermal noise model (1) for a resistor

$$S_i(f) = \frac{4k_BT}{R} \tag{1}$$

is consistent [8]. In (1), $S_i(f)$ is the power-spectral density (PSD) of the noise current, k_B is the Boltzmann's constant, T is the absolute temperature, and R is the resistance value. For two series elements R_1 and R_2 (Fig. 1), the total noise current introduced into the circuit: $S_{i\_\mathrm{tot}}(f) = 4k_BT/(R_1 + R_2)$ can be obtained by composing the individual noise sources or using (1) to calculate the noise of the equivalent resistor $R_1 + R_2$. The analysis can be extended to MOS transistors, because, for these devices, series and parallel equivalents are clearly defined [9], [10]. Consider, for example, the virtual cut of a transistor that slices it into two series elements as in Fig. 2(a). Suppose that the upper transistor M_u introduces a noise current with a PSD equal to $S_{i_{du}}$, and the lower transistor M_l introduces a noise current $S_{i_{dl}}$. Small-signal analysis [see Fig. 2(c)] allows the calculation of the PSD of the noise current $S_{i_{d\_s}}$ of the series-composed transistor. Considering $S_{i_{dl}}$ and $S_{i_{du}}$ to be uncorrelated noise current sources, it follows that

$$S_{i_{d\_s}}(f) = \left[\frac{}{1+k}\right]^2 S_{i_{dl}}(f) + \left[\frac{}{1+k}\right]^2 S_{i_{du}}(f) \tag{2}$$

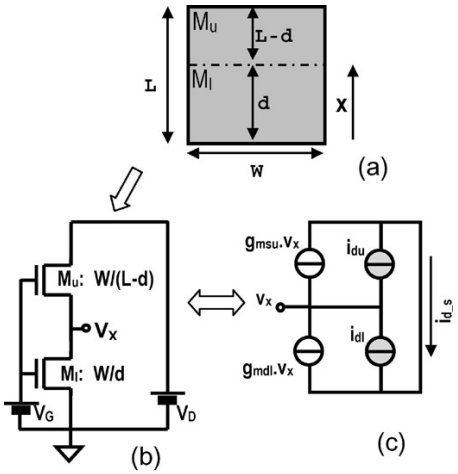

Fig. 2. Circuit for the calculation of the total noise produced by two transistors in series.

where $k = g_{msu}/g_{mdl}$, g_{msu}, and g_{mdl} are the source and drain transconductances of transistors M_u and M_l, respectively. Source (drain) transconductance $g_{ms(d)}$ is defined as the derivative of the drain current with respect to the source (drain) voltage. For the partition of the channel as in Fig. 2 we have [6], [7]

$$g_{msu} = -\mu \frac{W}{L-d} Q'_{IX} \quad g_{mdl} = -\mu \frac{W}{d} Q'_{IX} \qquad (2b)$$

where Q'_{IX} is the inversion charge density evaluated at a point X in the channel [Fig. 2(b)] and μ is the effective mobility. Consequently, $k = d/(L-d)$ depends only on the geometry and (2a) can be rewritten as

$$S_{i_{d\_s}}(f) = \left[\frac{}{L}\right]^2 S_{i_{dl}}(f) + \left[\frac{L-d}{L}\right]^2 S_{i_{du}}(f). \qquad (3)$$

As an example, let us now consider the application of (3) to thermal noise. It is already known [11] that the PSD of the thermal channel noise of an NMOS transistor is

$$S_{iw} = \frac{-4k_B T \mu Q_I}{L^2} \qquad (4)$$

where Q_I is the total inversion charge in the channel. Calculating the PSD of the upper and lower transistor using (4) and substituting the result into (3), yields

$$S_{iw} = -4k_B T \mu \left[\frac{Q_{Il}}{d^2}\left(\frac{d}{L}\right)^2 + \frac{Q_{Iu}}{(L-d)^2}\left(\frac{L-d}{L}\right)^2\right] = \frac{-4k_B T \mu Q_I}{L^2} \qquad (5)$$

where Q_{Il}, Q_{Iu}, and Q_I are the total inversion charge in the channel of the lower, upper, and equivalent transistor, respectively. As expected, the classical thermal noise model of the MOSFET is consistent with the series association of transistors. Not all noise models are consistent. In Table I, columns 2 and 3, the consistency (or inconsistency) regarding the series–parallel association of some SPICE-like flicker noise models [2], [12] is presented. Model $\mathrm{NLEV} = 1$ consistently represents the series association of transistors, but $\mathrm{NLEV} = 0$ and $\mathrm{NLEV} = 2, 3$ do not. Using nonconsistent models for noise gives different

TABLE I

USUAL FLICKER NOISE MODELS IMPLEMENTED IN SPICE. ✓: MODEL IS CONSISTENT WITH EXPERIMENTAL RESULTS. ✗: MODEL FAILS TO PREDICT EXPERIMENTAL RESULTS.

MODEL	SERIES EQUIVALENT	PARALELL EQUIVALENT	NORMALIZED P.S.D.: S_{Id}/I_D^2
Spice NLEV=0 $S_{I_d} = \frac{K_F I_D^{AF}}{C'_{OX}.L^2}.\frac{1}{f}$	✗	Only if AF =1 →	✗ Tends to ∞ in W.I.
Spice NLEV=1: $S_{I_d} = \frac{K_F I_D^{AF}}{C'_{OX}.W.L}.\frac{1}{f}$	✓	Only if AF =2 →	✗ Remains constant in the whole operating range.
Spice NLEV=2,3 : $S_{I_d} = \frac{K_F g_{mg}^2}{C'_{OX}.W.L}.\frac{1}{f^{EF}}$.	✗	✓	✓ $\propto \frac{g_{mg}^2}{I_D^2}$
BSIM 3v3 See ref .[12,14] for description.	✓ (see note (1))	✓	✓

(1) According to the manual [14], BSIM3v3 uses different models for strong and weak inversion.

total noise values for the same transistor, when the transistor is considered a series association of two parts. As an example, let us consider the series association in Fig. 2, with different divisions of the same channel length L. In strong inversion and using the NLEV = 2,3 model, the noise power of the series association of two $L/2$ transistors is 17% higher than the noise of the channel length L transistor. For a series association of a longer lower and a shorter upper transistor the noise power of the series association is roughly twice that of the channel length transistor.

III. CONSISTENT FLICKER NOISE MODEL IN TERMS OF INVERSION LEVELS

Flicker noise or simply $1/f$ noise displays a PSD of the form $S(f) = K/f^{\beta}$, with K, β constants, $\beta \approx 1$ [1]–[4]. According to analysis and experiment [4], the normalized PSD of the noise current S_{I_d}/I_D^2 presents a plateau in weak inversion and decreases in strong inversion. Even though moderate and weak inversion are very important for modern low-voltage low-power design, some of the available models of flicker noise do not give correct results in weak or moderate inversion. In Table I, column 4, the behavior of the ratio S_{I_d}/I_D^2 for usual models of flicker noise [2], [12] is shown. Spice models NLEV = 0, 1 predict wrong dependence of the noise performance in terms of the bias point. In model NLEV = 0, S_{I_d}/I_D^2 tends toward infinity in weak inversion. Spice NLEV = 1 gives a constant S_{I_d}/I_D^2 for all the operating regions. On the other hand, Spice NLEV = 2, 3 represent approximately the behavior of the ratio S_{I_d}/I_D^2, which is proportional to the gate transconductance to drain current ratio g_{mg}^2/I_D^2. The well-known EKV model [10] uses the Spice NLEV = 2, 3 expression for $1/f$ noise. The BSIM3v3 noise model [13] shows the correct behavior for the S_{I_d}/I_D^2 ratio from weak to strong inversion and is consistent for series and parallel association. However, the BSIM3v3 noise

model interpolates flicker noise in moderate inversion [13], [14] and it has the drawback of having 3 fitting parameters.

The physics-based compact model of [4]

$$\frac{S_{I_d}}{I_D^2} = \frac{q^2 N_{\rm ot}\mu}{L^2 n C'_{\rm OX} I_D} \cdot \frac{1}{f} \cdot \ln\left[\frac{nC'_{\rm OX}\phi_t - Q'_{IS}}{nC'_{\rm OX}\phi_t - Q'_{ID}}\right] \qquad (6)$$

is a simple, single-piece model, continuous in all operating regions from weak to strong inversion and from the linear to saturation regions. Equation (6) was deduced from a charge-based model integrated along the transistor channel, thus resulting in an inherently consistent model for the series and parallel associ- ations of transistors. $C'_{\rm OX}$, q, L, ϕ_t, n, Q'_{IS}, Q'_{ID} are, respectively, the oxide capacitance per unit area, electron charge, thermal voltage, channel length, channel charge density at source and drain, and is the slope factor, slightly dependent on the gate voltage. The parameter $N_{\rm ot}$ is the equivalent density of oxide traps defined [1] by

$$N_{\rm ot}[{\rm cm}^{-2}] = \frac{k_B T N_t(E)}{\gamma} \qquad (7)$$

where $N_t(E)[{\rm cm}^{-3}{\rm eV}^{-1}]$ is the density of oxide traps per unit volume and unit energy and $1/\gamma[{\rm cm}^{-1}]$ is the attenuation coefficient of the electron wave function in the oxide [1], [13]. For $N_t(E) \approx 4 \times 10^{16}\ {\rm cm}^{-3} \cdot {\rm eV}^{-1}$, $k_B T = 0.026$ eV and $1/\gamma = 1$ Å (10^{-8} cm), $N_{\rm ot}$ is of the order of $10^7\ {\rm cm}^{-2}$ [15].

A useful alternative expression for (6) is obtained if the charge densities at source (drain) are expressed in terms of the normal- ized forward and reverse currents i_f, i_r [6], [7]. In [6] and [7], the drain current I_D is expressed as the difference between for- ward I_F, and reverse I_R components

$$I_D = I_F - I_R = I_S(i_f - i_r) \qquad (8)$$

where $I_S = (1/2)\mu C'_{\rm OX} n \phi_t^2 (W/L)$ is the specific current, pro- portional to the geometric ratio W/L of the transistor. i_f and i_r are the normalized forward and reverse currents or inversion levels at source and drain, respectively. Using the relationship
between normalized charges and currents from [7]

$$-\frac{Q'_{IS(D)}}{nC'_{\rm OX}\phi_t} = \sqrt{1 + i_{f(r)}} - 1 \qquad (9)$$

expression (6) can be rewritten as

$$\frac{S_{I_d}}{I_D^2} = \frac{N_{\rm ot}}{WLN^{*2}} \cdot \frac{1}{f} \cdot \frac{1}{(i_f - i_r)} \ln\left[\frac{1+i_f}{1+i_r}\right] \qquad (10)$$

where we define $N^* = nC'_{\rm OX}\phi_t/q$ as in [13] and [14].

From weak to strong inversion in the linear region, $i_f \approx i_r$ and (10) reduces to

$$\frac{S_{I_d}}{I_D^2} = \frac{N_{\rm ot}}{WLN^{*2}} \cdot \frac{1}{f} \cdot \frac{1}{1+i_f}. \qquad (11)$$

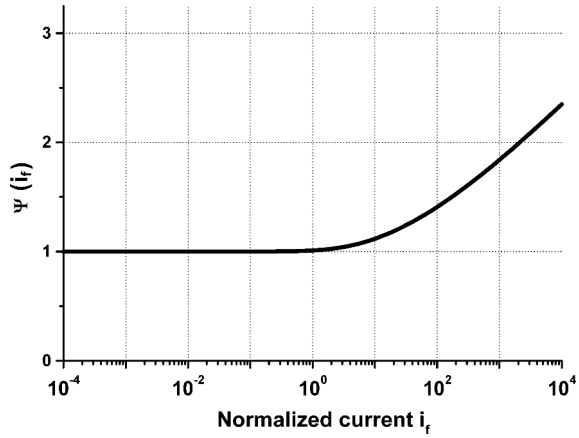

Fig. 3. Function $\psi(i_f)$.

In weak inversion, $i_r \ll 1$ and $i_f \ll 1$.The first-order series expansion of (10) leads to

$$\frac{S_{I_d}}{I_D^2} = \frac{N_{\rm ot}}{WLN^{*2}} \cdot \frac{1}{f}. \qquad (12)$$

Writing the drain current to gate transconductance ratio in terms of the inversion level for a transistor operating in saturation [7]:

$$\frac{I_D}{n\phi_t g_{mg}} = \frac{1 + \sqrt{1+i_f}}{2}. \qquad (13)$$

Sometimes, designers prefer to write the transistor noise referred to input or, equivalently, $S_{\rm Vgate} = S_{Id}/g_{mg}^2$. Then, from (10) and (13), it follows that

$$S_{\rm Vgate} = \frac{q^2 N_{\rm ot}}{WLC'^2_{\rm OX}} \cdot \frac{1}{f} \cdot \psi(i_f) \qquad (14)$$

where

$$\psi(i_f) = \left(\frac{1+\sqrt{1+i_f}}{2}\right)^2 \frac{\ln(1+i_f)}{i_f}. \qquad (15)$$

Because $\psi(i_f)$ shows very small variations with i_f, as depicted in Fig. 3, one of the so-called empirical models [11] follows if we consider this function equal to 1, or, equivalently

$$S_{\rm Vgate} \cong \frac{q^2 N_{\rm ot}}{WLC'^2_{\rm OX}} \cdot \frac{1}{f}. \qquad (16)$$

Due to its simplicity, the empirical model (16) is very convenient for hand calculations. Moreover, in current designs, the inversion level is seldom higher than 10^2. Thus, (16) can be used with SPICE defining K_F as $K_F = q^2 N_{\rm ot}/C'_{\rm OX}$ in Spice NLEV 2, 3 (Table I). Even though the empirical model of (16) gives a good estimation of the flicker noise of a transistor in saturation, it is not consistent with expression (3). In effect, the empirical model does not consider the distributed nature of the MOSFET, because it represents noise as a gate voltage source independent of the bias condition ($\psi(i_f) = 1$).

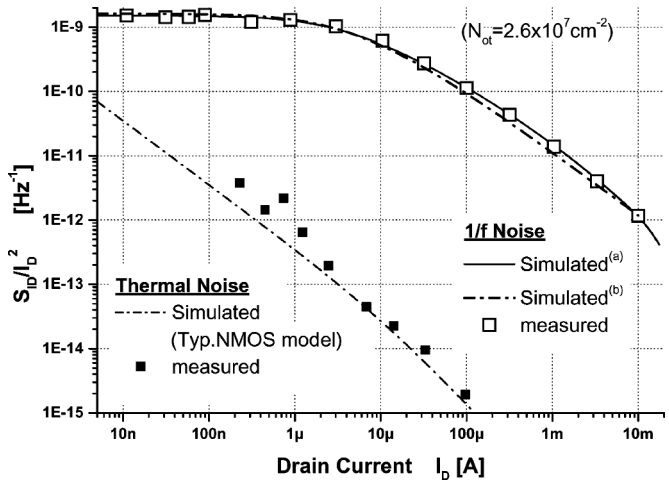

Fig. 4. Normalized flicker and thermal PSD at f = 1 Hz for a saturated NMOS (W/L = 200/5). Flicker noise is simulated using (a) physical model (10) (b) SPICE NLEV = 2 3; equivalent to approximation (16).

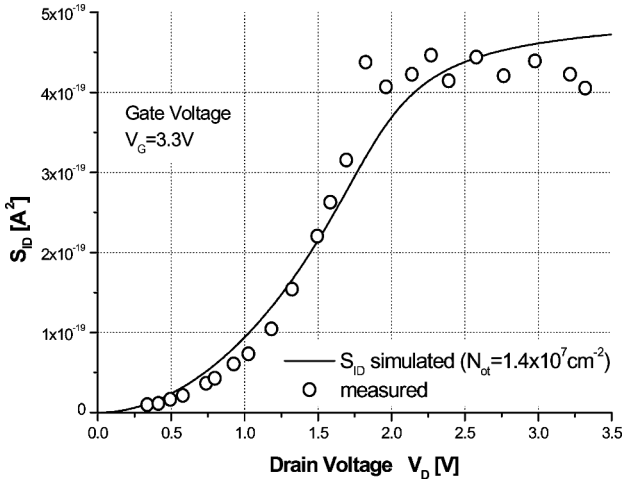

Fig. 5. Flicker noise PSD at f = 1 Hz, for a W/L = 20/10 NMOS transistor, from linear region up to saturation.

It should be noted that for high current applications such as those in RF circuits, equation (16) can give large errors. For a gate overdrive V_{GS}- V_{TH} of 1.5 V, $i_f = 2000$, and $\psi = 2$.

Fig. 4 shows measurements of the normalized PSD (S_{Id}/I_D^2) of the flicker noise for a saturated NMOS transistor of a 0.8-m CMOS process, with an aspect ratio $W/L = 200\mu$ m /5μm. The plateau of S_{id}/I_D^2 in weak inversion predicted by theory is apparent. In the same figure, simulations using (10) and SPICE NLEV 2, 3 with $K_F = K_F' N_{\rm ot}/C'_{\rm OX}$ are presented. Note the slight underestimation of flicker noise in strong inversion using the empirical model (16). Fig. 5 was obtained for a $20/10$ NMOS transistor, fabricated in the same 0.8μm process (but from different batches), from the linear up to the saturation region with V_G = 3.3 V. In both graphs, $N_{\rm ot}$ was adjusted to fit the measurements; the measurement procedure is described in [4]. The different values obtained for $N_{\rm ot}$ in Figs. 4 and 5 are acceptable, since the transistors were fabricated in different runs.

IV. Thermal Noise

From the classical model for thermal channel noise (4) and the expression of the total inversion charge in terms of the channel charge densities at the ends of the channel [7], [11], the PSD S_{iw} of the thermal noise is

$$S_{iw} = -4k_B T\mu \frac{W}{L} \times \frac{\frac{2}{3}\left(Q'^2_{IS}+Q'_{IS}Q'_{ID}+Q'^2_{ID}\right) - nC'_{\rm OX}\phi_t\left(Q'_{IS}+Q'_{ID}\right)}{Q'_{IS}+Q'_{ID}-2nC'_{\rm OX}\phi_t}. \quad (17)$$

Expression (17) is valid in all the operating regions, from weak to strong inversion and from the linear to the saturation region, but is rather cumbersome. Useful design expressions, originally presented in [6], in terms of the transistor transconductances are easily deduced. In the linear region, from weak to strong inversion $Q'_{IS} \cong Q'_{ID}$, and

$$S_{iw} \cong -4k_B T\mu \frac{W}{L} Q'_{IS} = 4k_B T g_{ms} \cong 4k_B T g_{md}. \quad (18)$$

As expected, the channel behaves as a resistance of value $1/g_{ms} = 1/g_{md}$.

In weak inversion, $\left|Q'_{IS(D)}\right| \ll nC'_{\rm OX}\phi_t$, and it is possible to rewrite (17) as

$$S_{iw} \cong -4k_B T\mu \frac{W}{L}\frac{(Q'_{IS}+Q'_{ID})}{2} = 4k_B T \frac{g_{ms}+g_{md}}{2}. \quad (19)$$

For a saturated transistor ($g_{ms} \gg g_{md}$) in weak inversion

$$S_{iw} = 2k_B T n g_{mg}. \quad (20)$$

In saturation $|Q'_{ID}| \ll |Q'_{IS}|$ and strong inversion, $|Q'_{IS}| \gg nC'_{\rm OX}\phi_t$. Thus, it is possible to rewrite (17) as

$$S_{iw} = \frac{8}{3} n k_B T g_{mg}. \quad (21)$$

In Fig. 4, the calculated and measured values of the normalized PSD of thermal noise are shown. These measurements were taken at a frequency of 25 kHz to minimize the effect of flicker noise.

V. Flicker Noise Corner Frequency

The corner frequency f_c, defined as the frequency at which the flicker noise and thermal noise PSDs have the same value, can be calculated directly in terms of Q'_{IS} and Q'_{ID} from (6) and (17). However, we obtain simpler results determining f_c in weak inversion with (12) and (20) and in strong inversion with the help of (10) and (21).

$$f_c = \frac{\alpha g_{mg}}{WLC'_{\rm OX}}\frac{N_{\rm ot}}{N^*} \cong \frac{\pi}{2}\frac{N_{\rm ot}}{N^*} f_T \quad (22)$$

with $\alpha = 1/2$ in weak inversion and $\alpha \cong 9/16$ in strong inversion. Note that the corner frequency in (22) is proportional to the transition frequency f_T of the transistor [7], [11], which results in a useful approximation for the designer.

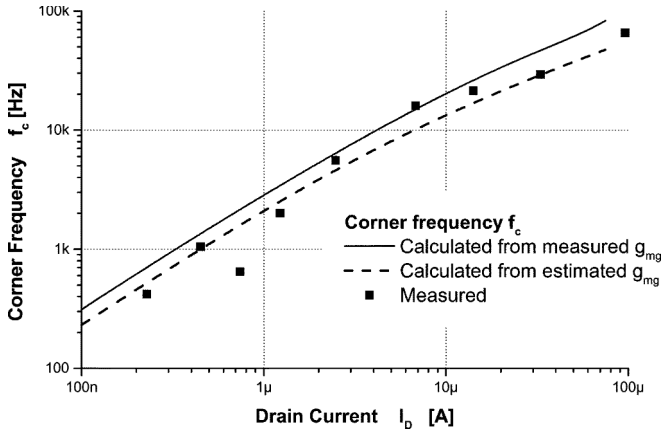

Fig. 6. Calculated and measured values of the corner frequency f , for a W/L == 2ü/5 NMOS transistor.

The total noise in a frequency band ($f_2 - f_1$) resulting from the contributions of both thermal and flicker noise can be cal- culated as an equivalent gate rms voltage. For a saturated tran- sistor operating in weak inversion, the integration of both (12) and (20) yields

$$v_{\text{gate}}^2 = \frac{2nk_BT}{g_{mg}}\left((f_2 - f_1) + f_c \ln\left(\frac{f_2}{f_1}\right)\right) \qquad (23)$$

For strong inversion, an analogous formula holds with slightly different coefficients.

In Fig. 6, we present the simulated and measured corner frequency of a saturated NMOS transistor for various bias currents. The solid line represents f_c calculated using (22) together with the measured value for g_{mg}. The dashed line represents f_c cal- culated using expression (13) for g_{mg}. For this transistor, the dimensionless factor $n^* \cong 0.8 \times 10^{-3}$. Both simulations and measurements predict that the corner frequency decreases as the transistor operates deep in weak inversion. This is in accordance with the noise measurements presented in [16].

VI. Aplication of Noise Models to Design of an OTA-C Filter

The low-noise, low-frequency G_m- preamplifier of Fig. 7(a) has been designed to be employed in an implantable sensor device where noise and power consumption are critical. The transfer function of the circuit is

$$G(f) = \frac{G_{m1}}{G_{m2}}\left(\frac{1}{1 + \frac{j2\pi fC}{G_{m2}}}\right) \qquad (24)$$

The cutoff frequency of the filter should be set to 20 Hz. The signal frequencies range from 0.3 to 10 Hz with a required input referred noise of less than 25 μV_{RMS}. The gain $G_{m1}/G_{m2} = 40$. Linearity of G_{m1} is not a major issue due to the low input-voltage swing, but the linear range of G_{m2} should be at least 100 mV. To achieve the required performance, series–parallel division of currents [17], [18] have been employed for G_{m2} [Fig. 7(c)], while G_{m1} is a standard symmetrical OTA [Fig. 7(b)]. Unless G_{m2} is excessively noisy, the total noise is mainly determined by the input OTA. Thus, design starts with an exploration of the design space for G_{m1}

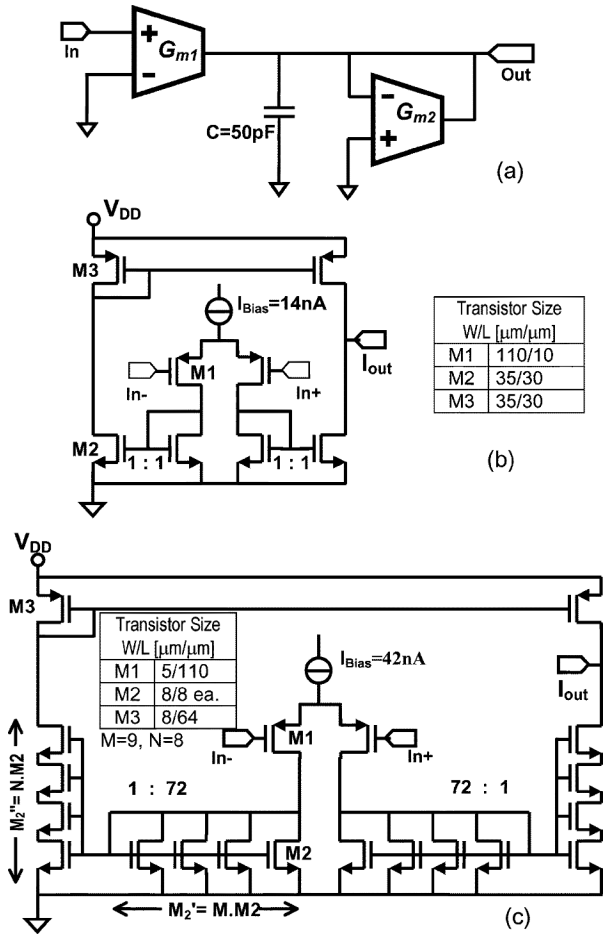

Fig. 7. (a) Topology for the target low-noise amplifier. (b) G_{m1} OTA. (c) G_{m2} OTA with series–parallel current division.

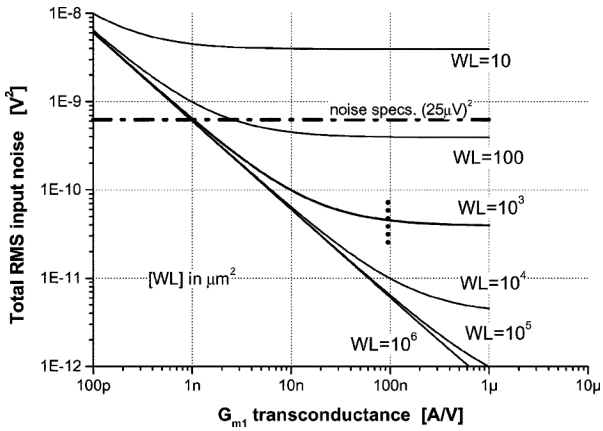

Fig. 8. Simplified design space for G_{m1} total input referred noise in the band of interest in terms of the gate area of the input pair, and G_{m1} transconductance. The horizontal dashed line indicates the maximum acceptable noise floor while the vertical line indicates the approximate selected solution.

shown in Fig. 8. Owing to the low frequencies involved and the specification of low power, all transistors in G_{m1} operate in weak inversion. Each transistor in the symmetrical OTA introduces approximately the same amount of noise if they have the same area, and the same number of effective traps for both nMOS and pMOS transistors is assumed. Consequently, neglecting the common mode noise of the current source, the

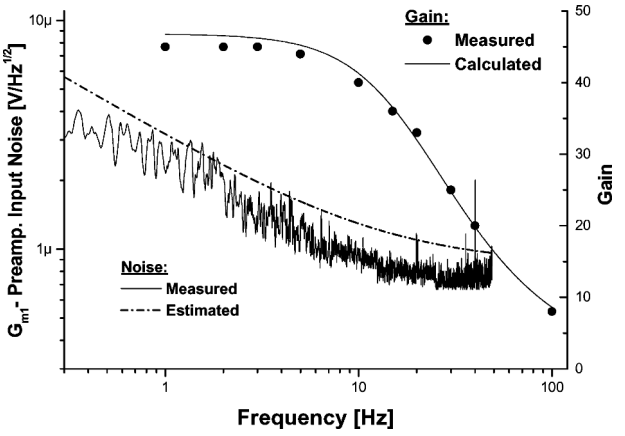

Fig. 9. Estimated and measured noise for G_{m1} and estimated and measured gain for the preamplifier.

input referred noise for G_{m1}, plotted in Fig. 8, is simply eight times the rms voltage given by (23).

For the specific area budget, the chosen solution was a 1000-μm^2 gate area for each transistor. A transconductance $G_{m1} = 100$ nS was chosen according to (22) to set the corner frequency $f_c \approx 10$ Hz, just above the signal band. Thus, at the selected point (indicated by the vertical dashed line in Fig. 8) flicker noise dominates, and the reduction of the total input noise is possible only by increasing the gate area but not the transconductance G_{m1} (22), (23).

The G_{m2} OTA topology is shown in Fig. 7(c), with series–parallel division of current to achieve a transconductance of 2.35 nS. The inversion level of the input pair is determined by the desired linear range [18] and the division factor ($M \cdot N$) results from $G_{m2} = g_{mg1}/(M \cdot N)$, where g_{mg1} is the gate transconductance of the input pair. In our design, the current division factor is 72 ($M = 9, N = 8$). A simple noise calculation is possible for G_{m2}, considering that M_2'', M_3 are in weak inversion and $M \quad N \gg 1$. The equivalent thermal noise at the G_{m2} input results in

$$v^2_{\text{input\_}w}(f) \approx \frac{4nk_BT}{G_{m2}}\left(\sqrt{1+i_f}+1\right) \qquad (25)$$

Note that (25) is very similar to that obtained for the simple symmetrical OTA G_{m1} but here we are paying a p rice in noise for the linearization represented by the factor ($\sqrt{1+i_f}+1$). An equation similar to (25) can be derived for flicker noise. The corner frequency for G_{m2} was estimated as 0.5 Hz. The pream- plifier and stand-alone OTAs were fabricated in a 0.8-m stan- dard CMOS technology. In Fig. 9, the measured voltage transfer function of the amplifier as well as the measured and predicted input noise for G_{m1} are shown. The noise current was mea- sured using a low-noise current preamplifier and a spectrum ana- lyzer. The total measured noise input voltages in the signal band (from 0.3 to 10 Hz assuming 20 db/dec band-pass filter) were 5 μ V_{RMS} for G_{m1}, 30 μ V_{RMS} for G_{m2}, and 5 μ V_{RMS} for the amplifier, while the estimated values were 6, 49, and 6 μV_{RMS}, respectively. The measured corner frequency for G_{m1} was 8 Hz. The circuit occupies a total area of 0.1 mm^2, and operates down to a 2-V supply with a current consumption of 14 nA for G_{m1} and 43 nA for G_{m2}

VII. Conclusion

The consistency of noise models regarding series–parallel association of transistors has been analyzed, and the flaws in some simple flicker noise models have been highlighted.Consistent models for flicker and thermal noise in MOSFETs, valid in weak, moderate and strong inversion, and in the linear region, have been presented. These models consist of simple and single- piece expressions in terms of the inversion levels. Design-ori- ented expressions for the different operating regions have been given, and the proportionality between corner frequency and transition frequency has been derived and experimentally veri- fied. As the final example shows, the expressions presented can provide a powerful tool for both hand calculations and com- puter-assisted analysis and design of MOSFET integrated cir- cuits. Although compact noise models can hardly fit every tran- sistor experiment, we expect this work to help design accurately and in a simple manner, low-noise circuits.

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