A Fully Differential Monolithic 2.4GHz PA for IEEE 802.15.4 based on Efficiency Design Flow

Rafaella Fiorelli
Eduardo Peralías

IMSE-CNM CSIC-Univ. de Sevilla
Spain

Nicolás Barabino
Fernando Silveira

GME-Univ. de la República
Uruguay

Outline

1. Introduction
2. PA modeling
3. PA Efficiency design flow
4. Circuit Implementation
5. Measurements
6. Conclusions and future work.

Introduction

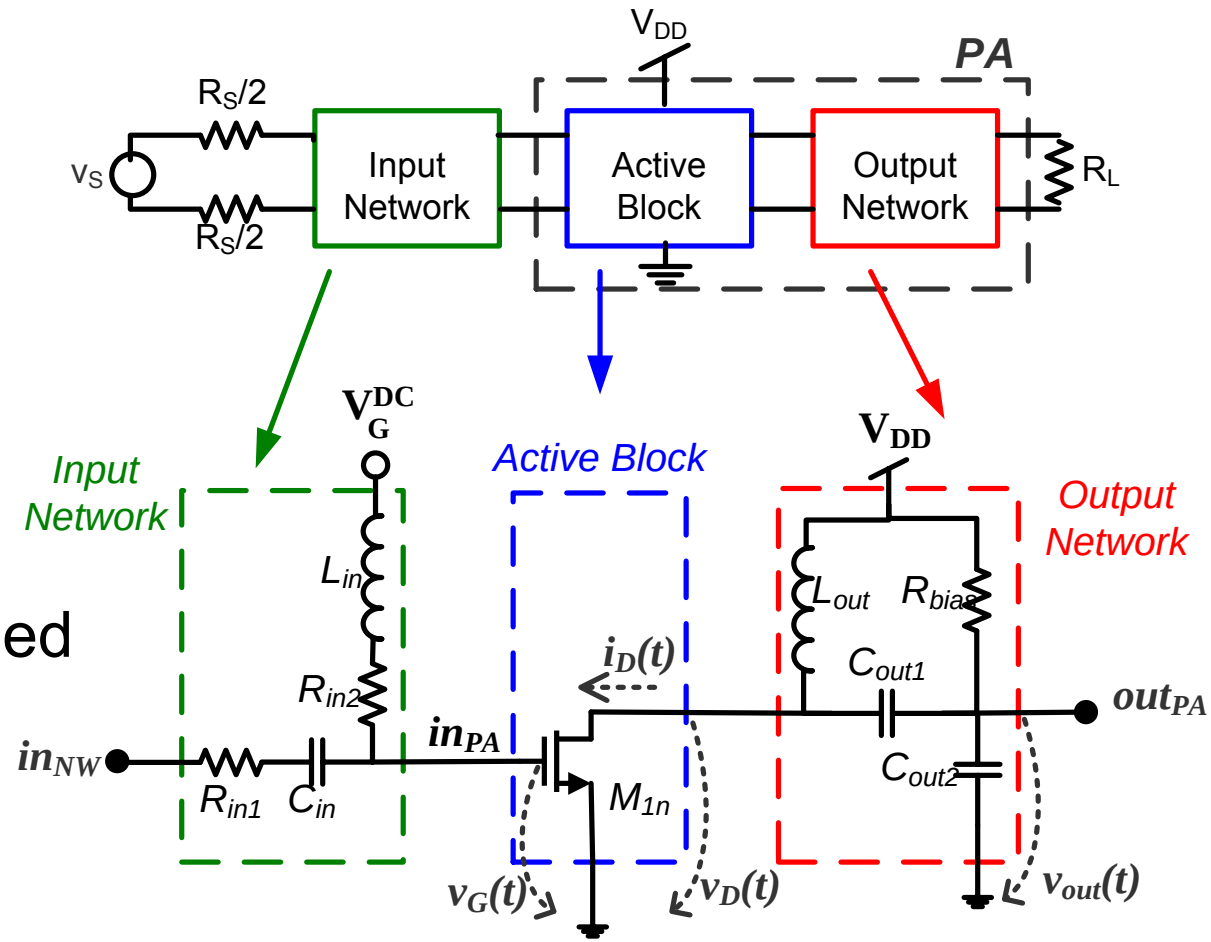
- An optimized class C PA suited for IEEE 802.15.4 is presented.
- Class C PAs support phase modulation.
- The design is being used to evaluate the Classes A-B-C PA design methodology [1].

[1] N. Barabino, R. Fiorelli, and F. Silveira, “Efficiency based design for fully-integrated class C RFpower amplifiers in nanometric CMOS” in IEEE International Sym*posium on Circuits and Systems (ISCAS), 2010.*

PA modeling

Differential topology

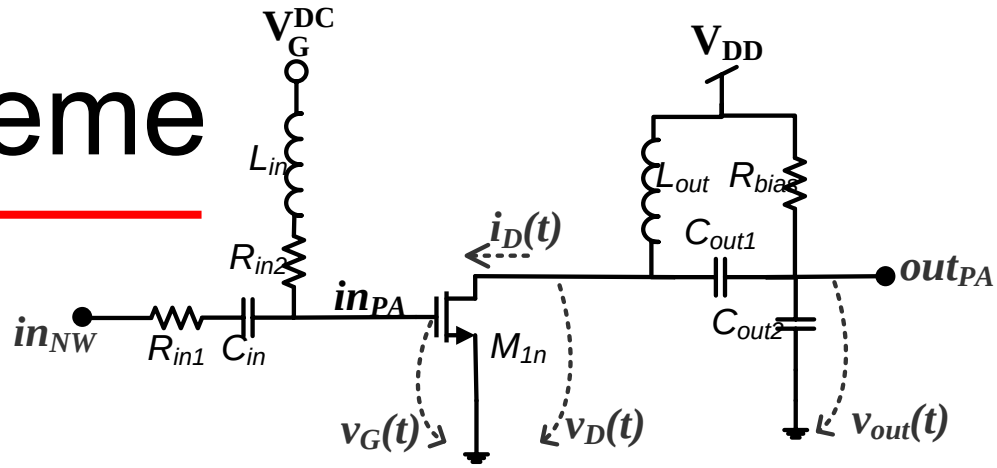
Single-ended topology



R_s=100Ω

R_L=100Ω

PA design scheme



Zigbee Specs:

$P_{out} = 0dBm$

$P_{harm}^{2nd} = -40dBm$

$P_{harm}^{3rd} = -20dBm$

OQPSK modulation

Low power

SPECIFICATIONS

P_{out}

P_{harm}^{2nd} ; P_{harm}^{3rd}

Efficiency η

Power

BOUNDARY CONDITIONS

Max power to RL → max voltage swing at V_D $2 \cdot V_{DD}$, V_{DD}, 0

Minimum L to reach the highest f_T

DESIGN FLOW

FINAL DESIGN

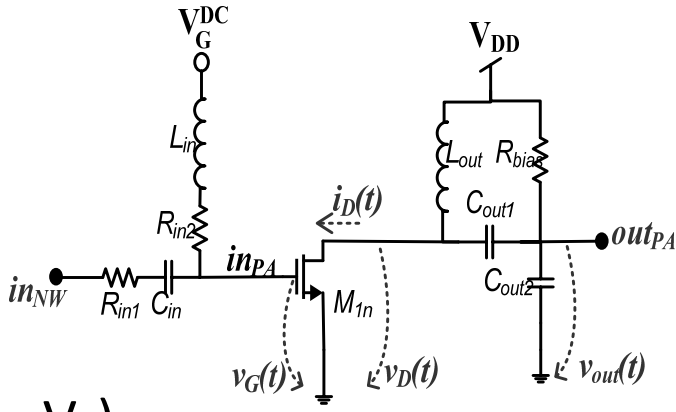
Transistor size (W)

Output NW sizing (Lout, C's)

Biasing → V_G^{DC}

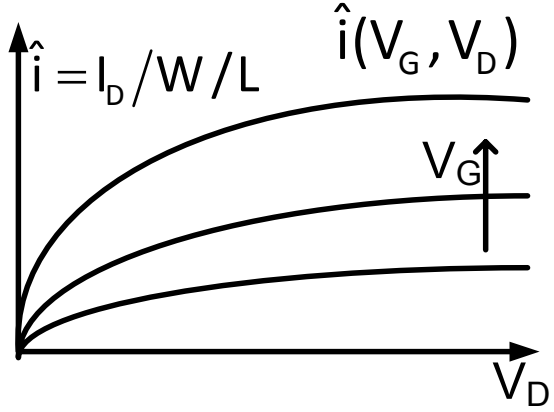
Max. Amplitude → V_G^{RF}

PA design flow



(1) MOS model in DC:

$$\hat{i} = I_D/(W/L) \quad \text{vs} \quad (V_G, V_D)$$



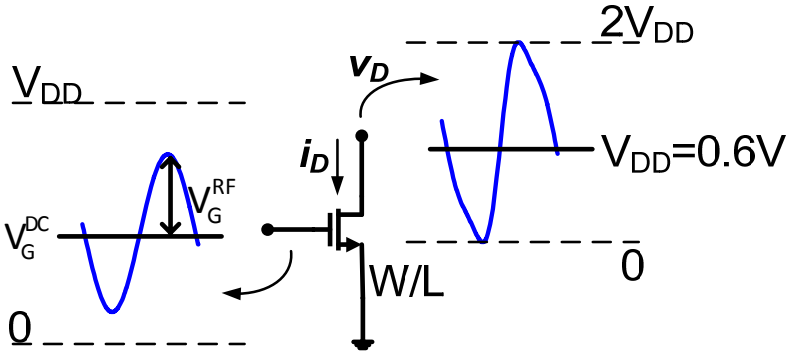
(2) Inductor modeling with S-parameters: L_{ind}, Q, R_p @ f_0

(3) Output NW: (i) transfer power to RL
(ii) filter the harmonics
$R_L \rightarrow R_{NW}$ (seen at the drain of MOS)

$$\begin{cases} P_{out} = \dfrac{V_{out}^2}{2R_L} \cong \dfrac{V_D^{RF^2}}{2R_{NW}} \\ v_D(t) = V_{DD} + V_D^{RF}\sin(\omega_0 t) \end{cases}$$

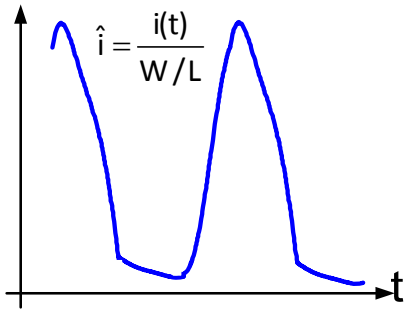
PA design flow

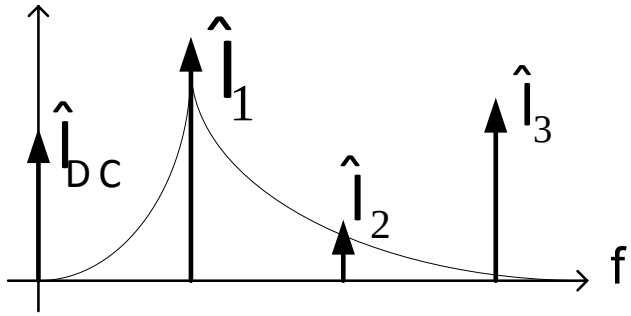
(4) Choose $\left(V_G^{DC}, V_G^{RF}\right) \rightarrow v_G(t) = V_G^{DC} + V_G^{RF}\sin(\omega t)$



(5) Main hipothesis: $\hat{i}(t)$ obtained with $\hat{i}(V_G, V_D)$, the DC normalized current of step (1)

By Fourier, $\hat{I}_{DC}, \hat{I}_1, \hat{I}_2$ and $\hat{I}_3$ are calculated.





PA design flow

(6) Calculate the efficiency of MOS: $\eta_{MOS} = \frac{P_{NW}}{P_{DC}} = \frac{I_1 V_D^{RF} / 2}{I_{DC} V_{DD}} = \frac{\hat{I}_1 V_D^{RF}}{2\hat{I}_{DC} V_{DD}}$

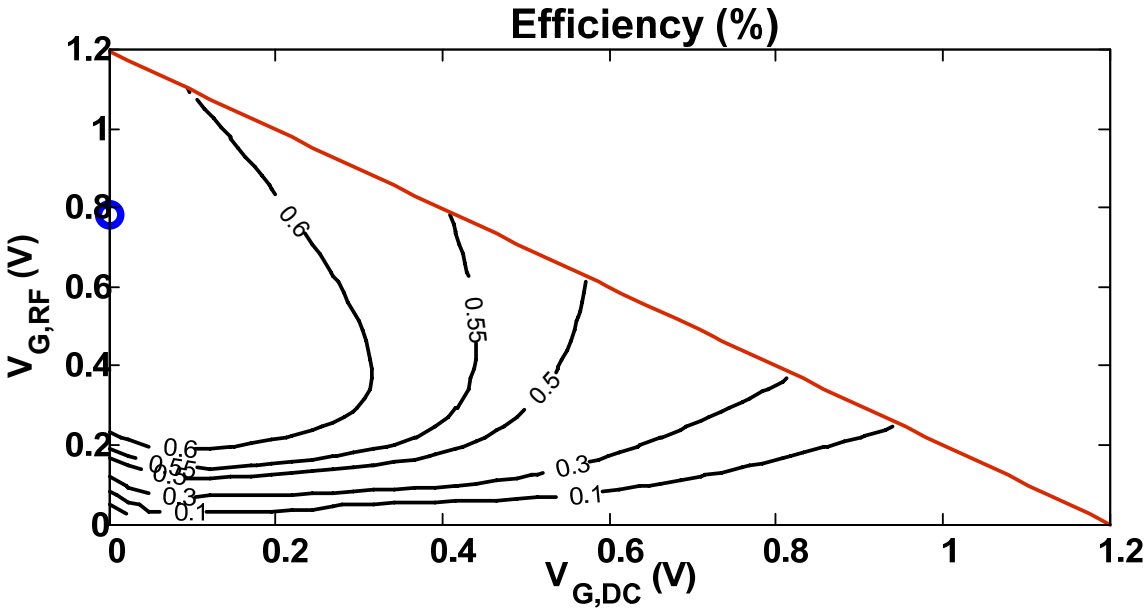
(7) Calculate the misspent power of the output network and the total PA efficiency:

$$P_{out} = P_{NW} - P_{miss} = \frac{V_D^{RF^2}}{2R_{NW}} - \frac{V_D^{RF^2}}{2R_p} \rightarrow \eta_{NW} = \frac{P_{out}}{P_{NW}} = 1 - \frac{R_{NW}}{R_p} \rightarrow \eta = \eta_{MOS}\eta_{NW}$$

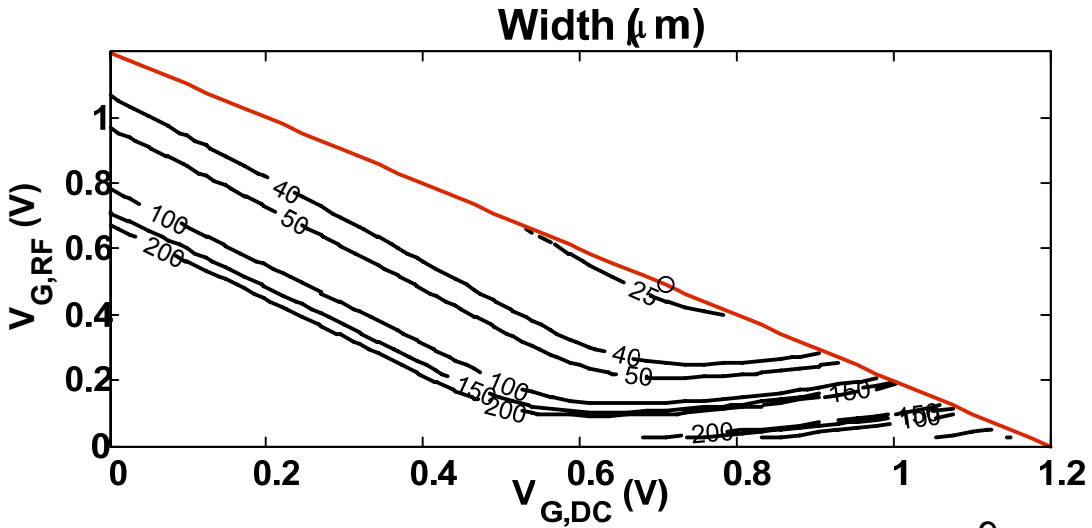
For P_{out} and L_{out} solve for: R_{NW}, P_{NW} and η. L_{out} provides the correct harmonic filtering.

(8) Calculate the transistor aspect ratio: $\frac{W}{L} = \frac{I_1}{\hat{I}_1} = \frac{2P_{NW} / V_D^{RF}}{\hat{I}_1}$

PA design flow (cont'd)



MATLAB tool design maps.



Circuit Implementation

Summary of specifications

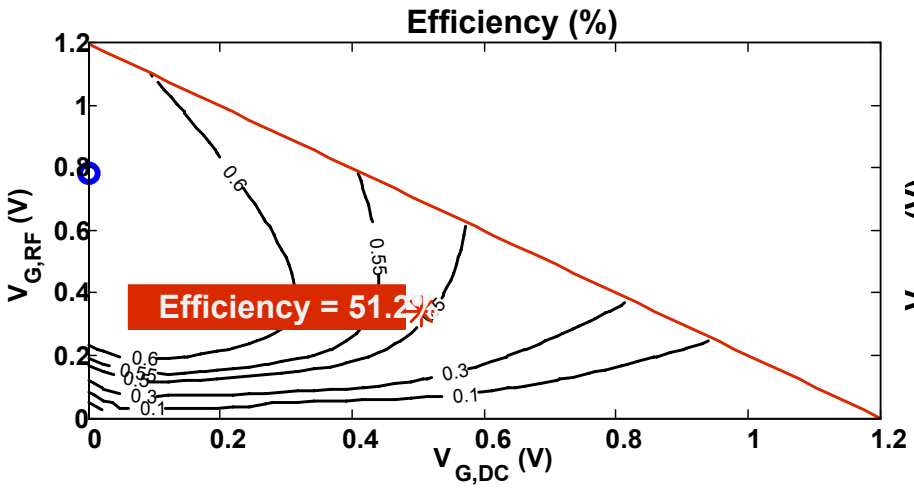
$P_{out} > 0$ dBm	$R_L = 100\Omega$	$P_{harm}^{2nd} \leq -40$dBm
$V_D^{RF} = 0.6$V	$R_P > 1k\Omega$	$P_{harm}^{3nd} \leq -20$dBm
$V_{DD} = 0.65$V	$\eta > 35\%$	$OP_{1dB} \geq -10$dB

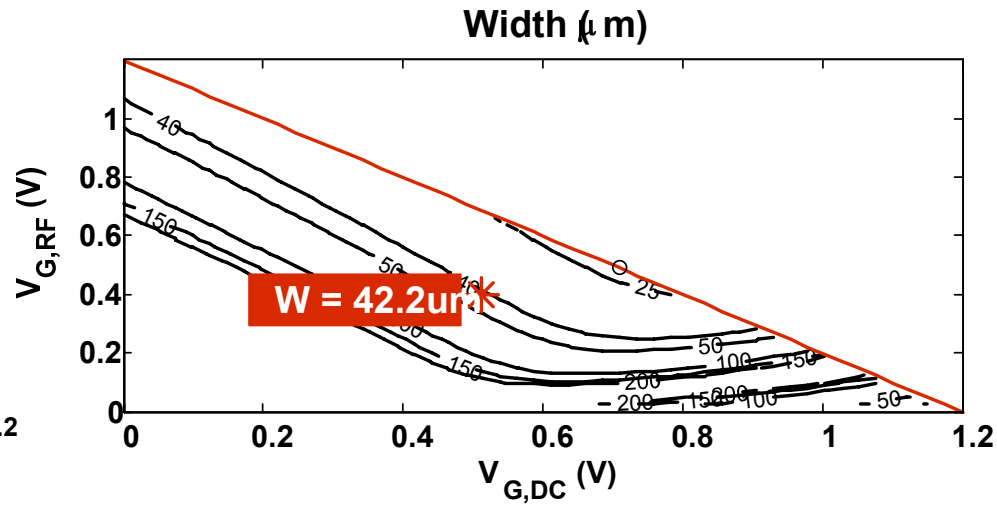
1.2V RF 90nm CMOS technology, 1P9M.

Minimum V_G supported by the technology limits us to select points with higher efficiency.

Final design point:

$$V_G^{DC} = 0.5V$$
$$V_G^{RF} = 0.4V$$

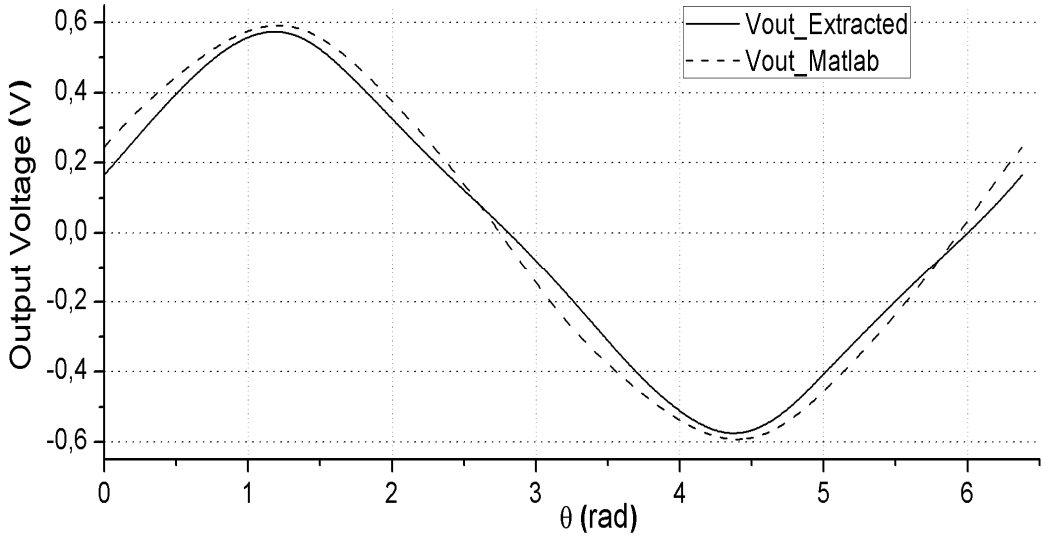




Circuit Implementation (cont'd)

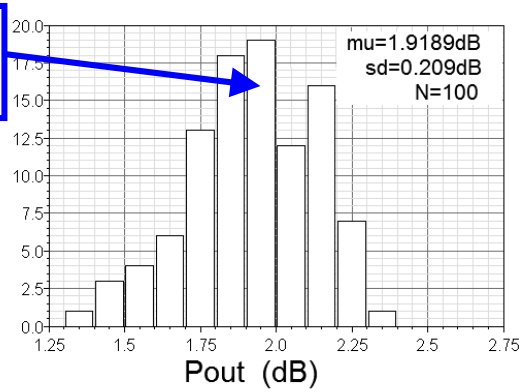
Characteristic	Post-layout simulations
V_{DD} (V)	0.65
P_{DC} (mW)	3.16
η (%)	46.6
P_{out} (dBm)	1.9
G_{pow} (dB)	26
$\hat{I}_{DC}$ (mA)	4.6
P_{harm}^{2nd} (dBc)	-67
P_{harm}^{3rd} (dBc)	-21

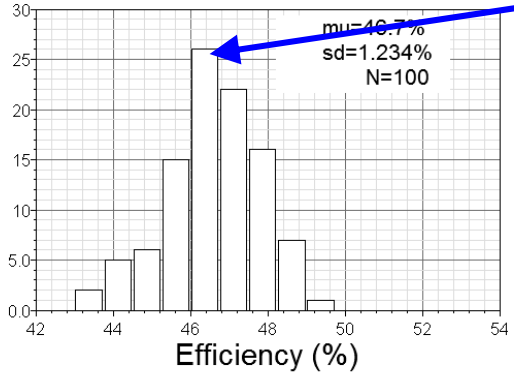
Circuit Implementation (cont'd)



Output voltage

$\overline{P}_{out} = 1.92\text{dBm}$





$\overline{\eta} = 46.7\%$

Montecarlo results for P_{out} and PA efficiency.

Comparison with other works

Ref	Techno (nm)	PA class	P_{out} (mW)	G_{pow} (dB)	PAE (%)	freq. (GHz)	FOM (W x GHz^2)
[2]	180	AB	2.2	8	14	2.4	1.45
[3]	350	Casdode +Class C	1	15	33	2.4	2.9
[4]	350	Class A + Class C	3.1	19	14	2.4	4.8
[5]	180	w/Folded Cascode	1	12	18.5	2.4	1.3
	90	**Class C**	**1.5**	**25.7**	**46.5**	**2.445**	**10.7**

[2] Khannur RFIC 2003

[3] Choi JSSC 2003

[4] Zito ICECS 2006

[5] Nguyen TMTT 2006

$$FoM = P_{out} \cdot G_{pow} \cdot PAE \cdot freq^2$$

(ITRS roadmap 2009 system drivers).

Conclusions

A compatible IEEE802.15.4 Class C PA design in 90nm CMOS is presented.

It is based on the “Design efficiency approach” presented in [1]

Post layout results and preliminary measurements show very good agreement with Matlab results.

Final design reaches interesting efficiency values and surpass the output power specification of the standard.

A Fully Differential Monolithic 2.4GHz PA for IEEE 802.15.4 based on Efficiency Design Flow

Rafaella Fiorelli
Eduardo Peralías

IMSE-CNM CSIC-Univ. de Sevilla
España

Nicolás Barabino
Fernando Silveira

GME-Univ. de la República
Uruguay

Contact: fiorelli@imse-cnm.csic.es