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All Inversion Region Design Based on g_m/I_D: the Non-linear Case of a Wake-up Receiver Radio Frequency Front-end.

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To Jimena, Julia and Antonia.

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Resumen

Las crecientes aplicaciones de Internet de las cosas y redes de sensores inalámbricos requieren la integración de módulos con consumo de energía y rendimiento optimizados. La evolución de la microelectrónica asociada a la reducción del tamaño de los transistores MOS ha permitido la viabilidad de circuitos de muy bajo consumo para la implementación de estos módulos. Un ejemplo son los receptores de despertado compuestos de dos partes principales, un bloque de radio frecuencia y un bloque de banda base. El bloque de radiofrecuencia, responsable de buena parte del consumo, consiste en un receptor muy simple compuesto por la antena y un demodulador que podría ser simplemente un detector de envolvente.

Este trabajo trata del estudio y diseño de un detector de envolvente a ser implementado usando tecnologías CMOS nanométricas para su uso en un detector de despertado para la banda de radio industrial, científica y médica (ISM) de 2.4 GHz. Los circuitos más usados que implementan esta función se basan en la característica no lineal intrínseca del transistor MOS. En esta tesis primero se muestra el origen físico y características de esta no linealidad. Luego se muestra como la elección del nivel de inversión en el cual se hace trabajar al transistor, impacta en el desempeño del detector. Por lo tanto permite seleccionar en que nivel de inversión conviene trabajar dependiendo de la o las especificaciones que se deseen priorizar, por ejemplo consumo, ganancia de conversión, relación señal a ruido (SNR). El estudio se basa en el uso de la corriente normalizada, también conocida como densidad de corriente $I_D/(W/L)$, que está relacionado con el nivel de inversión o coeficiente de inversión y la metodología g_m/I_D.

Inicialmente se realiza un desarrollo analítico complementado con modelos semiempíricos, simulaciones y mediciones, que tiene como resultado la obtención de dos novedosas figuras de mérito. Basadas en la relación entre parámetros claves, estas figuras de mérito son usadas como guía para el diseño. En particular una de ellas incluye las principales especificaciones de diseño del detector de envolvente como un bloque, a saber consumo, SNR, ancho de banda.

Usando dichos resultados se presenta el diseño de un detector de envolvente con red de adaptación integrada y un detector de envolvente mejorado, con una arquitectura novedosa, que presenta una caracteristica pasabanda intrínseca que mejora su sensibilidad. Ambos fueron fabricados en una tecnología CMOS de 0.13 μm y verificados exitosamente. Los resultados obtenidos mediante simulaciones eléctricas y medidas concuerdan razonablemente con los obtenidos con las herramientas presentadas. Se presentan medidas donde el detector de envolvente mejorado alcanza una notable ganancia de conversión con un factor de escala de 9800 V^{-1} y

una sensibilidad de -48.5 dBm para una SNR de 12dB, consumiendo 100 nA de una fuente de alimentación de 1.2 V.

El enfoque propuesto para la obtención de las figuras de mérito anteriormente mencionadas también se extiende al estudio de las características de distorsión en los transistores MOS. Se obtienen curvas características que pueden ser aplicadas como guía en el proceso de diseño de circuitos analógicos en general, en particular en el análisis de la distorsión armónica.

Summary

The growing applications of Internet of Things and wireless sensor networks require the integration of modules with optimized power consumption and performance. The very low consumption circuits for the implementation of such modules are now feasible due to the evolution of microelectronics that brought about the reduction in the size of MOS transistors. An example of such modules are wake-up receivers composed of two main parts, a radio frequency block and a baseband block. The radio frequency block, responsible for a good part of the consumption, consists of a very simple receiver composed of the antenna and a demodulator that could be just an envelope detector (ED).

This work deals with the study and design of an envelope detector to be implemented using nanometric CMOS technologies for use in a wake-up detector for the 2.4 GHz industrial, scientific and medical (ISM) radio band. The most used circuits that implement this function are based on the intrinsic nonlinear characteristic of the MOS transistor. This thesis first describes the physical origin and characteristics of this non-linearity. Then it is shown how the choice of the inversion level at which the transistor is working impacts the performance of the detector. Therefore it allows to select at which inversion level to work depending on the specification(s) to prioritize, e.g. consumption, conversion gain, signal-to-noise ratio (SNR). The study is based on the use of normalized current, also known as current density $I_D/(W/L)$, which is related to the level of inversion or inversion coefficient and the g_m/I_D methodology.

Initially, an analytical development is carried out, complemented with semi-empirical models, simulations and measurements, which results in obtaining two novel figures of merit. Based on the relationship between key parameters, these figures of merit can be used as guides for design. In particular, one of them includes the main design specifications of the envelope detector as a block, namely consumption, SNR, bandwidth.

Using these results, the design of an envelope detector with integrated matching network and an improved envelope detector, with a novel architecture that presents an intrinsic bandpass characteristic that improves its sensitivity, is presented. Both were fabricated in a 0.13 μm CMOS technology and successfully verified. The results obtained through electrical simulations and measurements agree reasonably with those obtained with the presented tools. Measurements are presented where the improved envelope detector achieves a notable conversion gain with a scale factor of 9800 V^{-1} and a sensitivity of -48.5 dBm for an SNR of 12dB consuming

100 nA from a 1.2V power supply.

The approach proposed for obtaining the aforementioned figures of merit also extends to the study of distortion characteristics in MOS transistors. This allows to obtain characteristic curves that can be applied as a guide in the design process of general analog circuits, particularly in the analysis of harmonic distortion.

List of Symbols

Physical parameters

Symbol	Description	Reference
q	Electron charge	Eq.2.11
k_B	Boltzmann's constant	Eq.2.11
T	Absolute temperature in degree Kelvin	Eq.2.11
ϵ_{si}	Permittivity of silicon	Eq.2.24
μ	Mobility of current carriers	Eq.2.6
μ_0	Low-field surface mobility	Eq.2.12
μ_z	Mobility including the effect of the vertical field	Eq.2.21
μ_{eff}	Effective mobility including the effects of the vertical and longitudinal fields	Eq.2.28
N_{ot}	Equivalent density of oxide traps	Eq.2.43
N_t	Density of oxide traps per unit volume and unit energy	Eq.2.43
γ	Attenuation coefficient of the electron wave function in the oxide	Eq.2.43

Process parameters

Γ_b	Substrate modulation factor	Eq.2.25
N_b	Doping concentration of the substrate	Eq.2.25
v_{drift}	Drift velocity of carriers	Eq.2.27
v_{sat}	Saturation value of v_{drift}	Eq.2.27

Geometry

W	Channel width	Eq.2.12
L	Channel length	Eq.2.12
x	Distance from source along the channel	Eq.2.6

Voltages and potentials

Symbol	Description	Reference
U_T	Thermodynamic voltage	Eq.2.11
Ψ_S	Surface potential	Eq.2.6
Ψ_P	Pinch-off surface potential	Eq.2.26
V_{FB}	Flat-band voltage	Eq.2.26
V_{T0}	Equilibrium threshold voltage	Eq.2.14
V_G	DC gate-to-bulk voltage	Eq.2.14
V_S	DC source-to-bulk voltage	Eq.2.16
V_D	drain-to-source voltage	Eq.2.16
V_P	Pinch-off voltage	Eq. 2.14
	Electric fields	
E_c	Critical longitudinal electric field	Eq.2.27
E_x	Electric field along the longitudinal direction	Eq.2.27
E_z	Electric field along the vertical direction	Eq.2.27
	Currents	
I_D	Static drain current flowing into the drain terminal	Eq.2.6
I_{spec}	Specific current	Eq.2.12
I_F	Static forward current	Eq.2.8
I_R	Static reverse current	Eq.2.8
i_{outbb}	Baseband output current	Eq.2.3
	Charges	
Q_i	Inversion mobile charge density	Eq.2.6
Q_{iS}	Inversion mobile charge density at the source	Eq.2.8
Q_{iD}	Inversion mobile charge density at the drain	Eq.2.8
Q_{spec}	Specific charge density	Eq.2.10

Transconductances and resistances

Symbol	Description	Reference
G_{spec}	Specific conductance	Eq.2.18
gm	Gate transconductance	Eq.2.17
gms	Source transconductance	Eq.2.16
gmd	Drain transconductance	Eq.2.16
g_{ms2}	Second order derivative of drain current respect to source voltage	Eq.2.19
g_{m2}	Second order derivative of drain current respect to gate voltage	Eq.2.20
g_{m3}	Third order derivative of drain current respect to gate voltage	Eq.4.2
g_{msovxz}	Source transconductance including the effects of the vertical and longitudinal fields	Eq.2.30
$g_{ms2ovxz}$	Second order derivative of drain current respect to source voltage including the effects of the vertical and longitudinal fields	Eq.2.31
Ro	Output resistance of a MOSFET	Eq. 2.5

Capacitances

C_{ox}	Oxide capacitance per unit area	Eq.2.7
C_{gs}	Intrinsic gate-to-source capacitance	Eq.2.44
C_{gd}	Intrinsic gate-to-drain capacitance	Eq.2.44
C_{gb}	Intrinsic gate-to-bulk capacitance	Eq.2.44

Noise

$S_{thermal} = \overline{i_{dth}^2}$	Thermal noise current power spectral density at the drain	Eq.2.38
$S_{flicker} = \overline{i_{dfl}^2}$	Flicker noise current power spectral density at the drain	Eq.2.40
$S_{inducedgate} = \overline{i_{ig}^2}$	Thermal noise current power spectral density at the gate (induced gate noise power spectral density)	Eq.2.45
$\delta_n D$	Thermal noise parameter at the drain	Eq.2.39
K_F	Flicker noise constant	Eq.2.40
f_c	Corner frequency	Eq.2.41
α	Correlation coefficient between gate and drain noise	Eq.2.46

Other

Symbol	Description	Reference
n	Slope factor	Eq. 2.7
θ	Parameter of field-dependent mobility	Eq.2.24
λ_c	Velocity saturation parameter	Eq. 2.34
λ_{ck}	Velocity saturation parameter	Eq. 2.33
L_{sat}	Velocity saturated portion of the channel	Eq.2.34
m	Modulation index	Eq. 2.2
k	Scaling factor	Eq. 2.5
G_{MN}	Matching network voltage gain	Eq. 3.2
$HD2$	Second harmonic distortion	Eq. 4.3
$HD3$	Third harmonic distortion	Eq. 4.4

Normalized symbols

$\gamma_b \triangleq \frac{\Gamma_b}{U_T}$	Normalized modulation factor	Eq.2.25
$\varphi_f \triangleq \frac{\Phi_F}{U_T}$	Normalized Fermi potential of silicon substrate	
$\psi_p \triangleq \frac{\Psi_P}{U_T}$	Normalized pinch-off surface potential	Eq. 2.26
$i_d \triangleq I_D/I_{spec}$	Normalized drain current	Eq.2.8
$i_f \triangleq \frac{I_F}{I_{spec}}$	Normalized drain current	Eq.2.8
$i_r \triangleq \frac{I_R}{I_{spec}}$	Normalized drain current	Eq.2.8
$i_{dmovxz} \triangleq I_D/I_{spec}$	Normalized drain current including the effects of the vertical and longitudinal fields	Eq.2.29
$q_i \triangleq \frac{Q_i}{Q_{spec}}$	Normalized inversion charge density	Eq.2.9
$q_s \triangleq \frac{Q_{iS}}{Q_{spec}}$	Normalized inversion charge density at the source	Eq.2.8
$q_d \triangleq \frac{Q_{iD}}{Q_{spec}}$	Normalized inversion charge density at the drain	Eq.2.8
IC	Inversion coefficient or factor	Eq.2.15
$v \triangleq \frac{V}{U_T}$	Normalized channel voltage	Eq. 2.9
$v_p \triangleq \frac{VP}{U_T}$	Normalized pinch-off voltage voltage	Eq. 2.13

List of Abbreviations

Common abbreviations

AGC	Automatic gain control
AM	Amplitude modulation
BB	Baseband
BLE	Bluetooth low energy
DTMOS	Dynamic threshold voltage MOSFET
ECC	Electronic Communications Committee
ED	Envelope detector
EIRP	Effective isotropic radiated power
ERP	Effective radiated power
ETSI	Europe the European Telecommunications Standards Institute
EU	European Union
FCC	Federal Communications Commission
FSPL	Free-space path loss
IF	Intermediate frequency
IoT	Internet of Things
ISM	Industrial, Scientific, and Medical
LNA	Low-noise amplifier
LO	Local oscillator
LUT	Look Up Tables
MAC	Medium Access Control
MN	Matching network
MOSFET	Metal-oxide semiconductor field-effect transistor
MOST	MOS transistor
OOK	On-off keying
OTA	Operational transconductance amplifier
PCB	Printed circuit board
PSD	Power spectral density
QPSS	Quasi-periodic steady state
RF	Radio Frequency
RF-MEMS	Radio-frequency microelectromechanical systems
RFID	Radio frequency identification
SAW	Surface acoustic wave
SNR	Signal to Noise Ratio

SOI	Silicon on insulator
ULP	Ultra-low power
URSEC	Unidad Reguladora de Servicios de Comunicaciones
WSN	Wireless Sensor Networks
WuRx	Wake-up receiver
WuS	Wake-up signal

Abbreviations related to MOS operation

DIBL	Drain-induced barrier lowering
MI	Moderate inversion
SI	Strong inversion
VFMR	Vertical field mobility reduction
VSAT	Velocity Saturation
WI	Weak inversion

Contents

Chapter 1

Introduction

Due to advances in wireless communications and electronics over the last decades, the development of networks of low-cost, low-power, multifunctional sensors has received increasing attention and given way to what we know today as Wireless Sensor Networks (WSN). A sensor network is designed to detect events or phenomena, collect and process data, and transmit sensed information to interested users as shown in figure 1.1. WSN are a fundamental part of the Internet of Things (IoT) [Internet of Things Community, 2015], which can be considered at a higher level. In IoT the network infrastructure is global (Internet) instead of local and the data, in addition to being processed, are analyzed. Also the "things" are not restricted to sensor nodes, they can even be virtual as long as an identity can be defined on the internet.

Figure 1.1: Applications of wireless sensor networks. Taken from [Williams, 2014]

The possible applications of WSN are countless, among others one can mention:

- Environmental applications like monitoring air pollution, forest fire detection or freshwater quality.
- Structural monitoring application in infrastructures like bridges or tunnels to monitor their movement.
- Industrial monitoring of machinery condition to generate maintenance alerts.
- Agricultural sector applications, like precision agriculture, and habitat monitoring.
- Transportation applications to collect real-time traffic information and arrange active feed regarding congestion and traffic problems.
- Health applications, to monitor physiological data such as body temperature, blood pressure, and pulse.

What mainly characterizes this type of network and differentiates them from others is the dense deployment and cooperative effort of the smart sensor nodes, the frequently changing topology, and the limitation in energy, transmit power, memory, and computing power.

The potential size of the network places two basic requirements on the hardware used to implement it, ultra-low power (ULP) consumption and low-cost implementation.

Most of the time the nodes should be in an asleep state but remain aware of the ambient environment.

Communication accounts for one of the main shares of consumption [Demirkol et al., 2009] therefore unnecessary communication is sought to be avoided and the energy used in it optimized. The WSN require the integration of Radio Frequency (RF) modules with optimized power consumption and performance [Porret et al., 2001], [Pletcher, 2008], [Mercier et al., 2022].

There are mechanisms based on communication protocols that aim to maximize the lifetime of the batteries [Lin et al., 2004]. These are based on alternate states of non-radio activity (very low power consumption, in the order of μW) and full activity modes where the radio is listening to the channel to detect requests for communication and achieve synchronization (with high power consumption, in the order of tens of mW). This is called 'Radio duty-cycle mode'. In this mode, the election of the duty-cycling ratio, the ratio of time the radio is on to the time it is off, determines the effectiveness of the protocol. Too high ratios cause what is called idle listening and is one of the main sources of consumption to eradicate. This occurs because the nodes monitor the communication medium even when there is no data to be received by the node. On the other hand, even in low data traffic scenarios, the ratio could not go too low to limit latency. So there is listening power consumption that cannot be avoided. Another requirement of this type of mechanism, which implies extra energy consumption, is time synchronization to ensure that the wake-up signal is transmitted when the sensor is awake and listening. An alternative to this would be to transmit continuously or repeatedly to ensure reception of the message, but this is detrimental to energy consumption.

A different option for this mode of operation is called 'event-triggered Radio mode' [Rabaey, 2009]. It consists in using a permanently on, very simple, auxiliary receiver in the node called a 'wake-up receiver' (WuRx) with a power consumption of about μW. This module listens to the radio channel and when it detects a certain pattern, it interprets that another radio is trying to establish communication. Then, this module wakes up the main radio and microcontroller as shown in Fig. 1.2, [Piyare et al., 2017]. In this way, the long listening channel times of the main radio are eliminated and also the MAC protocols are simplified.

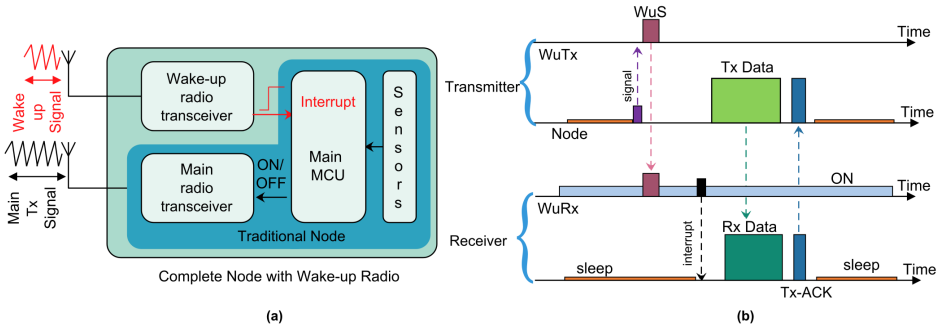

Figure 1.2: (a) Architecture of a Wireless Sensor Network with a wake-up radio. (b) Events and Timing on the node after a wake-up signal (WuS) is received. Taken from [Piyare et al., 2017]

In Fig. 1.2 the wake-up receiver and transmitter are separated from the main radio transceiver, opening the possibility that these radio links work at different frequencies. But it does not necessarily have to be like this, especially in the case where the working frequency is the same, then the wake-up signal can be generated with the main transmitter and the antenna used can be shared. Also different communication mediums, not RF-based, as acoustic [Yadav et al., 2011] [Höflinger et al., 2014] or optical [Mathews et al., 2010] [Kim et al., 2012] could be used.

Focusing on RF-based wake-up receivers the design and optimization, both in performance and cost, of the modules that compose them, particularly the RF ones becomes crucial. This cost reduction is done by means of utilizing CMOS technologies which, since a few years ago with the immense channel length reduction, have opened the path and are sufficiently evolved to be applied in RF applications. This evolution is accompanied by the need to have design methodologies and tools, that allow recognizing the link between the different design parameters and performance in a simple but efficient way. This work aims to contribute in this way by focusing on the design of a fundamental block of wake-up receivers.

1.1. Thesis Organization

This thesis is organized as follows. Initially, in subsequent sections of this chapter, wake-up receiver components, architectures, and characteristics are discussed

in parallel with a review of the state of the art. This gives way to the motivations and objectives of the work that will be presented in the following chapters.

In Chapter 2, first, the principle of operation of an active envelope detector is analyzed and the main characteristics that define its performance are presented. Then the MOS transistor model used to obtain the dependence of those characteristics as a function of the transistor bias point is revisited. After that, the said dependency is analytically obtained and confirmed with semi-empirical models, simulations, and measurements. Subsequently, a figure of merit, related to the inversion level of the transistor, to be used as a guide for design is presented. Next, an analysis is carried out regarding performance concerning noise. Starting with the transistor noise modeling, the analysis of the influence of the different types of noise present in an envelope detector, and continuing with the calculation of the signal-to-noise ratio. Culminating, a new figure of merit including the main design specifications of the envelope detector as a block, namely consumption, SNR, and bandwidth is presented. As before, the analytical results obtained are confirmed with simulation results and measurements.

Chapter 3 begins with the design of a basic envelope detector with integrated matching network. It starts with the analysis of the matching network gain and model, considering parasitics and transistor small signal components, determining the restrictions that come around for example in transistor size and bias to not degrade the MN performance. Then using the first figure of merit, obtained in the previous chapter, an estimation of the envelope detector performance is obtained and later confirmed with measurements. Next, a novel envelope detector for a wake-up receiver front-end with a tunable bandpass characteristic is proposed. The front-end is designed using the second figure of merit presented in chapter 2 to determine its performance in terms of sensitivity and consumption. Finally, the predicted design results are confirmed with measurements and compared with other works of the state of the art.

In Chapter 4 the approach proposed for obtaining the aforementioned figures of merit is extended to the study of distortion characteristics in MOS transistors. First, an overview of design methodologies that stem from the gm/ID method and that can be identified as ratio-based is presented. Then based on an analytical study and confirmed by simulations and measurements, characteristic curves are obtained. Those curves, which depend only on the inversion level, are subsequently used in the analysis of the second and third-order harmonic distortion and the results are confirmed by simulation.

Finally, Chapter 5 summarizes the contributions of this work and presents future works to carry out in the subject.

1.2. Wake Up Receivers

The efficiency of using a wake-up receiver as part of a wireless sensor network depends on several aspects of which power consumption is the most important. As previously mentioned the WURx power consumption should be several orders of magnitude lower than the main node receiver, well in the range of μW. This imposes several bounds limiting the receiver complexity and modulation schemes, which directly translates into other relevant and interconnected points to consider in the WuRx design, namely sensitivity, communication range, data rate, and time to wake-up (latency) among others.

There are a wide variety of ways to build a wireless receiver and detect an RF signal. On one hand are complex receivers that can detect signals with very high sensitivity. On the other hand are simple radio frequency identification (RFID) systems, which do not even have a power supply. Anyway, a WuRx is usually composed of two main parts: a radio frequency block and a baseband (BB) block as shown in figure 1.3.

The RF front-end is responsible for receiving and first processing the RF signal containing the wake-up message. It includes components such as an antenna, filter, matching network (MN), low-noise amplifier (LNA), and demodulator (mixer/detector). The BB back-end is responsible for the message decoding, addressing (dedicated wake-up packet for specific nodes), signal-to-noise enhancement, and making the decision to wake the node up.

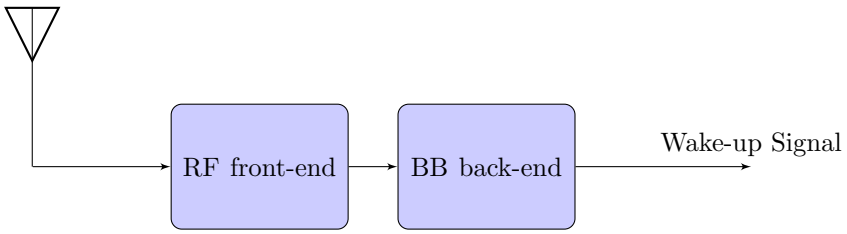

Figure 1.3: Wake-up receiver main components.

For the RF front-end block a key design parameter is the working frequency. It determines the radio link path loss and the antenna size. The antenna size in the range of only a few centimeters of the 915 MHz and 2.4 GHz ISM bands makes them very popular for WSN applications.

The free-space path loss (FSPL) formula derived from the Friss equation, assuming the Fraunhofer region and that the transmitter and receiver antennas are isotropic and with unity gain, is [Rappaport, 1996]

$$FSPL = 10log\frac{P_t}{P_r} = 10log\left(\frac{4\pi d}{\lambda}\right)^2 = 10log\left(\frac{4\pi df}{c}\right)^2 \tag{1.1}$$

where P_t and P_r are the transmitted and received power respectively, λ is the signal wavelength, f is the signal frequency, d is the distance between transmitter and receiver and c is the speed of light.

$Band$	λ	$Distance$				
-	–	$1\,m$	$3\,m$	$10\,m$	$30\,m$	$100\,m$
ISM 915 MHz	$32.8\,cm$	$31.7\,dB$	$41.2\,dB$	$51.7\,dB$	$61.2\,dB$	$71.7\,dB$
ISM 2.45 GHz	$12.2\,cm$	$40.2\,dB$	$49.8\,dB$	$60.2\,dB$	$69.8\,dB$	$80.2\,dB$

Table 1.1: Path loss and wavelength (λ) for the 915 MHz and 2.4 GHz ISM bands under free-space conditions.

Table 1.1 shows the evaluation of 1.1 for different distances for the 915 MHz and 2.4 GHz ISM bands.

Depending on the environment where the sensor network will be deployed, a more complex model to estimate the path-loss could be used, for example in [Cuiñas et al., 2010] [Martinez-Sala et al., 2005] modified models for different conditions, based on measurement campaigns, are presented.

The path loss and the maximum permitted radiated emission power for the selected frequency band determine the needed sensitivity of all systems to cover a certain range. All licensed or unlicensed devices have some limitations on the amount of output power or radiated energy, they can produce according to the local regulatory agencies. In Uruguay, the " Unidad Reguladora de Servicios de Comunicaciones " (URSEC) regulates the use of frequencies for wireless communication. In US, the Federal Communications Commission (FCC) regulates interstate and international communications. In Europe, the European Telecommunications Standards Institute (ETSI) defines the standards, and the Electronic Communications Committee (ECC) defines the frequency allocation then are translated into national law by all European Union (EU) countries. Non-EU members may use these standards for regulatory purposes.

The means of describing this limit differs among the various regulatory agencies. Radiated energy can be described in terms of the electrical field strength (E) measured at some distance from the radiator, the effective isotropic radiated power (EIRP), or the effective radiated power (ERP). The relations between those are:

$$EIRP = 10log\left(\frac{4\pi E^2 d^2}{0.377\,[V^2]}\right) = 10log\left(\frac{E^2 d^2}{0.03\,[V^2]}\right) \tag{1.2}$$

where d is the distance from the transmitting antenna as in 1.1, V is the unit of measurement (Volts) and the resulting EIRP is in dBm.

$$ERP = EIRP - 2.5\,dB \tag{1.3}$$

Power limits depend on the type of modulation. For example from [Loy et al., 2005], that condenses [Federal, 2009] sections 15.247 and 15.249, the power limits for the 2.4 GHz ISM band are summarized in table 1.2.

For the case of no frequency hopping nor digitally spread signal (Other in table), transmit strength can be up to 20 dB larger than the limits for continuous signals presented in table (-1.23 dBm) if the transmitter is activated in short bursts only. This is because of the power measurement procedure specification, also described in the standard. Above 1 GHz, an averaging detector is used. This detector

Transmission Type	**Fundamental**		**Harmonics**	
	E at 3 m	EIRP	E at 3 m	EIRP
Frequency hopping		≥75 channels: 36dBm	20 dB below the peak in−band emission in any 100 kHz bandwidth	
		<75 channels: 30dBm		
Digitally spread		36 dBm		
Other	50 mV/m	-1.23 dBm	500 $\mu V/m$	-41.23 dBm

Table 1.2: Transmit Power Limits for the 2.4 GHz ISM band [Loy et al., 2005].

should have a resolution bandwidth of 1 MHz and average the measurement results over a period of 100 ms. In all cases where an averaging detector is specified, an additional measurement using a quasi-peak detector, described in [IEC, 2010], has to prove that the peak emission is not more than 20 dB higher than the average emission. For example, if the transmitter in a 100 ms period is duty cycled by a 10 factor, the peak power could be 10 times larger than the limits would be if the transmitter were on for the full 100 ms averaging window. It is worth adding that the values presented in the table are also those that apply in Uruguay. Then for a 30 m range, considering the 69.8 dB path loss at 2.45 GHz from table 1.1, in the best scenario of maximum transmitted power (-1.23 dBm + 20 dB = 18.77 dBm) , the receiver sensitivity should be -51 dBm considering 0 dB receiver antenna gain.

As shown in table 1.2, given that spread spectrum and frequency hopping systems are less likely to interfere with other systems than are single frequency transmitters, higher output power is allowed for transmitters using this kind of modulation. Wi-fi and Bluetooth standards fall into this category.

Since standards impose rigorous frequency control, channelization, and other constraints, WuRXs that are fully compatible with standards tend to consume more power than proprietary WuRXs, making them inappropriate. An alternative that permits to use of the main standard transmitter is a technique called back-channel communication [Kim and Wentzloff, 2016], [Roberts et al., 2016]. Whereby carefully sequenced data bit streams from already-deployed infrastructure, like WiFi or Bluetooth Low Energy (BLE), generate packets that look like a lower complexity, lower bandwidth waveform that is more readily detectable by a low-power WuRX. Most of the implementations that use this approach end up consuming more power than a WuRX that is not standards compatible [Mercier et al., 2022].

1.2.1. RF front-end

A general architecture of the RF front-end of figure 1.3 is presented in figure 1.4. In that figure, the optional block named LNA stands for low noise amplifier, and the ED block for envelope detector.

The first component is a matching network responsible for matching the impedance to the input source, i.e. the antenna, and providing an RF filter to remove out-of-band noise and interfering signals. Additionally, as it will be seen in section 3.1, the matching network may provide passive voltage gain improving the

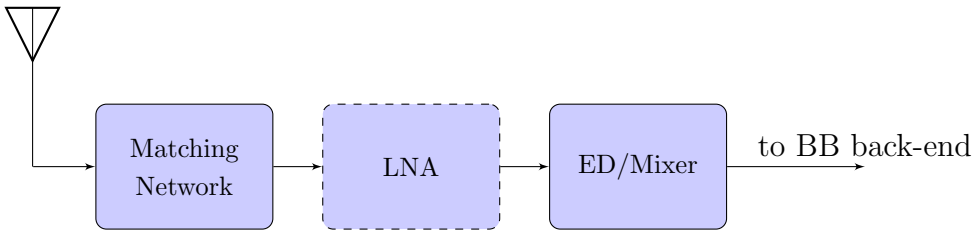

Figure 1.4: RF front-end components.

resulting sensitivity.

For the MN implementation there is a trade-off between integrated and external components, especially inductors. The use of integrated inductors reduces both size and cost and improves reliability and miniaturization but its quality factor is typically lower (5-10) than the commercial off-chip inductors (30-50) in the GHz frequency range. In figure 1.5 the quality factor of commercial off-chip inductors as a function of frequency and for several inductance values is presented [Coilcraft, 2023]. Anyway, in this frequency range, the use of external inductors is limited or not so efficient because high-Q nodes are sensitive to component variations.

The resonant frequency deviates due to tolerances in off-chip components and parasitic capacitances and inductances, which mainly depend on the packaging and the board [Darabi and Abidi, 2000], [Abidi et al., 2000], [Pletcher, 2008]. So the use of external inductors, must be accompanied by manual or automatic tuning to compensate for parasitics and tolerances and reduce center frequency or gain variations of the matching network response.

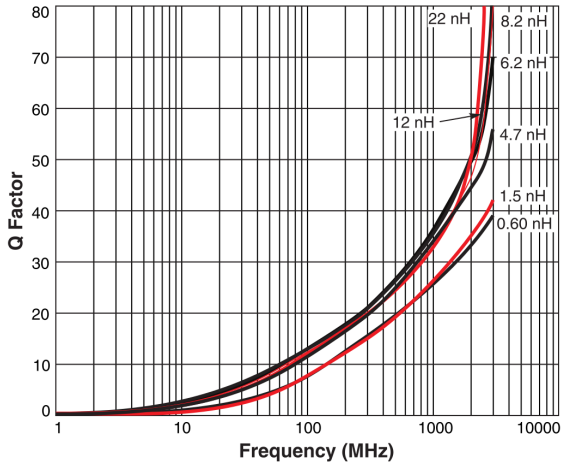

Figure 1.5: Coilcraft chip inductors 0201CT Series quality factor. Taken from [Coilcraft, 2023].

As an alternative or as a complement to on-chip passives and traditional off-chip passive components mounted on the printed circuit board (PCB), radio-frequency microelectromechanical systems (RF-MEMS) like surface acoustic wave (SAW) filter could be used [C. Hambeck, 2011], [Cheng et al., 2012]. Such filters

strongly enhance the receiver immunity to strong out of band signal interferences because of their out-of-band rejection typically in the order of 20 dB - 40 dB. Information on those devices is obtained from their manufacturers, for example, Kyocera [Kyocera, 2023] or Murata [Murata, 2023]. Aside from cost, the main drawback of using these components is the insertion loss normally in the order of 1dB to 3 dB. In the case of analog front-ends based on square-law detectors, if the baseband noise is dominant, a 3 dB loss results in 6 dB worsened SNR at the baseband output as will be shown in section 2.5.3.

The optional second component in figure 1.4 is a low noise amplifier. The purpose of this stage is to increase the sensitivity of the receiver by amplifying weak signals while meeting noise requirements.

The receiver sensitivity is not directly related to the LNA characteristics. It depends among other factors on the detector type that follows, the RF bandwidth determined by the matching network or filter, and the baseband bandwidth. In [Huang et al., 2013] an analysis of the sensitivity in this kind of architecture considering a square law detector is presented. This topic will be addressed in section 2.5.2.

Given that this block is working at high frequency, it generally dominates in terms of power consumption. Being in the order of microwatts-to-milliwatts and increasing as frequency increases.

For example in [Pletcher et al., 2007] a WuRx for 1.9 GHz operation including a LNA is presented. The measured sensitivity was -50 dBm, for SNR = 12 dB and a data rate of 40 kbps. The total power consumption from the 0.5 V supply is 65 μW with the LNA consuming approximately 75 % (48 μW) of the total. In [Huang et al., 2010] a WuRx for 915 MHz and 2.4 GHz including LNA and using a double sampling technique to improve noise rejection was presented. The sensitivity was -64 dBm and -69 dBm at 2.4 GHz for 100 kbps and 10 kbps respectively and -75 dBm y -80 dBm for 915 MHz, the SNR considered in all cases was 12 dB. The total power consumption was 51 μW (27 μW LNA, 5μW EnvDet).

The third component in figure 1.3, responsible for carrying out the demodulation of the signal, is an envelope detector or a mixer.

The use of a mixer is associated with conventional heterodyne architectures, where an on-chip local oscillator (LO) signal is used to mix down the RF signal to an intermediate frequency (IF) or directly to baseband. At intermediate frequency or baseband the amplification and noise or interference filtering is more power-efficient. Particularly in the case of moving to an intermediate frequency, this frequency can be selected to reduce 1/f noise influence. However, the need to use a tunable and high accuracy LO signal, implies considerable power consumption.

If power levels in the order of 10 μW - 100 μW are acceptable the use of these architectures is appropriate.

Given the modulation and channelization complexity, back-channel WuRx are good candidates to use this type of architecture. The implementations end up using a mixer as a demodulator and an LNA to improve sensitivity [Wang and Mercier, 2021], [Salazar et al., 2016], [Im et al., 2020].

Reaching very good sensitivity results (-90 dBm to -100 dBm) and data rates

in the order of 10 kbps - 100 kbps, the power consumption of this type of WuRx is in the order of hundreds of μW (100 μW - 500 μW), with the LNA and LO generation occupying around 70-80 % of the power budget.

A version with a consumption of less than 100 μW without LNA for 2 GHz is presented in [Pletcher et al., 2009]. The authors propose a super-heterodyne receiver with uncertain IF architecture as shown in figure 1.6. The RF signal is mixed with an LO whose frequency is not well-defined. Generated using a free-running ring oscillator with a relaxed phase noise and frequency accuracy specifications and so lower power consumption.

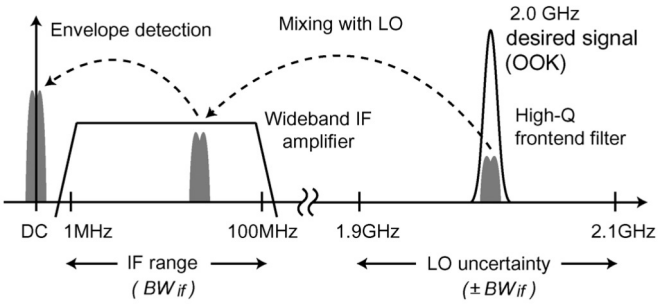

Figure 1.6: Uncertain-IF receiver frequency plan and method of operation. Taken from [Pletcher et al., 2009]

It achieves a medium sensitivity of -72 dBm at 100 kbit/s data rate and the power consumption is 52 μW from a 0.5 V supply. LO and mixer account for 50 % of the power consumption and IF amplifier for 40 %. The wide IF bandwidth required for detection, because of the lack of accuracy in the LO frequency, implies a wide noise equivalent bandwidth reducing the receiver sensitivity and increasing susceptibility to interference.

An alternative to reduce power consumption is the use of a direct-ED architecture, where the input RF signal is applied straight to an envelope detector to perform the demodulation to baseband.

This option can be implemented without using other active RF circuits (LNA, mixer, LO oscillator) that increase the power budget. The disadvantage, because of the non-coherent envelope detection, is the limitation on the possible types of modulation used. Usually, simple amplitude modulation schemes such as on-off keying (OOK), are used in this type of architecture. Furthermore, the filtering of the desired RF signal becomes very important, or else the detector will simultaneously demodulate several signals, degrading interference rejection. The envelope detector types for this use, along with the presentation of some designs that use them, are summarized in the following section.

1.2.2. Envelope Detectors

The architecture and type selection along with the design of the envelope detector has a significant impact on the sensitivity and power consumption of the

RF-front-end.

ED circuits are intrinsically nonlinear, when input signals are not sufficiently strong they operate under a square law regime [Wetenkamp, 1983], where the output voltage level is proportional to the input RF power level, this topic will be addressed in section 2.1.

Envelope detection can be obtained passively by a single rectifier diode or actively via a low-power amplifier biased to enhance second-order nonlinearities.

Passive envelope detectors

Generally in passive envelope detectors, to increase the output signal, several single-stage diode detectors are combined. Multi-diode circuits are based on voltage doublers ('charge-pump'). The two most used configurations for multistage detectors are the Dickson [Dickson, 1976] and the Villard [Villard, 1901] configuration shown in figure 1.7.

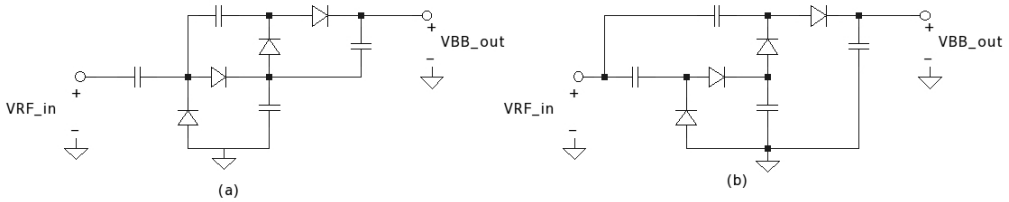

Figure 1.7: (a) Villard multiplier and (b) Dickson multiplier.

Several of these stages could be cascaded multiplying by 4 in each one. An important point to mention is that in practice this multiplication factor is affected by the diode and stray capacitances [Dickson, 1976]. In standard CMOS process the diodes are obtained with diode-connected MOSFETS, but in other processes such as SiGe BiCMOS technology Schottky diodes can be used.

Although a passive N-stage RF rectifier is a tempting solution considering it consumes no power and does not suffer from $1/f$ noise the presented real part of the input impedance of the detector is extremely high. So it is hardly possible to match the antenna's commonly 50 Ω impedance with low loss in the matching network and with a low reflection coefficient. This becomes impossible if the matching network must be integrated and the working frequencies are above 1 GHz. Also the increase in the number of stages to improve gain increases the rise time of the multiplier and the parasitic capacitances reducing the achievable baseband bandwidth and consequently the data rate. To reduce the impedance the diodes could be biased but in this case, the advantages previously mentioned about power consumption and noise are reduced.

Below are some works that use this type of detector, indicating their main characteristics.

In [Oh et al., 2013] a WuRX for the 402-405 MHz MICS band and the 915 MHz and 2.4 GHz ISM bands using a 30-stage passive ED implemented with zero-threshold transistors is presented. The obtained sensitivities for each band were -45.5 dBm, -43.4 dBm, and -43.2 dBm respectively, using an external matching network with a 5dB voltage gain and achieving a data rate of 12.5 kbps. The power consumption was 116 nW. Although the consumption is encouraging, the sensitivity achieved is quite low considering the use of an external matching network.

The authors in [Moody et al., 2018] present a WuRx with a 45-stage passive ED. The achieved sensitivity was -76 dBm in the 151.8 MHz MURS band and -71 dBm in the 433 MHz ISM band while consuming 7.4 nW. The obtained data rate is 0.2 kbps and the used external matching networks have a 27 dB and 25 dB voltage gain for each band respectively. Again the consumption results are very good but the sensitivity and data rate not so much adding the fact that the frequency used implies antenna sizes are not very small and that the matching network is external.

Active envelope detectors

Given the limitations of passive EDs regarding achievable data rates, active EDs are preferable when medium or high data rates are required.

As previously mentioned active envelope detectors are ULP amplifiers biased to enhance second-order nonlinearities. In section 2.1 the possible configurations to accomplish it will be presented, basically they are the same configurations in which a transistor can be connected as an amplifier.

Next, a review of WuRx implementations that make use of active EDs are presented analyzing its main characteristics and results.

The WuRx reported in [C. Hambeck, 2011] for the 868 MHz ISM band, makes use of an active ED achieving a -71 dBm sensitivity for a 100 kbps data rate (OOK modulation) while consuming 2.4 μW from a 1.0 V power supply. The ED consumes 1 μW. The total external matching network voltage gain, including the insertion loss of an input SAW filter for out-of-band interference suppression, was 21 dB. The other improvement in sensitivity is obtained by baseband correlation over 7 ms with a 64-bit pattern, this coding gain of up to 33 dB it can be shown that it is halved when considered at the input due to the square-law detector input-output characteristic.

Consumption and sensitivity results are good, and the latency introduced by the baseband coding is not too high. Clearly to achieve the desired transfer rate a trade-off arises between latency, coding gain, and the baseband bandwidth.

In [Cheng and Chen, 2017] a receiver fabricated in 0.18 μm CMOS technology to operate at 2.4 GHz is presented. The receiver achieves a - 50 dBm sensitivity at a data rate of 200 kbps (OOK modulation) while consuming 4.5 μW from a 0.8 V supply voltage. The ED architecture used is a differential one and the matching network was integrated with a gain of 12.5 dB. Differential input requires the use of an external balun. The total power consumption of the detector including the biasing circuit is 2.4 μW, 3 μA from 0.8 V of which 1 μA corresponds to the differential detector.

Considering that the adaptation network is internal and that there is no improvement in sensitivity through baseband processing (coding), the sensitivity and consumption results are good. A questionable aspect is the need for an external balun, which would increase costs.

The authors in [Wang et al., 2018] propose a WuRx, fabricated in a 180 nm silicon on insulator (SOI) CMOS process, that operates at 113.5 MHz and achieves a sensitivity of -69 dBm at a data rate of 300 bps while consuming 4.5 nW from a 0.4 V supply. The active envelope detector makes use of dynamic threshold voltage MOSFET (DTMOS) configuration transistors [Assaderaghi et al., 1997] to improve nonlinearity. The bias of the envelope detector transistor is implemented using a pseudoresistor forming an active-L load. To account for process variation an 8-bit binary weighted tuning capability for the envelope detector branch transistors (ED and bias) and 5 bit scheme for the pseudoresistor are used. The external matching network provides a 25 dB voltage gain and the baseband processing another 2 dB coding gain. The power consumption results are very good but the data rate is low and the frequency used implies antenna sizes are not very small. The matching network is external.

1.2.3. Base Band back-end

As previously stated BB back-end is responsible for signal-to-noise enhancement, message decoding, addressing (dedicated wake-up packet for specific nodes), and making the decision to wake the node up. All of the above is developed in baseband, that is, in low frequency and a good part in the digital domain. So that consumption is greatly reduced compared to the previously analyzed blocks intended to work in RF.

Even though the implementations may have different architectures, some components can be identified according to their functions as can be seen in the figure 1.8.

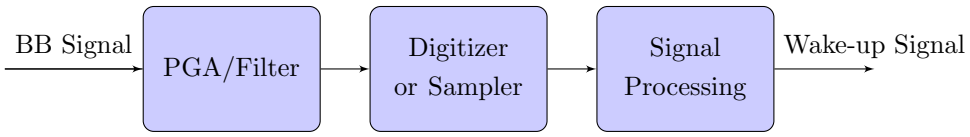

Figure 1.8: Baseband back-end components.

After demodulation, the baseband signal is amplified and filtered previously to be digitized/sampled. Usually, the amplification is programmable and with automatic gain control (AGC) to manage different signal strength cases without saturating. Carried out in several cascaded stages with the biggest gain in the first, so the noise of subsequent gain stages contributes much less to the overall noise figure and thus, they can operate with much reduced current consumption.

For example in [Pletcher et al., 2007] a PGA with digitally programmable gain settings between 18 dB and 50 dB and a bandwidth of 150 kHz is used, consuming 2.5 μW which represents less than 4 % of the total WuRX consumption.

The authors in [C. Hambeck, 2011] make use of a baseband amplifier chain with a second-order low-pass filter. Two PGAs provide 14 to 24 dB of gain each, a bandwidth of 700 kHz, and consume 200 nW (8 % of the total). In [Cheng and Chen, 2017] a baseband amplifier with a 3 dB bandwidth of 1.4 MHz, gain of 33 dB, and a power consumption of 0.9 μW (20 % of the total) is used.

The signal processing block of figure 1.8 concentrates different functions that, depending on the implementation, can be carried out in the digital, analog, or mixed domain. Among these functions can be mentioned sensitivity enhancement through the use of coding and addressing. Both mentioned functions can be implemented at the same time if individual codes are used for each sensor node. The trade-off of using coding to enhance sensitivity is the increase in latency. In a first approximation with the assumption of statistical independence of noise, the standard deviation is reduced by $\sqrt{N}$, where N is the number of bits of the code. So the code length directly determines coding gain. As previously mentioned in the case of square-law detectors the coding gain is translated to sensitivity enhancement root squared or if considered in dB divided by 2.

For example in [Wang et al., 2018] the output of the ED is digitized by a comparator, which serves as a 1-bit quantizer and provides the input to the digital baseband correlation logic that processes the incoming data. The correlator and the output driver to generate the wake-up signal are shown in figure 1.9, a 2x oversampling rate is used to sample the incoming bits. An optimal 16-bit code sequence is selected with a large Hamming distance from all of its shifted versions and from the all-0 sequence. As the input sequence shifts along the D flip-flop chain, the correlator computes the Hamming distance between the sequence and the programmable 32-bit oversampled code book. Once the value is below a preset threshold, the pattern is declared detected and the correlator generates a wake-up signal. The reported consumption of this block was 0.77 nW at 300 bps in 180 nm SOI CMOS process. In [Moody et al., 2018] a similar 8-bit correlator is used.

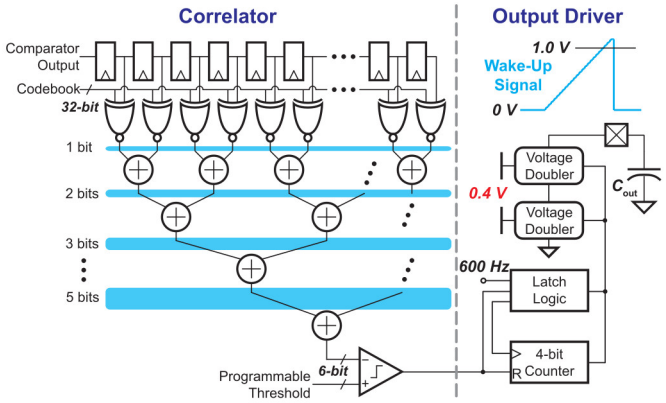

Figure 1.9: Digital correlator baseband logic with a wake-up signal output driver. Taken from [Wang et al., 2018]

In [C. Hambeck, 2011] a parallel mixed analog/digital approach is used as

shown in figure 1.10. A correlation unit with a switched capacitor principle is deployed, and also 2x oversampling rate is used. It includes 128 parallel correlation stages that have one common wired-OR output. Each stage is operated with a bit-shifted version of the pattern sequence. The sampled charge is transferred to either C_{P0} for positive bits or C_N0 for negative bits of the pattern filter output. Figure 1.10 (b) illustrates the generation of control signals for the switches. Since the ratio of $C_{P0,N0}/C_{S0}$ is chosen high, up to 700 samples are accumulated and averaged permitting consecutive sequences correlation to improve correlation gain. The correlation result is the voltage between C_{P0} and C_{N0}. It is evaluated using a comparator and a digital-to-analog converter once per pattern period to save power. All the architecture consumes only 0.4 μW at 200 kS/s in a 130 nm CMOS process.

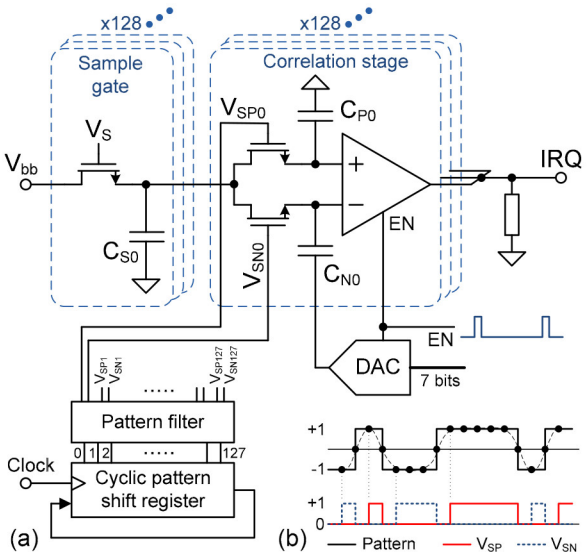

Figure 1.10: (a) Block diagram of correlation unit and (b), generation of pattern dependent control signals for MOS switches. Taken from [C. Hambeck, 2011]

1.3. Motivation

From the previous sections, it is clear that the direct-ED architecture is one of the most promising in terms of consumption-sensitivity trade-offs in particular those that make use of active detectors. This is confirmed also in recent surveys and analysis works like [Mercier et al., 2022] and [Piyare et al., 2017].

An important aspect that affects the performance of active envelope detectors is the bias point selection. In this sense, the works that analyze the characteristics of envelope detectors [Vittoz and Fellrath, 1977] [Simone Gambini and Rabaey, 2008] [Nilsson and Svensson, 2011] [Pletcher, 2008] or the implementations reviewed in 1.2.2 [C. Hambeck, 2011] [Wang et al., 2018] [Cheng and Chen, 2017], always consider the transistor that fulfills the detector function as working under

the exponential current-voltage characteristics in the subthreshold zone. Or from the point of view of design-oriented models based on the inversion charge of the transistor [Enz et al., 1995] [A. I. A. Cunha and Galup-Montoro, 1995], in the region known as weak inversion.

It is then of interest to address the origin of these nonlinearities and their dependence on the bias point or inversion zone, not only in a specific one but for all inversion regions. In this way, the best bias point choice can be determined depending on characteristics to be prioritized in the design, for example, consumption or gain.

It would also be desirable to have tools that, in the quickest and easiest way possible, allow us to visualize the link between said choice and other fundamental parameters such as the SNR of the detector.

Last but not least, it is important to confirm the results experimentally with the design, fabrication, and characterization of a fully integrated RF front-end prototype. For this prototype, the selected frequency, for the antenna size aspect previously mentioned, is 2.4 GHz ISM band. Also motivated by the cost-effective and failure points reduction, the total integrated option even for the matching network will be considered.

Chapter 2

MOS transistor modeling tools for envelope detector design.

This chapter aims to provide the basis for the design of a MOS envelope detector for WuRX. Initially Section 2.1 presents and compares different circuit configurations and the main equations and metrics that characterize envelope detector properties. Section 2.2 briefly presents the MOS transistor model used. The physical characteristics of the transistor that will impact the envelope detector operation and performance are highlighted. In Section 2.3 the second derivative behavior as a key design variable is analyzed through simulations and measurements. Section 2.4 proposes a novel figure of merit to aid the design that only depends on the inversion level. Section 2.5 presents the noise in MOS transistors and the equations that describe the noise characteristics of the ED due to different contributors. Subsequently in Section 2.6 the Signal to Noise Ratio of the ED is analyzed and a new figure of merit, which also only depends on the inversion level, is proposed. The main contributions presented in this chapter are published in [Reyes and Silveira, 2015], [Reyes and Silveira, 2018].

2.1. Circuit Analysis

The circuit in Fig. 2.1 is a popular form of an active RF envelope detector and is a MOS transistor (MOST) implementation of the bipolar version presented in [Meyer, 1995]. The voltage-current nonlinear characteristic of transistor M1 is what makes possible the demodulation of the RF signal.

Transistor M1 implements a source follower where C is sized so that the output bandwidth $\left(\frac{g_m}{2\pi C}\right)$ is much smaller than the RF input signal frequency.

Under the assumption of weak nonlinearity, considering small amplitudes of the RF signal at the transistor gate, taking the Taylor expansion around the bias current I_{D0} and neglecting the terms of order higher than two, the drain current can be expressed as

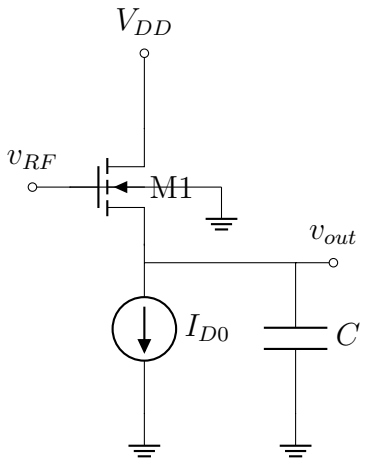

Figure 2.1: Common drain envelope detector schematic.

$$i_D \cong I_{D0} + \left(\frac{\partial I_D}{\partial V_G}\right) v_g + \left(\frac{\partial^2 I_D}{\partial V_G^2}\right) \frac{v_g^2}{2} \tag{2.1}$$

where v_g is the ac component of the gate voltage v_{RF}.

The contribution of the nonlinearity due to the drain-source voltage variation to the conversion can be considered negligible because the high-frequency input signal is largely attenuated at the output.

The amplitude of the demodulated current signal will be proportional to v_g^2 which appears multiplied by the second derivative of I_D with respect to V_G.

Given an amplitude-modulated (AM) signal at the input, defined as

$$v_{RF} = v_{in}(1 + m.sinw_m t)cosw_c t \tag{2.2}$$

where w_m is the modulation angular frequency, m is the modulation index, and v_{in} is the amplitude of the RF carrier at the gate. The amplitude of the baseband output current at angular frequency w_m can be expressed as

$$i_{outbb} = \left(\frac{\partial^2 I_D}{\partial V_G^2}\right) \frac{v_{in}^2.m}{2} \tag{2.3}$$

To evaluate the performance of the envelope detector, a voltage conversion gain VC_{Gain} and a scaling factor k are defined as:

$$VC_{Gain} = \frac{v_{outbb}}{v_{in}} = \left(\frac{\partial^2 I_D}{\partial V_G^2}\right) \frac{v_{in}.m.R_o}{2} \tag{2.4}$$

$$k = \frac{v_{outbb}}{v_{in}^2} = \left(\frac{\partial^2 I_D}{\partial V_G^2}\right) \frac{m.R_o}{2} \tag{2.5}$$

where R_o is the circuit output impedance. Current conversion gain and current scaling factor could be also defined, the expressions are the same as 2.4 and 2.5 without R_o.

In the case of a source follower, the baseband output impedance is $1/g_m$, and so the voltage conversion gain and scaling factor are low. To increase them, alternatives such as the common gate or common source architectures shown in 2.2 could be used. In both cases, the output impedance is $1/g_{ds}$.

The expression for the drain current is equal to Eq 2.1 for the common source. For the common gate, the derivatives and dependence are obtained by replacing V_G with V_S. As previously C is sized so that the output bandwidth $\left(\frac{g_{ds}}{2\pi C}\right)$ is much smaller than the RF input signal frequency.

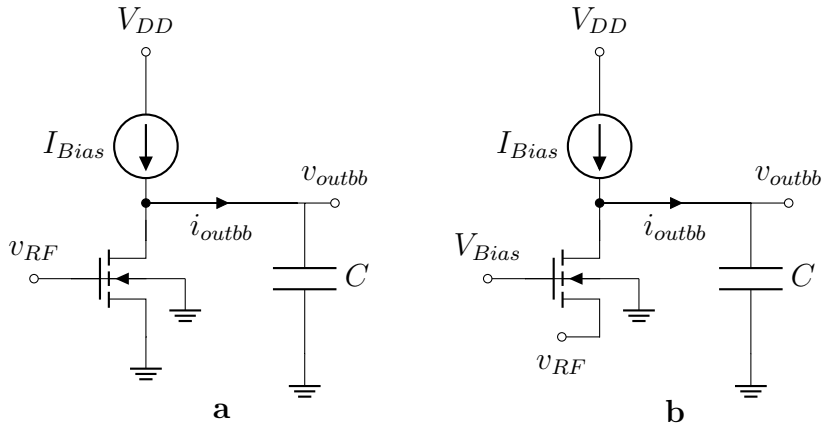

Figure 2.2: Common source (a) and common gate (b) envelope detector schematic.

In this work the common gate circuit of Fig. 2.2 is chosen. A common gate topology takes advantage of the increased coupling to the channel of the source terminal with respect to the gate terminal. Or, from an equivalent point of view, of the joint action of the front gate and the bulk operating as a "back gate".

As will be shown the second derivative for the drain current in saturation with respect to V_S is approximately n^2 times bigger than the second derivative for the drain current with respect to V_G, with n the sub-threshold slope factor [Enz and Vittoz, 2006]. An example of that is shown in the measured results of Fig. 2.3. Therefore common source and drain topologies achieve less current conversion gain than the common gate configuration.

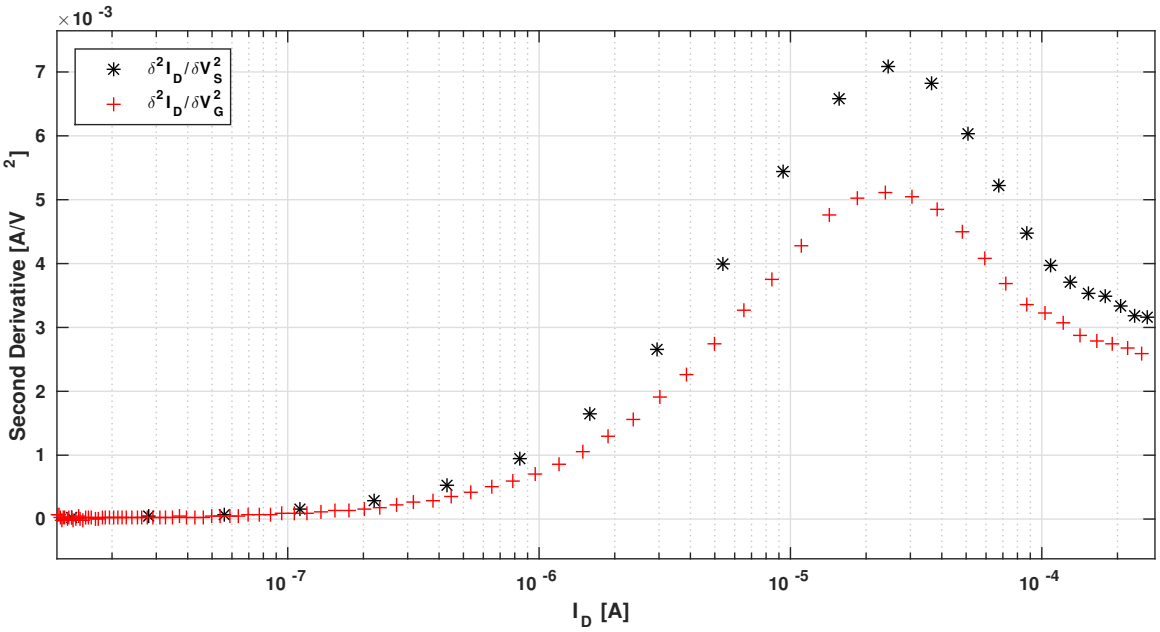

Figure 2.3: Measured Second Derivative comparison $\left(\frac{\partial^2 I_D}{\partial V_S^2}\right)$ and $\left(\frac{\partial^2 I_D}{\partial V_G^2}\right)$ for W = 10 μm, L = 1 μm, $V_{DS} = 0{,}6V$.

2.2. Analysis based on compact model

From the design point of view, as shown in 2.1, given the dependence of the conversion gain and scaling factor on the second derivative, it's important to know its behavior as a function of the transistor bias point. For a theoretical analysis, given its accuracy in describing the physical phenomena and its simplicity, a compact model like EKV [Enz and Vittoz, 2006] or ACM [A. I. A. Cunha and Galup-Montoro, 1998] [Galup-Montoro and Schneider, 2007] is useful. Following the EKV MOS transistor model is selected and a brief outline of it is presented closely following [Enz and Vittoz, 2006].

The currents to voltages relationships are obtained from the charge-sheet expression 2.6 [Tsividis, 2011], [Brews, 1978] and the approximation of the linear dependence of the inversion charge density on the surface potential [Maher and Mead, 1987] for a constant gate-to-bulk voltage 2.7.

$$I_D = \mu W \left(-Q_i \frac{d\Psi_S}{dx} + U_T \frac{dQ_i}{dx} \right) \tag{2.6}$$

$$dQ_i = nC_{ox} d\Psi_S \tag{2.7}$$

In 2.6 μ is the mobility, W is the channel width, Q_i is the inversion charge density, Ψ_S is the surface potential and x is the coordinate along the channel length. The first term could be identified as the drift component of the current, propor-

tional to longitudinal electric field $\frac{-d\Psi_S}{dx}$, and the second term as the diffusion component, proportional to the gradient of the charge concentration $\frac{dQ_i}{dx}$.

In 2.7 C_{ox} is the oxide capacitance per unit area, and n is the slope factor.

The core equations of the model in its normalized form [Enz and Vittoz, 2006] are:

$$i_d = i_f - i_r = q_s + q_s^2 - q_d - q_d^2 \tag{2.8}$$

and

$$2q_i + \ln q_i = v_p - v \tag{2.9}$$

Where q_i is the inversion charge density, q_s and q_d are this charge density evaluated at the source and drain respectively. All of them are normalized to the specific charge

$$Q_{spec} \triangleq -2nC_{ox}U_T \tag{2.10}$$

U_T is the thermal voltage

$$U_T = k_B T/q \tag{2.11}$$

In 2.8 the drain current is expressed in terms of two components that preserve the structural source-drain symmetry, where i_f is a source-related forward current and i_r is a drain-related reverse current both normalized to the specific current

$$I_{spec} \triangleq 2n\mu_0 C_{ox}\frac{W}{L}U_T^2 \tag{2.12}$$

μ_0 is the constant low-field electron mobility and W and L are the transistor width and length respectively.

In 2.9 v_p and v are the pinch-off 2.13 and channel voltages normalized to U_T.

$$v_p \triangleq \frac{V_P}{U_T} \triangleq v|_{q_i|_{(2q_i+\ln q_i=0)}} = v|_{q_i=0{,}4263} \tag{2.13}$$

$$V_P \approx \frac{V_G - V_{T0}}{n} \tag{2.14}$$

where V_{T0} is the threshold voltage in equilibrium, corresponding to the value of V_G for which V_P is equal to zero.

The previous normalization makes the equations 2.8, 2.9 independent of technology or size and allows the introduction of the inversion coefficient concept IC

$$IC = max\,(i_f, i_r) \tag{2.15}$$

which directly relates to the inversion channel establishment, strongly or weakly established, and so if the dominant method of conduction is drift or diffusion.

In forward saturation, when $q_d \approx 0$ and so the reverse current is negligible compared to the forward current $i_f \gg i_r$, $i_f = 0{,}1$ is considered the limit for the

weak inversion (WI) region and $i_f = 10$ a lower bound for strong inversion (SI) operation. The region in between is known as moderate inversion (MI).

Using equations 2.8 and 2.9 is straightforward to obtain the transconductance values

$$g_{ms(d)} = -(+)\frac{\partial I_D}{\partial V_{S(D)}} = G_{spec} q_{s(d)} \tag{2.16}$$

$$g_m = \frac{\partial I_D}{\partial V_G} = \frac{G_{spec} q_s}{n} \tag{2.17}$$

$$G_{spec} = \frac{I_{spec}}{U_T} \tag{2.18}$$

and the, previously mentioned in section 2.1, second derivatives with respect the source or gate voltage

$$g_{ms2} = \left(\frac{\partial^2 I_D}{\partial V_S^2}\right) = \frac{G_{spec}}{U_T}\frac{q_s}{(2q_s+1)} \tag{2.19}$$

$$g_{m2} = \left(\frac{\partial^2 I_D}{\partial V_G^2}\right) = \frac{G_{spec}}{n^2 U_T}\frac{q_s}{(2q_s+1)} \tag{2.20}$$

By inspection of 2.19 the second derivative with respect to the source increases with the inversion charge or equivalently with the inversion level, asymptotically to $\frac{G_{spec}}{2U_T}$.

This demeanor is unrealistic because the second derivative decreases as the inversion level increases, as shown in Fig. 2.3. Next, we will show that this is due to the effect of Vertical Field Mobility Reduction (VFMR) and Velocity Saturation (VSAT).

Vertical field mobility reduction and velocity saturation effects

The VFMR and VSAT effects can also be modeled as a function of the inversion charge [Enz and Vittoz, 2006], [da Silva et al., 2008], [Schneider and Galup-Montoro, 2010], [Pino-Monroy et al., 2022].

The vertical field E_z effects are represented in [Enz and Vittoz, 2006] in a mobility μ_z with the form:

$$\frac{\mu_z}{\mu_0} = \frac{1}{k_1 q_i + k_2} \tag{2.21}$$

with $k1$ and $k2$

$$k_1 = \theta\left(\frac{1}{2} - \frac{1}{1+\frac{2}{\gamma_b}\sqrt{\psi_p}}\right) \tag{2.22}$$

$$k_2 = 1 + \frac{\theta\psi_p}{1+\frac{2}{\gamma_b}\sqrt{\psi_p}} \tag{2.23}$$

where

$$\theta = \frac{Q_{spec}}{\epsilon_{si} E_0} \tag{2.24}$$

with ϵ_{si} the permittivity of silicon and $E_0 \cong 4$ x $10^7\, V/m$ the electric field at which the mobility starts to decrease significantly.

γ_b is the normalized substrate modulation factor

$$\gamma_b = \frac{\Gamma_b}{U_T} = \frac{\sqrt{2qN_b\epsilon_{si}}}{C_{ox}U_T} \tag{2.25}$$

where N_b is the doping concentration of the substrate.

ψ_p is the normalized pinch-off surface potential, defined as the normalized surface potential ψ_s for which the inverted charge becomes zero

$$\psi_p = \frac{\Psi_P}{U_T} \triangleq \frac{\Psi_S\left(Q_i = 0\right)}{U_T} = V_G - V_{FB} - \Gamma_b^2 \left(\sqrt{\frac{V_G - V_{FB}}{\Gamma_b^2} + \frac{1}{4}} - \frac{1}{2} \right) \tag{2.26}$$

V_G is the DC gate-to-bulk voltage and V_{FB} is the Flat-band voltage.

The velocity saturation effect is treated in [Enz and Vittoz, 2006] and [Mangla et al., 2011], considering different models to describe the velocity field dependence and defining an effective mobility μ_{eff} as a function of the horizontal electric field E_x.

The simplest one is a piecewise linear model defined by

$$v_{drift}\left(E_x\right) = \begin{cases} \mu_z \left|E_x\right| & \text{for } \left|E_x\right| < E_c \\ v_{sat} & \text{for } \left|E_x\right| \geq E_c \end{cases} \tag{2.27}$$

where E_x is the longitudinal electric field, v_{sat} is the saturated drift velocity, E_c is the critical field for which the velocity starts to saturate and μ_z is the previously defined mobility that takes into account the vertical field effect.

An effective mobility μ_{eff} is defined as

$$\mu_{eff}\left(E_x\right) \triangleq \frac{v_{drift}}{\left|E_x\right|} = \begin{cases} \mu_z & \text{for } E_x < E_c \\ \frac{v_{sat}}{\left|E_x\right|} & \text{for } E_x \geq E_c \end{cases} \tag{2.28}$$

Including the mobility bias dependence in the solution of drift-diffusion equation 2.6, assuming some simplification in the vertical field mobility reduction effect [Enz and Vittoz, 2006], the expression for i_d and the derivatives considering both mobility reduction effects are obtained [Mangla et al., 2013] :

$$i_{d_{movxz}} = \frac{4\left(q_s + q_s^2\right)}{2 + \lambda_{ck} + \sqrt{4\left(1 + \lambda_{ck}\right) + \lambda_{ck}^2\left(1 + q_s\right)^2}} \tag{2.29}$$

$$g_{ms_{movxz}} = G_{spec} \frac{\left(a - 1\right)}{\sqrt{4 + 4\lambda_{ck} + a^2\lambda_{ck}^2}} \tag{2.30}$$

$$g_{ms2_{movxz}} = \frac{G_{spec}}{U_T} \frac{g_{ms_{movxz}}}{a} \frac{4 + 4\lambda_{ck} + a\lambda_{ck}^2}{4 + 4\lambda_{ck} + a^2\lambda_{ck}^2} \tag{2.31}$$

where

$$a = 1 + q_s \tag{2.32}$$

$$\lambda_{ck} = \frac{\lambda_c}{k_2} \tag{2.33}$$

and

$$\lambda_c = \frac{L_{sat}}{L} \tag{2.34}$$

is the fraction of the channel under full velocity saturation which scales as $1/L$ and L_{sat} the velocity saturated portion of the channel. L_{sat} is a technology parameter extracted from measurements and it is ideally unique for any transistor length.

In figure 2.4 the calculated second derivative considering both effects, calculated without considering them and measured is presented as a function of the inversion coefficient 2.15. The parameter values I_s, λ_{ck} and n were obtained from measurements using the method presented in [Enz et al., 2017] for the target 130 nm CMOS process. In moderate and strong inversion the influence of mobility reduction and velocity saturation effects is evident.

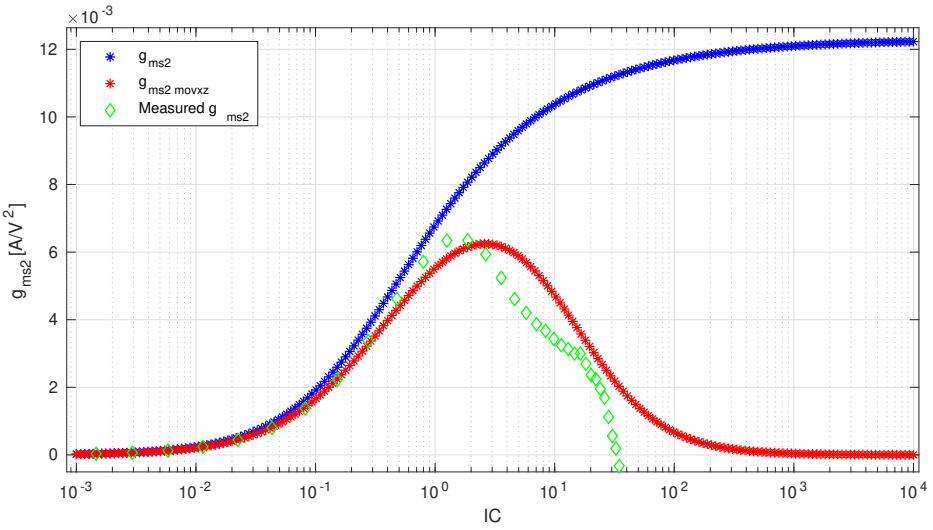

Figure 2.4: Second derivative Eq. 2.19, 2.31 and measured for W = 10 μm and L = 1 μm , considering I_{spec} = 16.44 μA, $\lambda_{ck} = 0{,}2875$, $n = 1{,}31$ and V_{DS} = 0.4 V.

2.3. Second Derivative Behavior

In the previous section, in a first approximation, the qualitative behavior of the second derivative was deduced from the EKV model highlighting the second-order effects that define it.

An analytical model that considers the analyzed (VFMR, VSAT) and other nonidealities requires adjusting a growing set of fitting parameters.

To simplify the analysis we apply a semi-empirical model approach extracting by electrical simulation a small set of Look Up Tables(LUTs) of specific low-frequency MOST characteristics [R. Fiorelli, 2011]. This approach considers the nonidealities of nanometer technologies. The data are easily obtained by extracting MOST characteristics via low-frequency simulations using a factory-provided PSP model.

To acquire these LUTs, the simple circuit of figure 2.5 is used. In it, the MOS transistor gate, drain, and source nodes are connected to a DC voltage source, while bulk nodes are connected either to the ground (nMOS transistor) or to the supply voltage (pMOS transistor). Gate voltage V_G is swept extracting I_D , g_m, g_{ds} and capacitances C_{ij}, with $ij = \{gs, gd, gb, bs, bd\}$. The same simulation must be run for a set of widths, lengths, and Drain voltage V_D values. Derivatives with respect to V_S like $g_{ms}(g_{ms2})$ could be obtained by finite difference method simulating two (three) circuits and applying a $V_S + \delta V_S$ in one of them ($V_S + \delta V_S$ and $V_S + 2\delta V_S$).

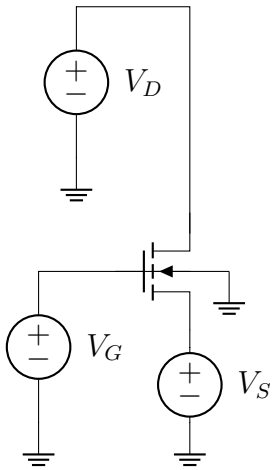

Figure 2.5: Used circuit to extract LUT's.

To better understand the dependence of the second derivative on the bias point and the dimensions of the transistor, various plots of simulated and, in some cases, measured values of the second derivatives will be presented and discussed.

The value of the simulated second derivative with respect to source voltage is presented as a function of the drain current for a fixed W/L ratio in Fig. 2.6. The impact of short channel effects becomes clear for the shortest channel (120nm) where the derivative value reduces significantly.

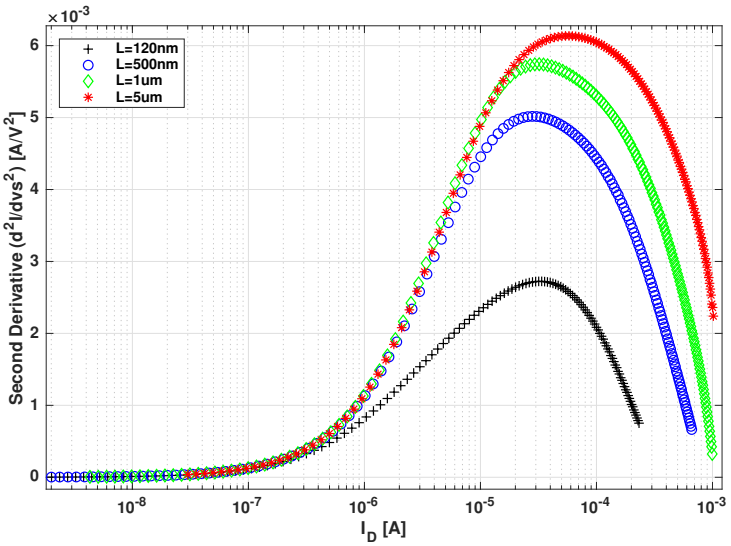

Figure 2.6: Simulated second derivative $\left(\frac{\partial^2 I_D}{\partial V_S^2}\right)$ for W/L = 10, L = (120 nm, 500 nm, 1 μm, 5 μm), V_{DS} = 0.6 V.

The value of the simulated and measured second derivative with respect to source voltage is presented in Fig 2.7 as a function of the drain current for different W/L ratios and W fixed. For low I_D values (sub μA) the second derivative in the logarithmic graph grows with current, this happens where the current is dominated by the diffusion terms and depends exponentially on the source voltage, similar to the behavior of bipolar transistor in active mode.

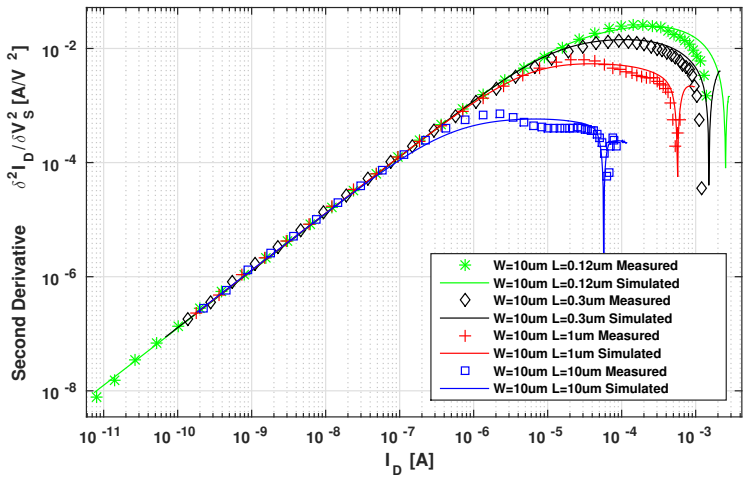

Figure 2.7: Second Derivative $\left(\frac{\partial^2 I_D}{\partial V_S^2}\right)$ as a function of I_D for W = 10 μm, L = 0.12 μm, 0.3 μm, 1 μm, 10 μm, V_{DS} = 0.4 V.

g_m over I_D ratio as indication of the inversion level

The use of adequately chosen ratios of magnitudes as key variables in analog design is a powerful technique that makes the design space more manageable and easier to visualize. This is the case of the g_m/I_D methodology [Silveira et al., 1996]. The g_m/I_D ratio varies in a small range and is related to key magnitudes for analog design and to the inversion level, thus being an excellent choice to be used as a guiding variable for the designer and giving rise to the g_m/I_D vs. $I_D/(W/L)$ curve as a universal curve. Figure 2.8 shows the g_m/I_D vs. $I_D/(W/L)$ curve for the used technology for several transistors width and length. When short channel transistors are considered, there is a slight dependency of the g_m/I_D curve on the channel length. This dependency is more pronounced for minimum length transistors, as is already noticeable in Fig. 2.8, even in a 130 nm process. Thus in those cases, the need arises to consider the g_m/I_D curve (and other characteristics) for each considered L (o a representative curve for each range of L). Similar dependence could arise for narrow transistors, close to the minimum W, but these are seldom applied in analog design.

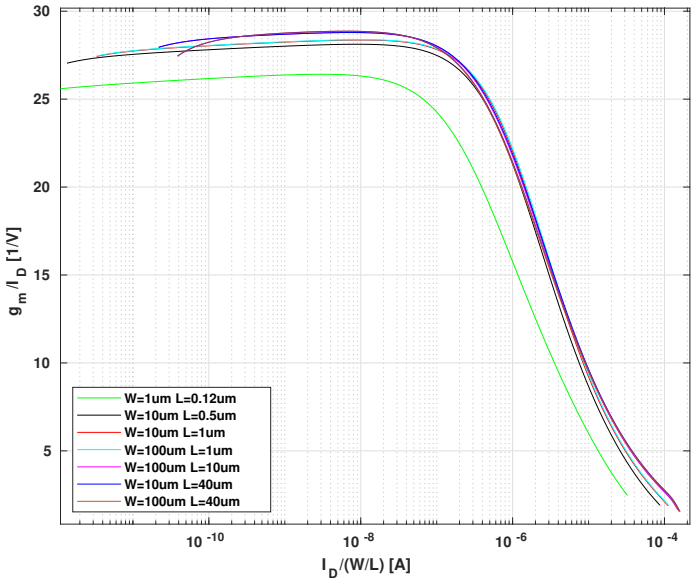

Figure 2.8: Simulated g_m/I_D as a function of $I_D/(W/L)$ for W = 1 μm L = 0.12 μm, W = 10 μm L = 0.5 μm, W = 10 μm L = 1 μm, W = 100 μm L = 1 μm, W = 100 μm L = 10 μm, W = 10 μm L = 40 μm, W = 100 μm L = 40 μm, V_{DS} = 0.4 V.

Since the behavior due to the v_s signal is considered, the g_{ms}/I_D ratio (equal to $-\frac{\partial(log(I_D))}{\partial V_S}$) is used instead of the g_m/I_D ratio (equal to $\frac{\partial(log(I_D))}{\partial V_G}$). Because of the control through v_s, as will be seen in the next sections, relevant performance aspects are directly related to the g_{ms}/I_D ratio. It is worth remembering, as can be deduced directly from equations 2.17 and 2.16, that g_m/I_D ratio is equal to the g_{ms}/I_D ratio divided by the n slope factor, which depends on the process.

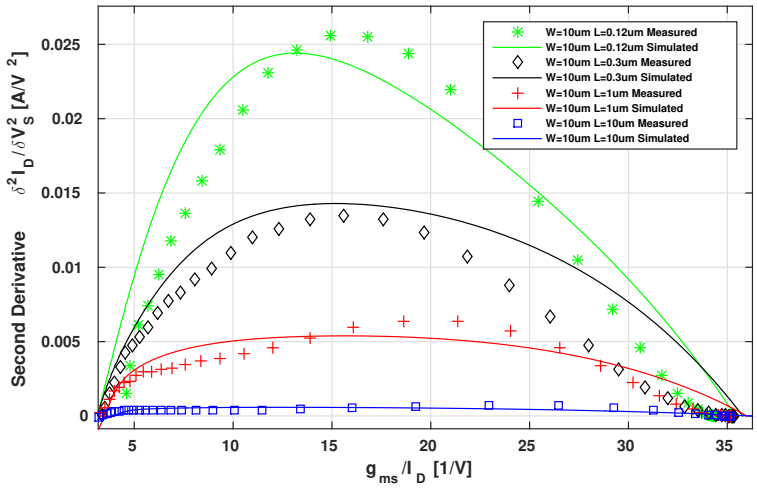

Figure 2.9: Second Derivative $\left(\frac{\partial^2 I_D}{\partial V_S^2}\right)$ as a function of g_{ms}/I_D for W = 10 μm, L = 0.12 μm, 0.3 μm, 1 μm, 10 μm, V_{DS} = 0.4 V.

Fig. 2.9 shows measured and simulated plots of the second derivative as a function of the g_{ms}/I_D ratio. The maximum is achieved in moderate inversion region ($10V^{-1} < g_{ms}/I_D < 25V^{-1}$) and increases with the W/L ratio.

2.4. Second Derivative over I_D

To reach a certain conversion gain (2.4) or scaling factor (2.5), that is certain second derivative value, from Fig. 2.9 it is not clear which size to choose. For example, given a minimum second derivative value and a current budget, we can operate in the moderate inversion region with a low W/L ratio or go toward weak inversion with a higher W/L ratio. To aid in the design decision, a figure of merit showing the efficiency in terms of the second derivative value obtained per drain current value is presented as a function of the g_{ms}/I_D ratio. This figure of merit depends only on the inversion level as shown next.

First, the expression of the second derivative of the current as a function of g_{ms}/I_D and I_D is derived.

$$\frac{\partial^2 I_D}{\partial V_S^2} = -\frac{\partial g_{ms}}{\partial V_S} = -\frac{\partial g_{ms}}{\partial I_D}\frac{\partial I_D}{\partial V_S} = \frac{\partial g_{ms}}{\partial I_D} g_{ms} \tag{2.35}$$

$$\frac{\partial g_{ms}}{\partial I_D} = \frac{\partial\left(\frac{g_{ms} I_D}{I_D}\right)}{\partial I_D} = \frac{\partial\left(\frac{g_{ms}}{I_D}\right)}{\partial I_D} I_D + \frac{g_{ms}}{I_D} \tag{2.36}$$

Using equations (2.35) and (2.36) and changing the variable of derivation from I_D to $(I_D/(W/L))$

$$\left(\frac{\partial^2 I_D}{\partial V_S^2}\right)\frac{1}{I_D} = \left(\frac{\partial\left(\frac{g_{ms}}{I_D}\right)}{\partial\frac{I_D}{W/L}}\frac{I_D}{W/L} + \frac{g_{ms}}{I_D}\right)\frac{g_{ms}}{I_D} \tag{2.37}$$

Since it has been shown that the proposed figure of merit depends only on g_{ms}/I_D and $I_D/(W/L)$, and these quantities are directly defined by the inversion level (2.12) [Silveira et al., 1996], this figure of merit only depends on the inversion level.

The simulation and measurement results for this figure of merit are presented in Fig. 2.10 where it is appreciated the dependency on inversion level and the independence of transistor sizes.

To evaluate the differences between curves for different transistor sizes, the percentage variation is calculated for simulated values taking the curve corresponding to W = 10 μ m, L = 1μm as a reference. The results are presented in figure 2.11 showing variation less than 2.5 %.

From Fig. 2.10 it is clear that the efficiency $\frac{\frac{\partial^2 I_D}{\partial V_S^2}}{I_D}$ grows with g_{ms}/I_D, the maximum achievable value is $1/U_T^2$ V^{-2} (current-voltage exponential relationship). Then for a given current budget, the second derivative value is maximized when biasing at the maximum feasible g_{ms}/I_D. This implies to increase in transistor aspect ratio which increases capacitances. This determines, as will be discussed later, a limit on the maximum g_{ms}/I_D that is convenient to choose.

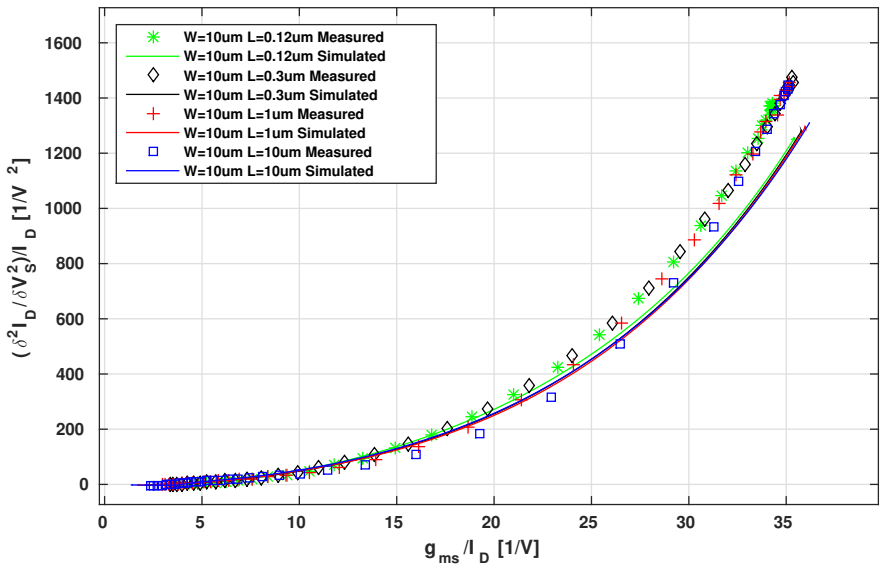

Figure 2.10: Second Derivative over I_D as a function of g_{ms}/I_D for W = 10 μ m, L = 0.12 μm, 0.3 μm, 1 μm, 10 μm, V_{DS} = 0.4 V.

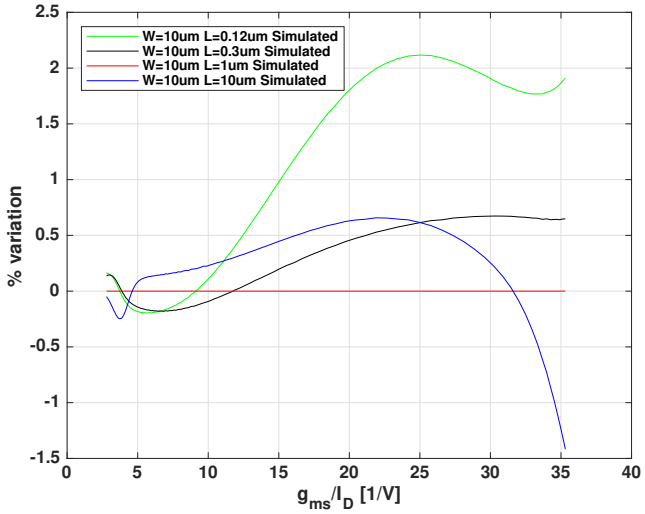

Figure 2.11: Second Derivative over I_D percentage variation as a function of g_{ms}/I_D for W = 10 μ m, L = 0.12 μm, 0.3 μm, 1 μm, 10 μm, V_{DS} = 0.4 V.

For a common gate configuration, if a high output impedance bias current source is used, R_o in (2.4) is determined by the output resistance of the transistor $1/g_{ds}$. Which in weak inversion could be considered approximately inversely proportional to I_D. In figure 2.12 the product of the second derivative by $1/g_{ds}$ is presented for different W/L ratios and W fixed.

The impact of short channel effects becomes clear for the shortest channel

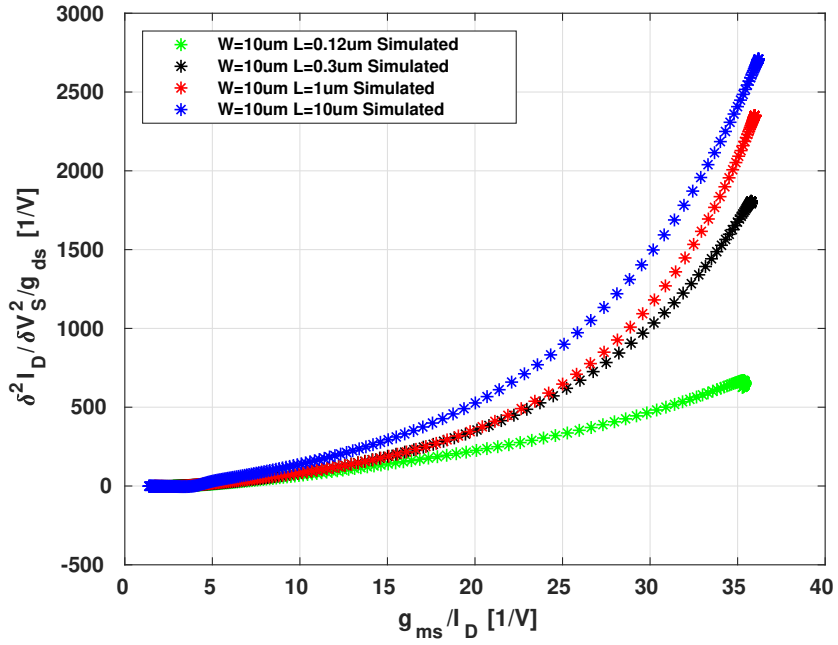

Figure 2.12: Second Derivative over g_{ds} as a function of g_{ms}/I_D for W = 10 μ m, L = 0.12 μm, 0.3 μm, 1 μm, 10 μm, V_{DS} = 0.4 V.

(120nm), mainly by the influence of the drain-induced barrier lowering effect (DIBL) increasing g_{ds} value i.e. decreasing R_o [Tsividis, 2011], [Binkley, 2008]. This suggests the convenience of using a nonminimum transistor for the detector.

2.5. Noise

In previous sections aspects related to the gain of the ED were analyzed. The other characteristic that should be taken into account in the design is the noise, which in conjunction with the gain will define the Signal to Noise Ratio of the circuit.

2.5.1. Noise in MOS transistors

This section presents the MOS transistor noise. The MOS transistor presents several sources of noise of different types or origins that determine a characteristic output current power spectral density (PSD) as the one shown in Fig.2.13.

In this figure three regions are recognized: the flicker noise zone, the thermal or white noise zone, and the induced-gate noise zone. The first two are modeled as an output current source and the last one as an input current source as shown in figure 2.14.

Thermal noise is due to the random thermal motion of electrons and holes, the PSD for the channel noise current due to the white or thermal noise is [Enz and

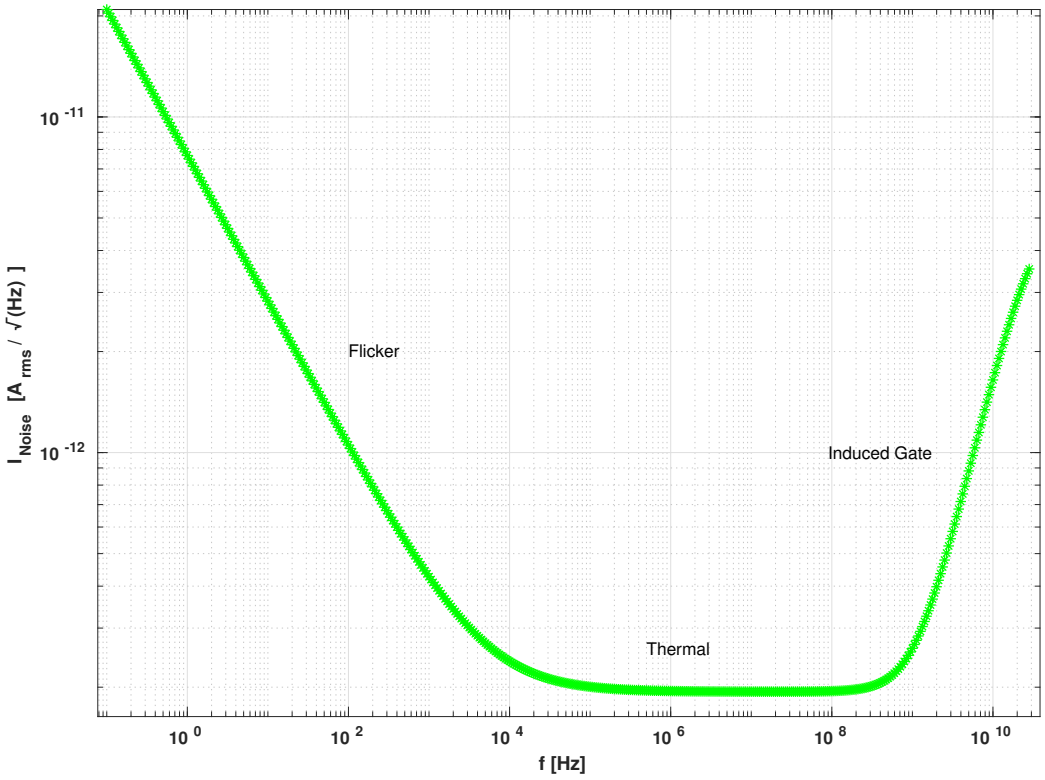

Figure 2.13: Simulated noise output current PSD as a function of frequency for a transistor with W = 10 μ m, L = 1 μm, V_{GB} = 0.1 V, V_{DB} = 0.4 V and V_{SB} = 0 V.

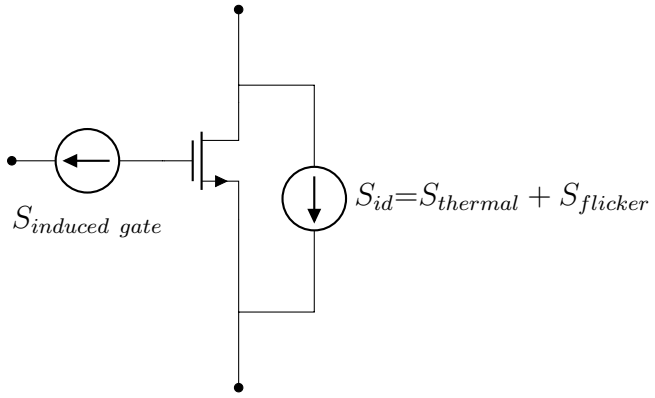

Figure 2.14: MOS noise equivalent circuit model.

Vittoz, 2006]:

$$\overline{i_{dth}^2} = S_{thermal} = 4\delta_{nD} k_B T g_{ms} \tag{2.38}$$

where k_B is the Boltzmann constant, T is the absolute temperature and δ_{nD} is a thermal noise parameter

$$\delta_{nD} = \frac{2}{3}\frac{q_s + 3/4}{q_s + 1} = \begin{cases} \frac{1}{2} \text{ WI and saturation } (q_s \ll 1) \\ \frac{2}{3} \text{ SI and saturation } (q_s \gg 1) \end{cases} \tag{2.39}$$

In addition to the thermal noise, the MOS transistor also exhibits flicker or $1/f$ noise. It is quite well accepted that the sources of flicker noise are mainly carrier number and mobility fluctuations due to random trapping–detrapping of carriers in energy states near the surface of the semiconductor. It is characterized by a PSD 2.40 that is inversely proportional to frequency [C. Galup-Montoro and Cunha, 1999], it therefore dominates at low frequency.

$$\overline{i_{dfl}^2} = S_{flicker} = \frac{K_F g_m^2}{C_{ox} W L f} \tag{2.40}$$

In 2.40 K_F is the flicker noise constant and f is the frequency.

To compare it to the thermal noise the corner frequency f_c [Arnaud and Galup-Montoro, 2004] is defined as the frequency at which the flicker-noise and thermal-noise PSDs have the same value. In saturation

$$f_c = \frac{\alpha g_m}{W L C_{ox}} \frac{N_{ot}}{N^*} \cong \frac{\pi}{2} \frac{N_{ot}}{N^*} f_T \tag{2.41}$$

with

$$\alpha = \begin{cases} \frac{1}{2} \text{ WI and saturation } (q_s \ll 1) \\ \frac{9}{16} \text{ SI and saturation } (q_s \gg 1) \end{cases} \tag{2.42}$$

The parameter N_{ot} is the equivalent density of oxide traps defined [Nemirovsky et al., 2001] by

$$N_{ot} = \frac{k_B T N_t}{\gamma} \tag{2.43}$$

where N_t is the density of oxide traps per unit volume and unit energy and γ is the attenuation coefficient of the electron wave function in the oxide. N^* is defined as $N^* = nC_{ox}U_T/q$ and f_T is the intrinsic transition frequency

$$f_T = \frac{g_m}{2\pi\left(C_{gs} + C_{gb} + C_{gd}\right)} \tag{2.44}$$

The approximation in 2.41 was based on the fact that α is almost insensitive to the inversion level and the total capacitance sum can be approximated without significant loss of accuracy by $C_{gs} + C_{gb} \simeq WLC_{ox}/2$.

In Fig.2.15 the corner frequency obtained by noise simulation for two n-channel transistors of different lengths (L= 0.12 μm , 1 μm) and the same width W is shown as a function of the inversion level represented by the gm/ID ratio. As f_T [Enz and Cheng, 2000] the corner frequency drops with the inversion level.

For very high frequencies another type of noise known as induced gate noise could be significant. The origin of the induced gate noise of a MOS transistor is

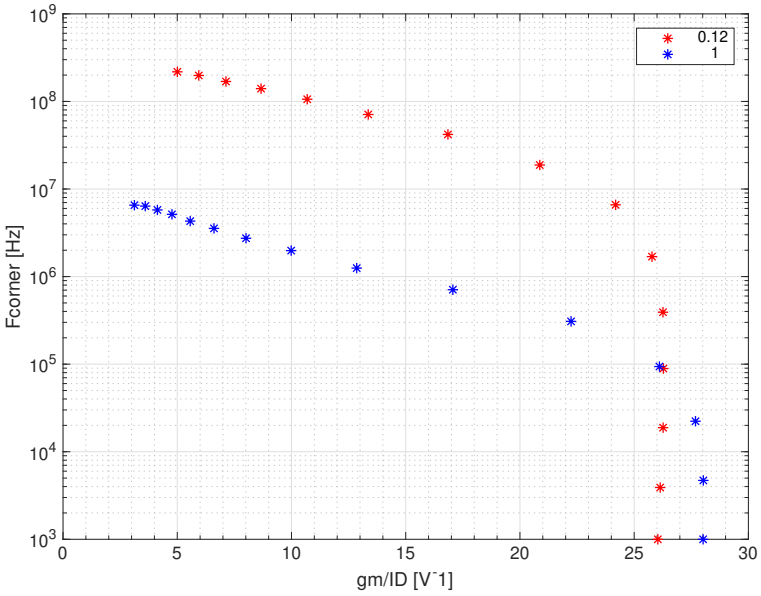

Figure 2.15: Simulated corner frequency vs g_m/I_D for a transistor with W = 10 μm, L = 0.12μm, 1 μm, V_{DB} = 0.4 V and V_{SB} = 0 V.

the thermal noise of the conducting channel which is capacitively coupled to the gate [C. Galup-Montoro and Cunha, 1999], [Enz and Vittoz, 2006]. The simplified expression of the PSD in saturation for weak and strong inversion is:

$$\overline{i_{ig}^2} = S_{induced\ gate} = \begin{cases} \dfrac{w^2\left(C_{gs}+C_{gd}\right)^2}{6\left(g_{ms}+g_{md}\right)} \text{ WI and saturation} \\ \\ \dfrac{4w^2C_{gs}^2}{15g_{ms}} \text{ SI and saturation} \end{cases} \tag{2.45}$$

Since both of the noise sources, thermal and induced gate, are due to the same physical cause they are usually correlated. The correlation coefficient c between gate and drain noise is defined as

$$c = \frac{\overline{i_{ig}i_{dth}^*}}{\sqrt{\overline{i_{ig}^2}}\sqrt{\overline{i_{dth}^2}}} \tag{2.46}$$

As shown in [C. Galup-Montoro and Cunha, 1999] in saturation $|c| \rightarrow 0{,}4$ in SI and $|c| \rightarrow 0{,}6$ in WI.

2.5.2. Noise in RF Envelope Detector

As described in [Huang et al., 2013], [Nilsson and Svensson, 2011] and [Simone Gambini and Rabaey, 2008] three different output noise current components

are identified in an envelope detector like the one shown in Fig. 2.1. Noise at radio frequencies coming from the transistor, like the induced gate noise, or external that is converted to baseband when mixed by the nonlinear detector with, either, the signal of interest or an interferer. Baseband noise being transferred without any frequency conversion (e.g. from bias circuits) and baseband noise from the channel of the detector transistor.

RF noise converted to baseband

Radio frequency noise is converted to baseband by two mechanisms, the mixing between the signal carrier or interferer ($v_{in}cos\,(2\pi f_c t)$) and noise, and the self-mixing of noise as shown in figure 2.16.

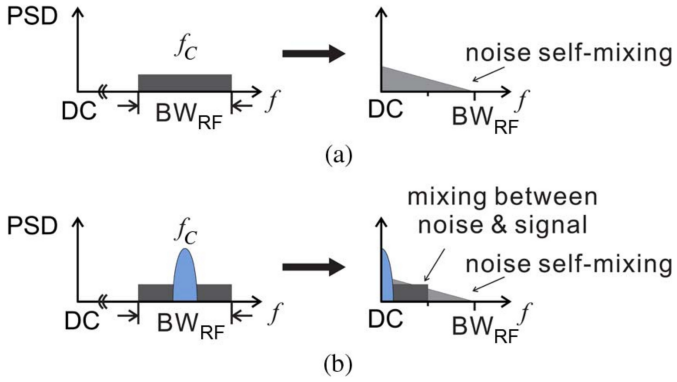

Figure 2.16: Noise spectral distribution during envelope detection. (a) Noise self-mixing. (b) Mixing between noise and signal. Taken from [Huang et al., 2013]

As shown in [Huang et al., 2013] for a square detector, where the input (x) and output (y) are related according to 2.47 [1]

$$y = k^* x^2 \tag{2.47}$$

Considering an input signal $S_{ED,IN}$ with input power $S^2_{ED,IN}$ plus RF input noise $N_{ED,IN}$ with zero mean and variance $\sigma^2_{ED,IN}$ the output voltage is

$$\begin{aligned} y &= k^* \left(S_{ED,IN} + N_{ED,IN}\right)^2 \\ &= k^* \left(S^2_{ED,IN} + 2S_{ED,IN}N_{ED,IN} + N^2_{ED,IN}\right) \end{aligned} \tag{2.48}$$

and the variance of the output noise is [2]

[1] k^* is the scaling factor for a general input signal and general square detector. The k defined in 2.5 applies to the particular case of an amplitude-modulated input signal.

[2] Calculated by making use of the first, second, third, and fourth central moments of Gaussian distribution [Huang et al., 2013]

$$\begin{aligned}\sigma_y &= E\left(y^2\right) - \left(E\left(y\right)\right)^2 \\ &= 4k^{*2}S_{ED,IN}^2\sigma_{ED,IN}^2 + 2k^{*2}\sigma_{ED,IN}^4\end{aligned} \tag{2.49}$$

In this expression two terms are recognized, the first one due to signal-noise intermodulation and the second due to self-mixing noise. Since one-half of the signal and noise power reside at $2f_c$ and the other half at baseband the baseband noise power is half of 2.49. For the self-mixed noise, considering a white noise spectrum, the convolution of bandpass-filtered results in triangular-shaped output PSD between *dc* and the radio-frequency bandwidth BW_{RF}. For the noise results of signal-noise mixing, the baseband noise is white between *dc* and $BW_{RF}/2$.

Then the noise PSD at the ED output can be written as

$$PSD_{ED,OUT} = \frac{2k^{*2}S_{ED,IN}^2\sigma_{ED,IN}^2}{BW_{RF}/2} + \frac{k^{*2}\sigma_{ED,IN}^4 2\left(BW_{RF} - f\right)}{BW_{RF}BW_{RF}} \tag{2.50}$$

where f is the baseband frequency in the range of $[0, BW_{RF}]$. Usually, the baseband bandwidth (BW_{BB}) is much smaller than BW_{RF} so the total noise power considering this band could be approximated by

$$\begin{aligned}\sigma_{OUT}^2 &= \int_0^{BW_{BB}} PSD_{ED,OUT}\, df \\ &\approx \left(4k^{*2}S_{ED,IN}^2\sigma_{ED,IN}^2 + 2k^{*2}\sigma_{ED,IN}^4\right)\frac{BW_{BB}}{BW_{RF}}\end{aligned} \tag{2.51}$$

For the common gate circuit case 2.2 b the RF input noise $N_{ED,IN}$ is mainly the external RF noise at the input v_{RF}, the induced gate voltage noise is negligible because the gate is shorted to ground especially at high frequencies. Usually in 2.51 the first term is dominant because the signal or blocker power is bigger than the noise power. Anyway, usually, the influence of the RF input noise converted to baseband is negligible compared to the intrinsic baseband noise. In [Nilsson and Svensson, 2011] the authors compare the influence of the signal\blocker-noise intermodulation term of 2.49 with the baseband thermal transistor noise for the particular case of WI (current-voltage exponential relationship), concluding that even for very large blockers (or signals), we can allow quite large input RF noise without affecting the total noise current.

Baseband noise

Baseband noise comes from the envelope detector transistor and complementary circuits like bias. Some of them, for example the noise present in the gate bias voltage, can be reduced by shorting to ground at baseband frequencies. The baseband noise from the envelope detector transistor consists of $1/f$ and thermal noise. The total noise current power at the output is obtained by integrating the noise PSD from the lowest f_{MIN} to the highest f_{MAX} frequency of interest.

These frequencies will be determined by the baseband frontend frequency response (BW_{BB}). If the signal of interest includes dc then f_{MIN} is not 0, it will be determined by the observation duration.

$$\begin{aligned}\sigma^2_{i\,ED\,transistor\,OUT} &= \int_{f_{MIN}}^{f_{MAX}} (S_{thermal} + S_{flicker})\; df \\ &= S_{thermal}.\left((f_{MAX} - f_{MIN}) + f_c.\ln\left(\frac{f_{MAX}}{f_{MIN}}\right)\right)\end{aligned} \tag{2.52}$$

To minimize the baseband noise, the minimum BW_{BB} to accomplish signal requirements should be considered, this is the case in the WuRX scenario where the data rate and therefore the bandwidth required is small. Also, if possible, the influence of the flicker noise could be attenuated selecting a transistor size and bias to reduce f_c and a baseband modulation scheme with no dc component allowing to select f_{MIN} high enough to keep the $\ln\left(\frac{f_{MAX}}{f_{MIN}}\right)$ factor low. Fulfilling the above, only thermal noise is relevant.

2.5.3. Signal to Noise Ratio

In what follows, we analyze what happens with the signal-to-noise ratio in all inversion regions considering that the transistor channel thermal noise is the dominant contributor.

Considering the rms value of (2.3) and (2.38) the output signal-to-noise ratio can be expressed as

$$SNR = \frac{i^2_{outbb_{rms}}}{i^2_n} = \left(\frac{\partial^2 I_D}{\partial V_S^2}\right)^2 \frac{v^4_{in}\, m^2}{32\,\delta_{nD}\,k_B\,T\,g_{ms}\,BW_{BB}} \tag{2.53}$$

where BW_{BB} is the noise integration bandwidth.

The result of evaluating equation 2.53 for all inversion levels and considering an input amplitude $v_{in} = 1{,}6\,mV_{rms}$ and a noise bandwidth $B = 15{,}7\,kHz$ [1] is shown in figure 2.17. The higher values of SNR are obtained for the moderate inversion region and for the higher values of W/L.

The estimation results of equation 2.53 are compared with simulation results of the SNR for an example case (L = 1 μm, W = 10 μm). The simulated SNR is evaluated using a Quasi-Periodic Steady State analysis (QPSS) and a Noise analysis for sub μA bias currents in a baseband spectrum from 10 kHz to 100 kHz ($BB_{BW} = 90\,kHz$). The results are presented in figure 2.18.

The SNR values estimated and obtained by simulation show a good agreement with a difference smaller than 1 dB when only the thermal noise is considered. Considering the total noise, thermal, and flicker, the difference is notorious for higher currents where the corner frequency (Fig 2.15) surpasses the baseband lower frequency f_{MIN} and the flicker noise contribution to the total noise dominates as seen in table 2.1.

[1] These values correspond to design data presented in section 3.2

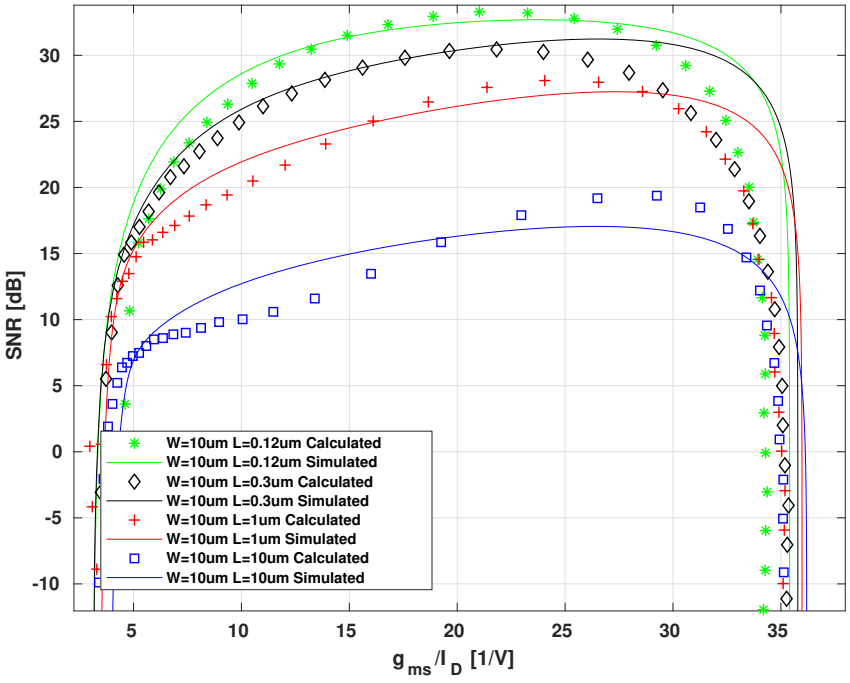

Figure 2.17: SNR for simulated and calculated from measured values of $\frac{\partial^2 I_D}{\partial V_s^2}$ and g_{ms} as a function of g_{ms}/I_D for W = 10 μm, L = 0.12 μm, 0.3 μm, 1 μm, 10 μm, BW_{BB} = 15.7 kHz, δ_{nD} = 0.5, m = 0.5, v_{in} = 1.6 mV$_{rms}$ (P_{in} = -43 dBm), V$_{DS}$ = 0.4 V.

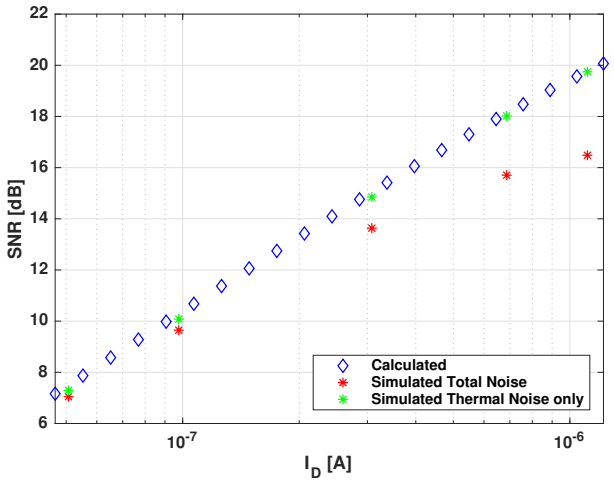

Figure 2.18: SNR results from QPSS and noise simulation, considering the total noise and only thermal noise, and calculated using equation 2.53 (L = 1 μm, W = 10 μm, v_{inrms} = 2 mV$_{rms}$, BW_{BB} = 90 kHz, V$_{DS}$ = 0.4 V, δ_{nD} = 0.5, $T = 300\,K$).

$I_D\,[A]$	$\frac{g_m}{I_D}\,[V^{-1}]$	$\sigma^2_{Total}\,[A^2_{rms}]$	$\sigma^2_{thermal}\,\%$	$\sigma^2_{flicker}\,\%$
$51e^{-9}$	29.4	$1.26e^{-21}$	95.0	5.0
$98e^{-9}$	29.3	$2.53e^{-21}$	90.5	9.5
$308e^{-9}$	29.1	$9.46e^{-21}$	75.5	24.5
$687e^{-9}$	28.7	$2.71e^{-20}$	58.5	41.5
$1.11e^{-6}$	28.2	$5.34e^{-20}$	47.4	52.6

Table 2.1: Simulation noise power values for different bias currents (L = 1 μm, W = 10 μm, V_{DS} = 0.4 V, BB_{BW} = 90 kHz).

As mentioned in section 2.5.2, flicker noise influence could be attenuated by selecting a transistor size and bias to reduce f_c and a baseband modulation scheme with no *dc* component and f_{MIN} high enough.

2.6. SNR over I_D

In the same way, as we considered a figure of merit showing the efficiency in terms of the second derivative value obtained per drain current value, we present the SNR obtained per drain current value. This figure of merit also depends only on the inversion level, as shown here:

$$\frac{SNR}{I_D} = \left(\frac{\partial^2 I_D}{\partial V_S^2}\right)^2 \frac{v_{in}^4\, m^2}{I_D\, 32\, \delta_{nD}\, k_B\, T\, g_{ms}\, BW_{BB}} \tag{2.54}$$

multiplying and dividing (2.54) by I_D and rearranging

$$\frac{SNR}{I_D} = \left(\frac{\partial^2 I_D}{I_D\, \partial V_S^2}\right)^2 \frac{I_D}{g_{ms}} \frac{v_{in}^4\, m^2}{32\, \delta_{nD}\, k_B\, T\, BW_{BB}} \tag{2.55}$$

the first factor is the previous figure of merit squared and the second factor is inversely proportional to g_{ms}/I_D, so again this new figure of merit only depends on the inversion level.

To express the SNR in dB and the input power P_{in} in dBm, we take logarithm on both sides of (2.55),

$$\begin{aligned} &SNR\,|_{dB} - 10.log_{10}\left(\frac{I_D}{1\,A}\right) = \\ &10.log_{10}\left(\left(\frac{\partial^2 I_D}{I_D.\partial V_S^2}\right)^2 \left(\frac{I_D}{g_{ms}}\right)\left(\frac{(0.225V)^4}{8\,\delta_{nD}\, k_B\, T\, 1\,Hz\, 1\,A}\right)\right) \\ &- 10.log_{10}\left(\frac{BW_{BB}}{1\,Hz\,m^2}\right) + 2\,P_{in}\,|_{dBm} \end{aligned} \tag{2.56}$$

In Fig. 2.19 the results of evaluating $10log_{10}(\frac{SNR}{I_D})$ is presented for simulated and measured values of $\frac{\partial^2 I_D}{\partial V_S^2}$ and g_{ms} for different transistor sizes. Again is clear

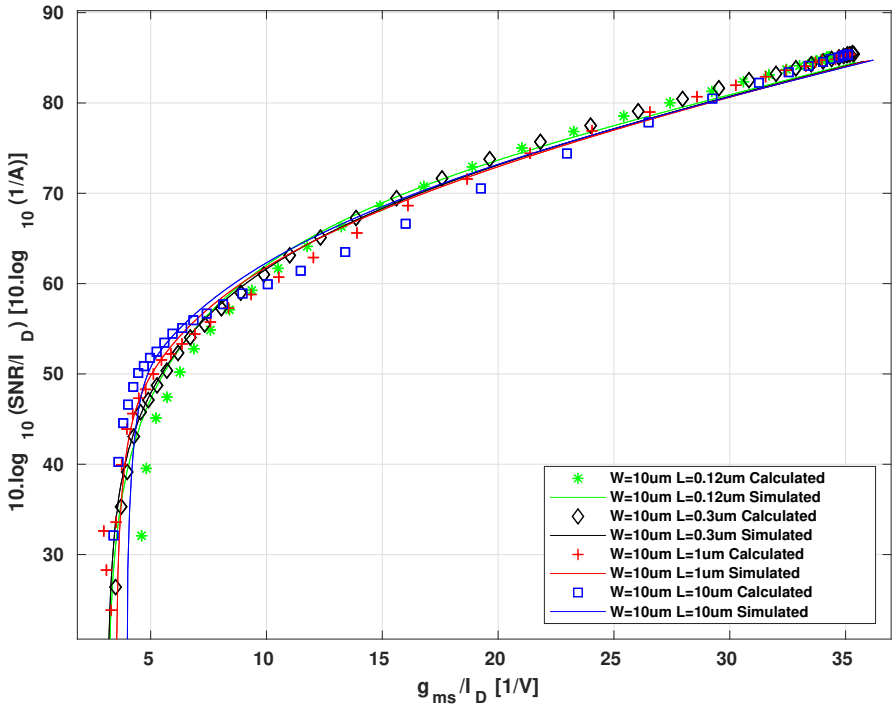

Figure 2.19: SNR/I_D for simulated and calculated from measured values of $\frac{\partial^2 I_D}{\partial V_S^2}$ and g_{ms} as a function of g_{ms}/I_D for W = 10μm, L = 0.12μm, 0.3μm, 1μm, 10μm, BW_{BB} = 15.7 kHz, δ_{nD} = 0.5, m = 0.5, v_{in} = 1.6 mV$_{rms}$ (P_{in} = -43 dBm), V_{DS} = 0.4 V.

that the efficiency $\frac{SNR}{I_D}$ grows with g_{ms}/I_D. Then for a given current budget, the signal-to-noise ratio value is maximized with maximum g_{ms}/I_D.

Equation (2.56) relates the usual specifications of the circuit, signal-to-noise ratio (SNR), current budget (I_D), bandwidth (B), input power (P_{in}) and a term that is determined by the technology and bias point chosen and can be obtained as a function of g_{ms}/I_D. A change in specifications just translates the curve of Fig.2.19 up or down.

2.7. Conclusions

In this chapter first, the physical basis and modeling of the behavior of the second derivative of the current with respect to source or gate voltage were presented. Then two figures of merit to guide the optimization of the performance-consumption trade-offs of a MOS envelope detector for WuRX were presented. These figures of merit are related to the inversion level of the transistor. It is demonstrated that operation with maximum g_{ms}/I_D improves the conversion gain and SNR for a given current budget.

Chapter 3

Ultra low power wake-up receiver front end

The goal of this chapter is to evaluate and use the results presented in chapter 2. Initially Section 3.1 presents the design process, simulation, and measurement results of a fully integrated common gate Envelope Detector with an input matching network. In Section 3.2 the design of a novel enhanced envelope detector is analyzed and the corresponding simulation and measurement results are presented.

The main contributions presented in this chapter are published in [Reyes and Silveira, 2019].

3.1. Common Gate Envelope Detector with Matching Network

To evaluate the results presented in chapter 2 a radio frequency Envelope Detector as shown in figure 3.1 is designed. The implementation of this circuit in a 130 nm CMOS technology at 2,4GHz imposes several constraints in transistor size and bias.

Detector input signal and consequently sensitivity is maximized for minimized loss in RF signal path and power matching. In a fully integrated approach where very high-quality inductors are not available the simpler the network the better, that is the case of the implemented network. This simple scheme has the drawback that there is no tuning available to adjust central frequency deviation due to parasitic variation or component tolerance. Given that to evaluate the circuit a controlled frequency obtained from a waveform generator is used, the characterization could be done without problems. In a field wake-up receiver scenario, the use of a tuning circuit could be advisable or even mandatory.

The matching network (C_m, L_m), which results in the maximum power transfer, provides a voltage gain that quadratically increases the signal output current according to (2.3). The gain contribution of the passive input matching network could be estimated considering the simplified circuit shown in figure 3.2, adding the

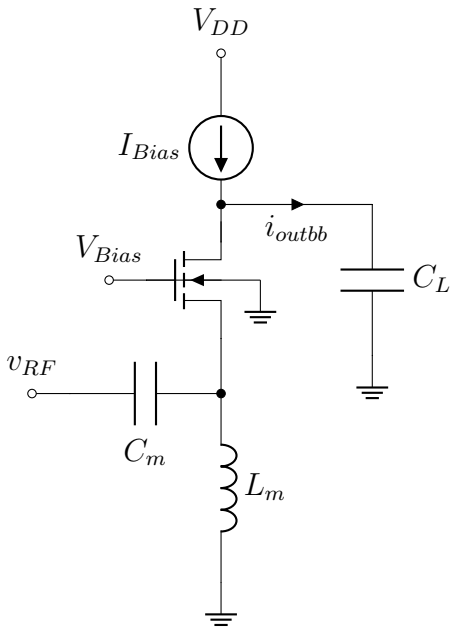

Figure 3.1: Common gate envelope detector schematic.

inductor parallel parasitic resistance and capacitance (R_p, C_p) and the transistor input impedance at source $(1/g_{ms}, C_s)$.

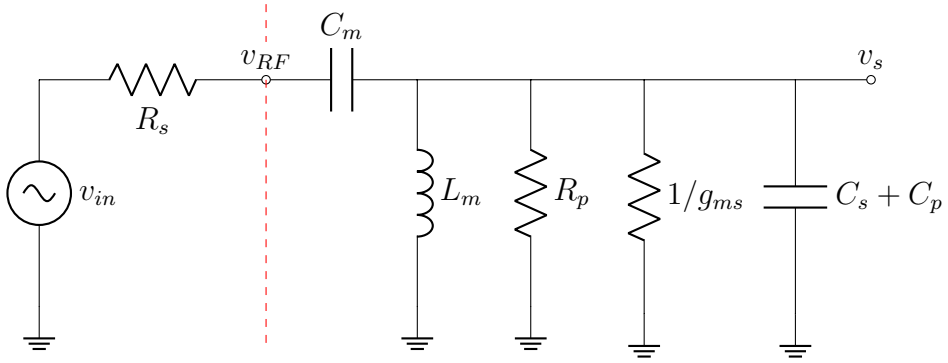

Figure 3.2: Simplified equivalent small signal circuit of Fig. 3.1

Assuming the matching circuit to be lossless and transforming the impedance seen from the source terminal to the source resistance R_s ($v_{RF} = \frac{v_{in}}{2}$), the power dissipated in R_s and $R_p//1/g_{ms}$ should be equal

$$\frac{v_S^2}{R_p // (1/g_{ms})} = \frac{v_{RF}^2}{R_s} \tag{3.1}$$

where v_S is the voltage at the source node of the transistor and v_{RF} is the input voltage. From Eq.3.1 the voltage gain of the matching circuit can be expressed as

$$G_{MN} = \sqrt{\frac{R_p // (1/g_{ms})}{R_s}} \tag{3.2}$$

The increase of the parallel $R_p // (1/g_{ms})$ increases the gain value. For the inductor, higher values of inductances come with higher values of R_p and C_p, the limit will be imposed by area and self-resonance frequency.

For the used technology and work frequency(2.4 GHz) a maximum reasonable value fulfilling the area and self-resonance frequency requirements is 8 nH. For the mentioned inductor $R_p \approx 1.55\,k\Omega$ and $C_p \approx 0{,}06\,pF$.

If the input impedance of the transistor is high enough the maximum gain obtained by the selected inductor will be achieved.

For the real part term $(1/g_{ms})$, assuming a drain current I_D lower than 1 $\mu A -$ 100 nA and working in weak inversion as the previous chapter results suggest, the g_{ms} is maximum and can be approximated by (I_D/V_T). Then this real part will be greater than 26 $k\Omega - 260\ k\Omega$, not influencing the result of the parallel with R_p.

The imaginary part of the transistor input impedance is the total capacitance seen from the source, which is proportional to the transistor size, and at work frequency is the term that dominates in the transistor input impedance.

This imposes a restriction on the maximum transistor ($M1$) size that could be considered and hence the lower inversion level at which is possible to operate achieving the desired specifications for the required current.

We apply the following criterion: the impedance at 2.4 GHz of the input capacitance of the transistor shall be 20 times higher than the impedance of the inductor.

For the previously considered inductance (8 nH) the limit for the maximum input capacitance of the transistor is about 0.03 pF.

The total source capacitance $C_s = c_{sg} + c_{sb} + c_{sd}$ for different transistor sizes and inversion levels is presented in figure 3.3.

To fulfill the requirements, transistor sizes of the order of $10\mu m^2 - 20\mu m^2$ should not be surpassed, even for weak inversion region. In addition, a safety margin must be considered because these capacitances are added to the interconnection capacitances that can be evaluated after the extraction of the final design.

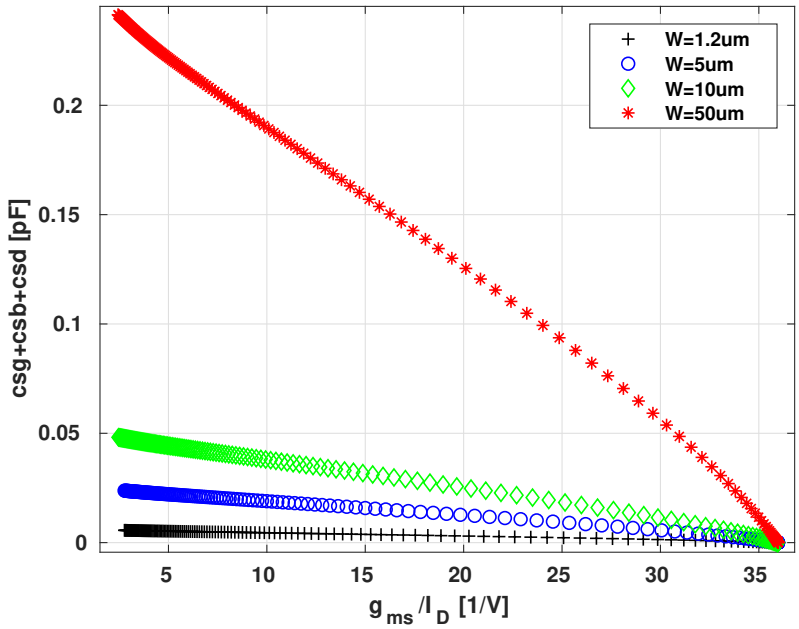

Figure 3.3: Capacitance $c_{sg} + c_{sb} + c_{sd}$ for L = 1μm, W = (1.2 μm, 5 μm, 10 μm, 50 μm).

To complete the design of the matching network circuit of figure 3.2 the pad capacitances (C_{pad}), the bondwire inductor (L_{bw}) and the package capacitance (C_{pack}) should be added as in figure 3.4. Maintaining the lossless hypothesis of added elements, the voltage gain of the matching network keeps the same value of 3.2

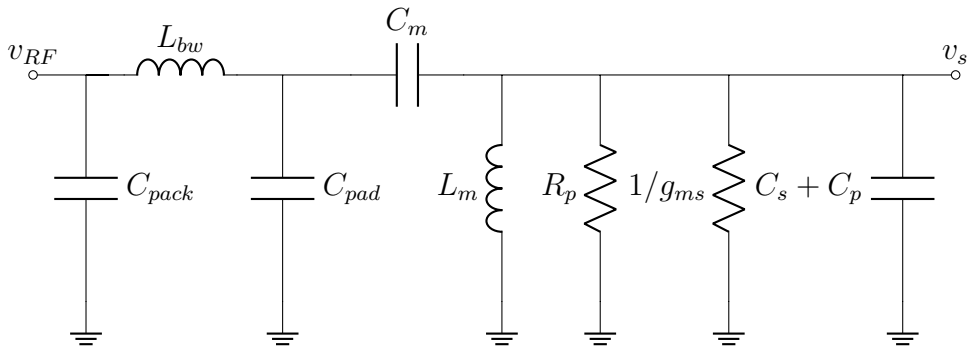

Figure 3.4: Equivalent input circuit considering pad, bondwire, and package.

Many of the components in 3.4 are parasitic and can be estimated by extraction or de-embedding. The estimated values and the sensitivity of the matching network gain G_{MN}, were calculated and presented in table 3.1.

From there, it is clear that the central frequency is mainly determined by

Component	Value	G_{MN} peak value	G_{MN} f_c	G_{MN} Q
L_m	8.27 nHy	0.06	-0.46	-0.28
C_m	0.5 pF	-0.08	-0.39	-0.40
R_p	1.55 $k\Omega$	0.27	0	0.36
$C_s + C_p$	0.06 pF	0.01	-0.06	0.32
C_{pad}	0.8 pF	0.01	0.01	-0.07
L_{bw}	1.2 nHy	-0.06	-0.05	-0.18
C_{pack}	2.6 pF	0.08	-0.05	0.74

Table 3.1: Components values and sensitivity for G_{MN} peak value, G_{MN} central frequency f_c, G_{MN} quality factor Q respect each component variations.

the original matching network values C_m, L_m, and that the parasitic component $(C_s + C_p, L_{bw}, C_{pack}, C_{pad})$ have an important influence in the selectivity Q of the network particularly the package capacity C_{pack}.

The simulated matching network gain for the table 3.1 values is presented in figure 3.5.

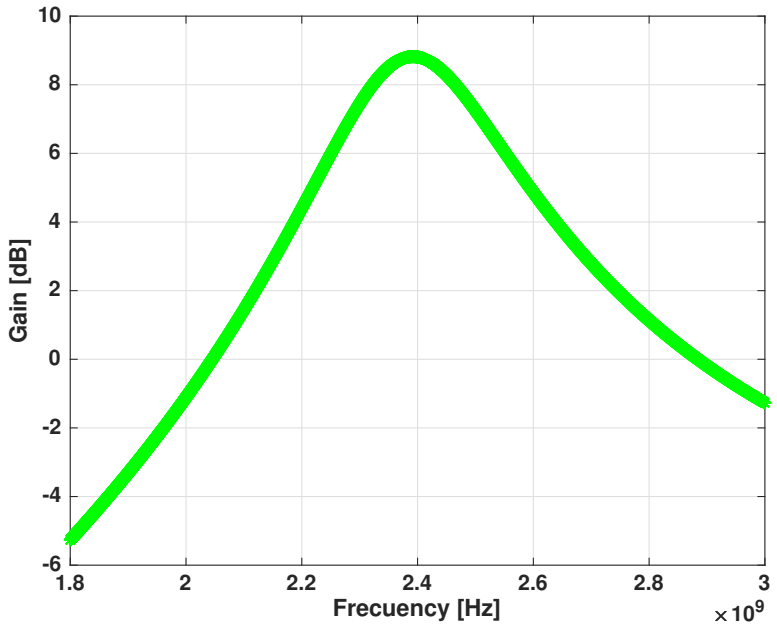

Figure 3.5: Simulated matching network Gain for the values presented in table 3.1.

In figure 3.6 the Measured S11 of the fabricated ED is presented.

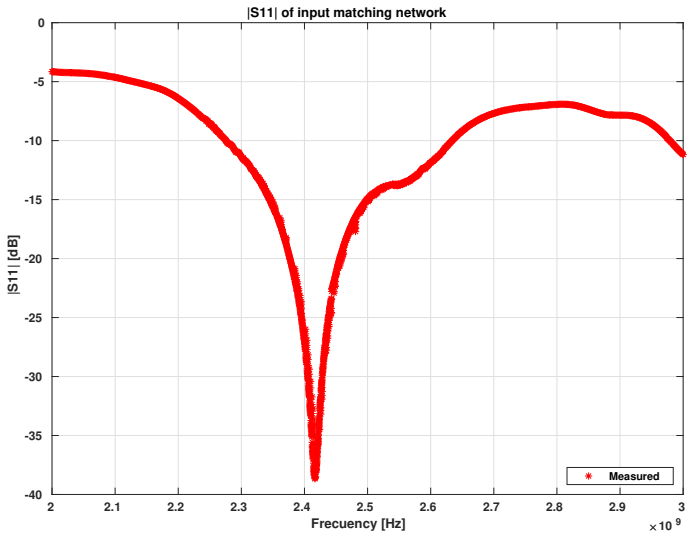

Figure 3.6: Measured S11 for the fabricated Envelope Detector of figure 3.1.

As mentioned in section 2.4, for a given current budget the second derivative and so the current conversion gain is maximized when biasing at the maximum feasible g_{ms}/I_D. This means, as can be seen in figure 3.7 that the $I_D/(W/L)$ ratio should be lower than $10^{-7}A$.

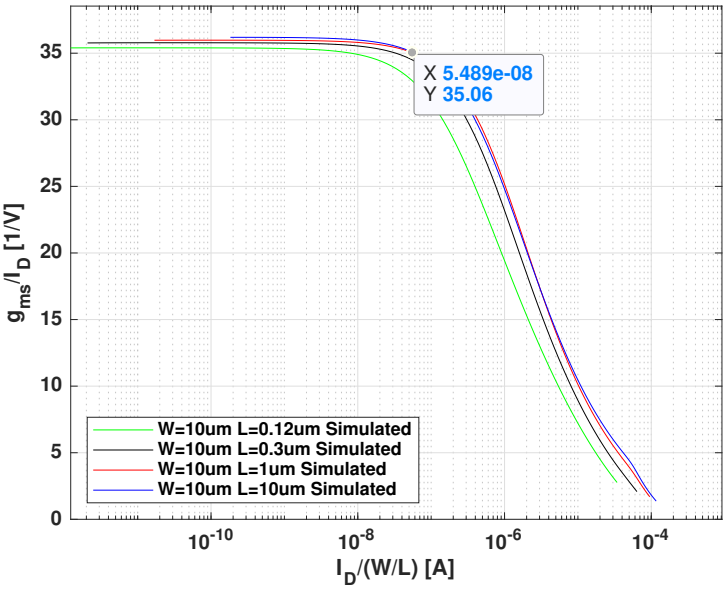

Figure 3.7: g_{ms}/I_D as a function of $I_D/(W/L)$ for $W = 10\mu$m $L = 0.12\,\mu$m, $0.3\,\mu$m, $1\,\mu$m, $10\,\mu$m, $V_{DS} = 0.4$ V.

Considering the previous paragraph criteria, the area restriction imposed by the transistor capacitance previously analyzed and staying away from minimum length transistor to avoid short channel effect, a transistor of $W = 16\mu$m and $L = 1\mu$m and a bias current of 50 nA were selected ($I_D/(W/L) = 3.125$e-9 A).

Neglecting I_{BIAS} source output impedance, an estimation of the voltage scaling factor Eq. 2.5 could be obtained.

Eq. 2.5 from section 2.1 is repeated for convenience including the matching network gain G_{MN} and substituting R_o with $1/g_{ds}$

$$k = \frac{v_{outbb}}{v_{in}^2} = \left(\frac{\partial^2 I_D}{\partial V_S^2}\right)\frac{mR_oG_{MN}^2}{2} = \frac{\partial^2 I_D}{\partial V_S^2}\frac{1}{g_{ds}}\frac{mG_{MN}^2}{2} \tag{3.3}$$

For the previously selected design values, using figures 3.7 and 2.12 the product of the second derivative and the output impedance of the transistor is obtained $(\frac{\partial^2 I_D}{\partial V_S^2}\frac{1}{g_{ds}})$

$$\begin{aligned} &\frac{I_D}{(W/L)}\left(3.125e^{-9}A\ \right)\xrightarrow{Fig3.7}\ \frac{g_{ms}}{I_D}\left(35.8V^{-1}\right) \\ &\xrightarrow{Fig2.12}\ \frac{\partial^2 I_D}{\partial V_S^2}\frac{1}{g_{ds}}\left(2300V^{-1}@L = 1\mu m\right) \end{aligned} \tag{3.4}$$

Evaluating 3.3 for $G_{MN} = 2.81V/V$ (maximum matching network gain obtained from simulation values Fig. 3.5) and $m = 0{,}5$ the scaling factor is $k = 4.54e^3\ V^{-1}$.

A corner simulation was conducted to evaluate the influence of the transistor process variation on the used figure of merit, the results are presented in appendix A. The circuit of figure 3.1 was fabricated and measured. The used measurement setups are presented in appendix B.

In figure 3.8 the baseband output power as a function of the carrier frequency, for an input power $P_{in} =$ -47 dBm and a modulation frequency of 120 Hz is shown.

Using the previous calculated scaling factor and considering $P_{in} =$ -47 dBm ($v_{in} = 1.41mV$) the estimated baseband output voltage is

$$v_{outbb} = k.v_{in}^2 = 9\,mV \tag{3.5}$$

then the baseband output power over a 50 Ω impedance considering a unity gain measurement setup is

$$P_{BB} = 20log_{10}(9\,mV/(\sqrt{2}\,0.225\,V)) = -30.9\,dBm, \tag{3.6}$$

so the measured value (-31.7 dBm) is approximately 1 dB below. Also, a moderate deviation from the nominal center frequency is present, as previously mentioned this is the drawback of this kind of simple matching network with no tuning available.

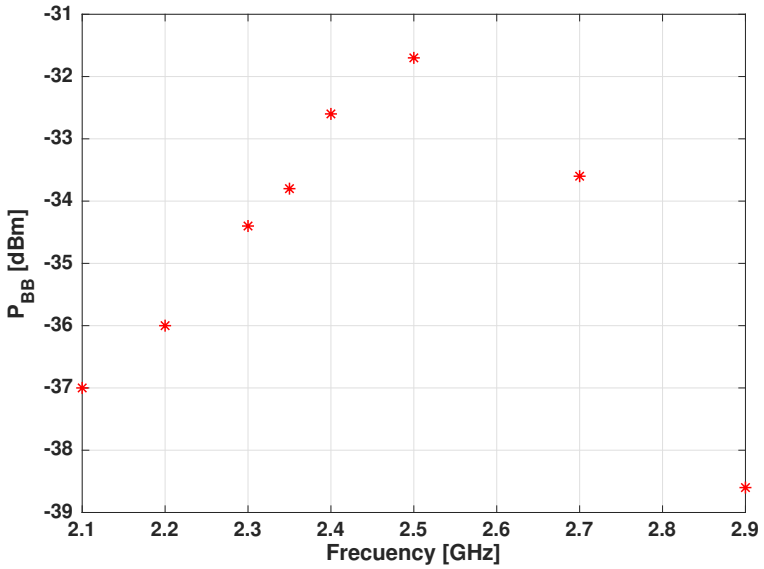

Figure 3.8: Measured baseband output power (P_{BB}) vs carrier frequency, for an AM input signal with frequency 120 Hz, input power P_{in} = -47 dBm and modulation index m = 0.5 (W = 16 μm L = 1μm, V_{DS} = 0.4 V,I_{BIAS} = 50 nA).

3.2. Envelope detector for wake-up receiver front-end

This section presents the design of an envelope detector for the front-end of a wake-up receiver. The design is based on the previously presented analysis and results with the addition of an arrangement for the bias circuit that leads to an intrinsic bandpass characteristic that improves the signal-to-noise ratio.

The implemented envelope detector is presented in Fig. 3.9. A cascode gain stage formed by transistors $MN1$ and $MN2$ and a cascode bias source enhances the output impedance to achieve higher voltage conversion gain.

The transconductance feedback architecture allows setting the DC output value through V_{ref} and provides a bandpass response, filtering the low-frequency noise ($1/f$), improving SNR.

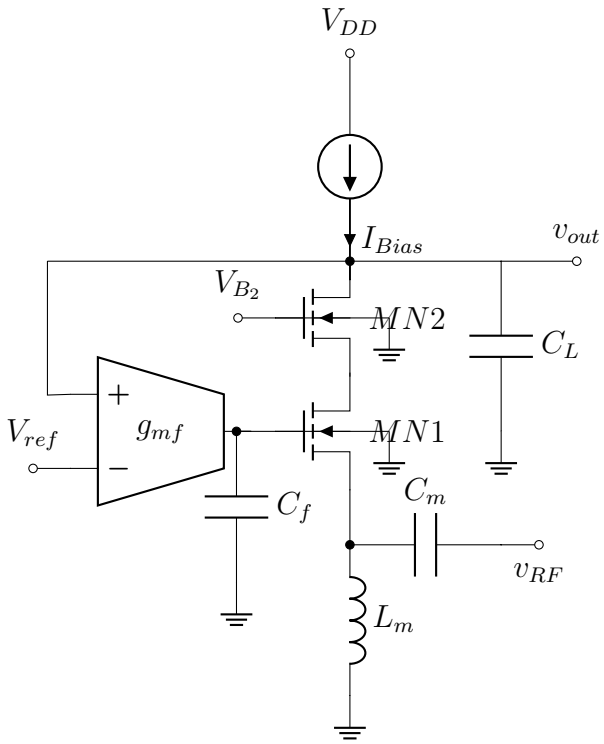

Figure 3.9: Cascoded common gate envelope detector with transconductance feedback.

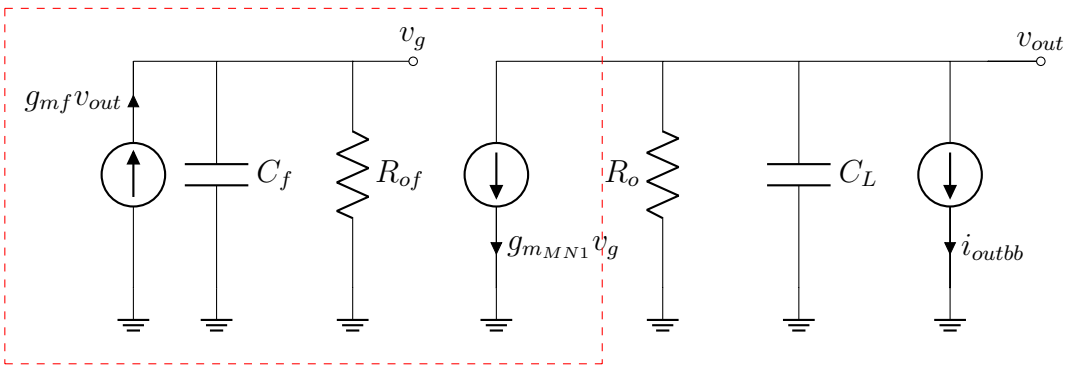

Figure 3.10: Small signal model of the circuit of Fig. 3.9.

To obtain the baseband frequency response of the circuit of Fig. 3.9 the small signal model is presented in Fig. 3.10. There R_{of} is the g_{mf} transconductance output resistance , R_o is the $MN1$, $MN2$ cascode and I_{Bias} output resistance and i_{outbb} is the baseband current generated by the $MN1$ nonlinearity as calculated in Eq. 2.3.

The $MN1$ transconductance current could be expressed as

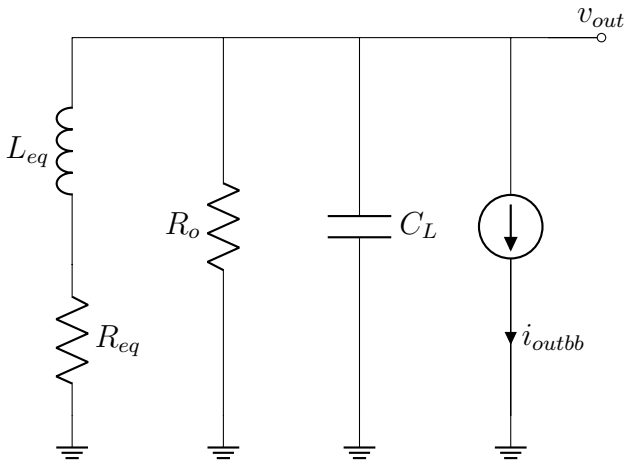

Figure 3.11: Equivalent circuit of Fig. 3.10.

$$g_{m_{MN1}} v_g = \frac{g_{m_{MN1}} g_{mf} R_{of} v_{out}}{R_{of} C_f s + 1} = \frac{v_{out}}{Z_{eq}} \tag{3.7}$$

where Z_{eq}

$$Z_{eq} = \frac{C_f s}{g_{m_{MN1}} g_{mf}} + \frac{1}{g_{m_{MN1}} g_{mf} R_{of}} = L_{eq} s + R_{eq} \tag{3.8}$$

and

$$L_{eq} = \frac{C_f}{g_{m_{MN1}} g_{mf}} \tag{3.9}$$

$$R_{eq} = \frac{1}{g_{m_{MN1}} g_{mf} R_{of}} \tag{3.10}$$

So to calculate the output voltage v_{out} as a function of the baseband current i_{outbb}, the circuit inside the red dashed lines could be substituted by a series inductance and resistance like in Fig. 3.11

The result of the central frequency and bandwidth of the bandpass response are straightforwardly calculated

$$f_c = \frac{1}{\left(2\pi \sqrt{\frac{C_f . C_L}{g_{m_{MN1}} g_{mf}}}\right)} \tag{3.11}$$

$$BW_{filter} = \frac{1}{\left(2\pi \left(R_{eqp} // R_o\right) C_L\right)} \tag{3.12}$$

where R_{eqp} is the equivalent parallel resistance of R_{eq}

$$R_{eqp} \approx Q_L^2 R_{eq} = \frac{g_{m_{MN1}} g_{mf} C_f R_{of}^2}{C_L} \frac{1}{g_{m_{MN1}} g_{mf} R_{of}} = \frac{R_{of} C_f}{C_L} \tag{3.13}$$

where Q_L is the quality factor of the inductance L_{eq} and resistance R_{eq} series at f_c.

The central frequency could be tuned by on-chip tuning of gm_f.

For the designed prototype the following specifications were considered:

- Minimal SNR of 12 dB.
- -3 dB bandwidth of at least 10 kHz, suitable for a data rate of 2.5 kbps at a BER of 10^{-3} with an OOK-based modulation. These correspond to an equivalent noise bandwidth BW_{BB} of 15.7 kHz.
- Sensitivity P_{min} of -43 dBm at source terminal. Considering at least a 6 dB improvement due to the matching network gain, the front-end sensitivity $P_{in_{min}}$ reaches -49 dBm.

The above values were those used in Fig. 2.19 which is repeated for convenience.

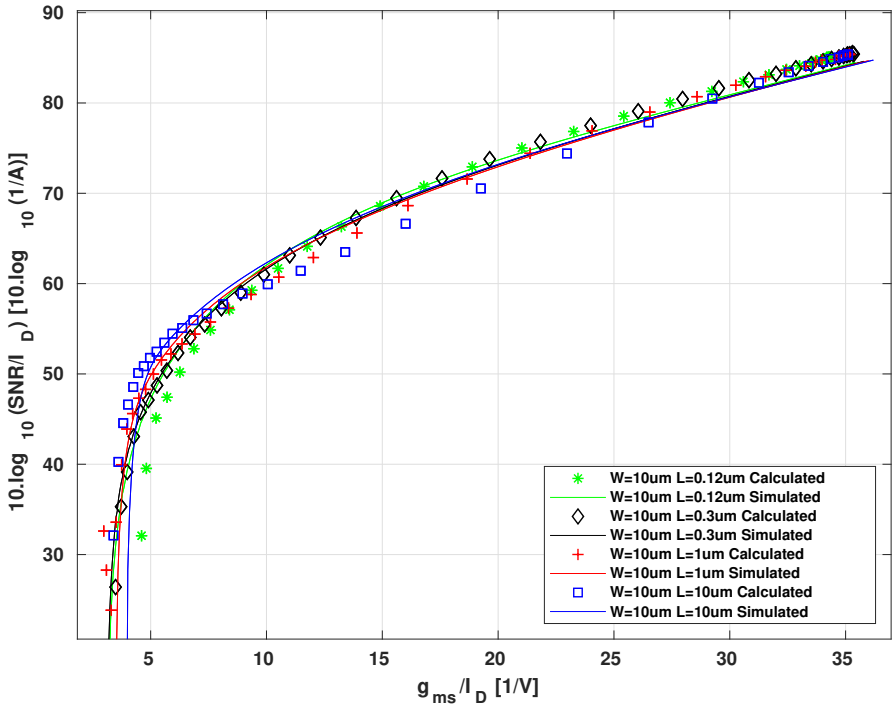

Figure 3.12: SNR/I_D for simulated and calculated from measured values of $\frac{\partial^2 I_D}{\partial V_S^2}$ and g_{ms} as a function of g_{ms}/I_D for W = 10μm, L = 0.12μm, 0.3μm, 1μm, 10μm, BW_{BB} = 15.7 kHz, δ_{nD} = 0.5, m = 0.5, v_{in} = 1.6 mV$_{rms}$ (P_{in} = -43 dBm), V_{DS} = 0.4 V.

From the curve, the maximum $10log_{10}(\frac{SNR}{I_D})$ is 86 dB. So the minimum current budget to achieve specifications, considering that the SNR = 12 dB, is 40 nA ($10log_{10}(1/40nA) = 74\ 10log_{10}(1/A)$).

The design from the previous section with the same matching network is used. The bias current of the transistor was 50 nA complying with the requirement of the previous paragraph, the size was W = 16μm and L = 1μm, which yield a g_{ms}/I_D value of 35.8 V^{-1}. The feedback transconductance value used is g_{mf} = 56 nS, and the capacitor values were C_f = 45 pF and C_L = 0.18 pF. Evaluating equation 3.11 a central frequency f_c of 16.7 kHz is obtained.

I_D [nA]	W [μm]	L [μm]	g_{ms}/I_D [1/V]	SNR/I_D [dB] ($10log_{10}(1/A)$)	C_f [pF]	C_L [pF]	f_c [kHz]	g_{mf} [nS]
50	16	1	35.8	86	45	0.18	16.7	56

Table 3.2: Design parameters values.

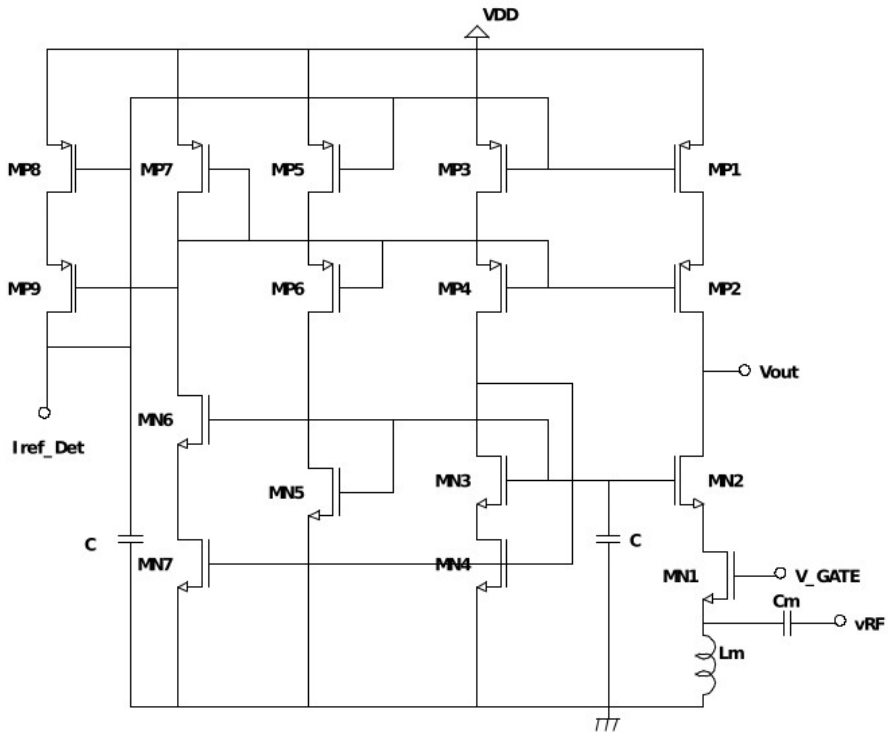

Figure 3.13: Envelope detector and bias circuit.

Component	L [μm]	W [μm]	I_D [nA]
$MN1, MN2$	1	16	50
$MN3, MN4$	1	4	12.5
$MN5$	96	2	150
$MN6, MN7$	1	16	50
$MP1, MP2$	1.25	4	50
$MP3, MP4$	1.25	1	12.5
$MP5, MP6$	1.25	12	150
$MP7$	60	0.5	50
$MP8, MP9$	1.25	4	50

Table 3.3: Transistor dimensions and current values of the circuit of Fig. 3.13.

The schematic of the detector is shown in Fig. 3.13. The bias voltages for the main transistors (MN2, MP1, MP2 in Fig. 3.13), are obtained using the design methodology presented in [Aguirre and Silveira, 2006] to set the drain voltage of the cascoded transistors above its saturation voltage.

In table 3.3 the transistor dimensions and currents are presented.

From table 3.3 the estimated total current consumption considering all branches is 312.5 nA.

The g_{mf} block is implemented with a cascoded operational transconductance

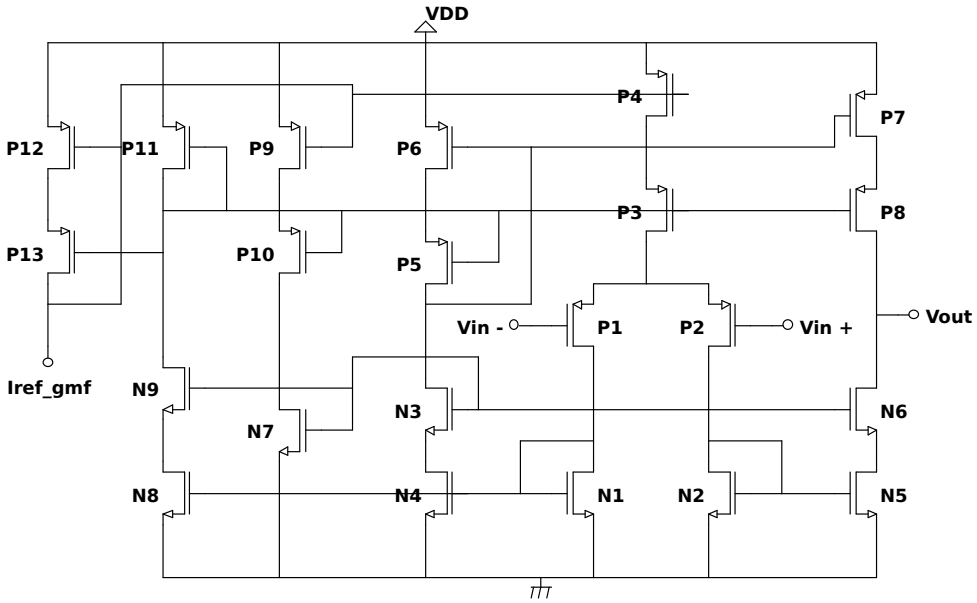

Figure 3.14: Simplified circuit of the g_{mf} transconductance.

amplifier (OTA). The g_{mf} schematic is shown in Fig. 3.14. The estimated total consumption of the g_{mf} block is 47 nA. The transistor MN1 gate and so the g_{mf} block output is externally available through a switch to have access to this key point to confirm the correct operation of the g_{mf} block. An internal buffer is added to the envelope detector output to perform the measurement. The buffer input capacitance is considered in the C_L value.

All the transistors, except for transistors MN1 and MN2, were implemented as a series or parallel association of unitary regular transistor (L = 1μm and W = 2 μm for the n-channel L = 1.25 μm and W = 0.5 μm for the p-channel). Transistors MN1 and MN2 are nfet_rf type, these RF layouts have low resistance gate connections and provide local n-well or p-well tie-downs.

The complete layout of all designed and fabricated circuits is shown in Fig. 3.15. The actual position of the cascode detector and g_{mf} circuits are pointed out, layout and dimensions of each block are also drawn and superimposed. The total front-end area, including the inductance, is 100000 μm^2.

A microphotograph of one 2.25 mm^2 fabricated die is shown in Fig. 3.16. The main cascode detector block and the test circuits, including the one presented in section 3.1, are identified.

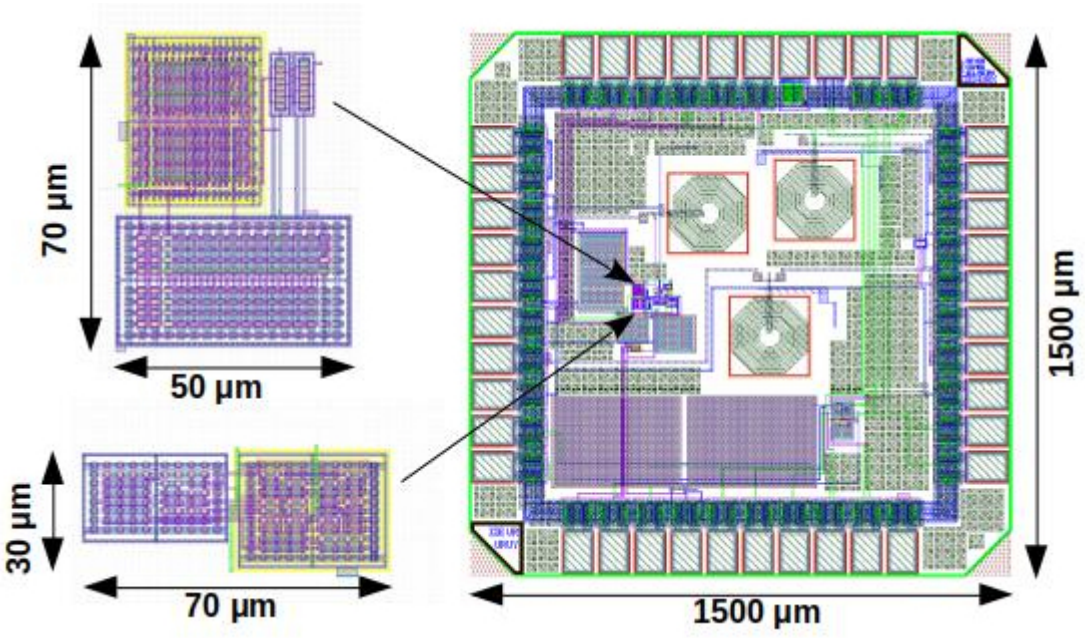

Figure 3.15: Rigth: Layout of complete 2.25 mm^2 die, top left: layout of circuit of Fig. 3.13, bottom left: layout of circuit of Fig. 3.14

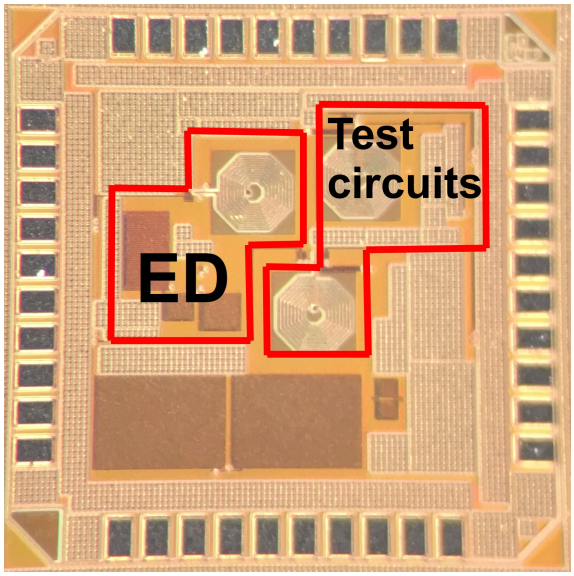

Figure 3.16: Annotated microphotograph of 2.25 mm^2 die.

3.2.1. Measurements results

To evaluate the performance of the implemented detector a modulated input signal over a carrier of 2.4 GHz is applied to the input v_{RF}. The frequency of the modulating signal is swept to assess the bandpass response. The 2.4 GHz AM modulated signal was generated with an Agilent E4438C signal generator, using

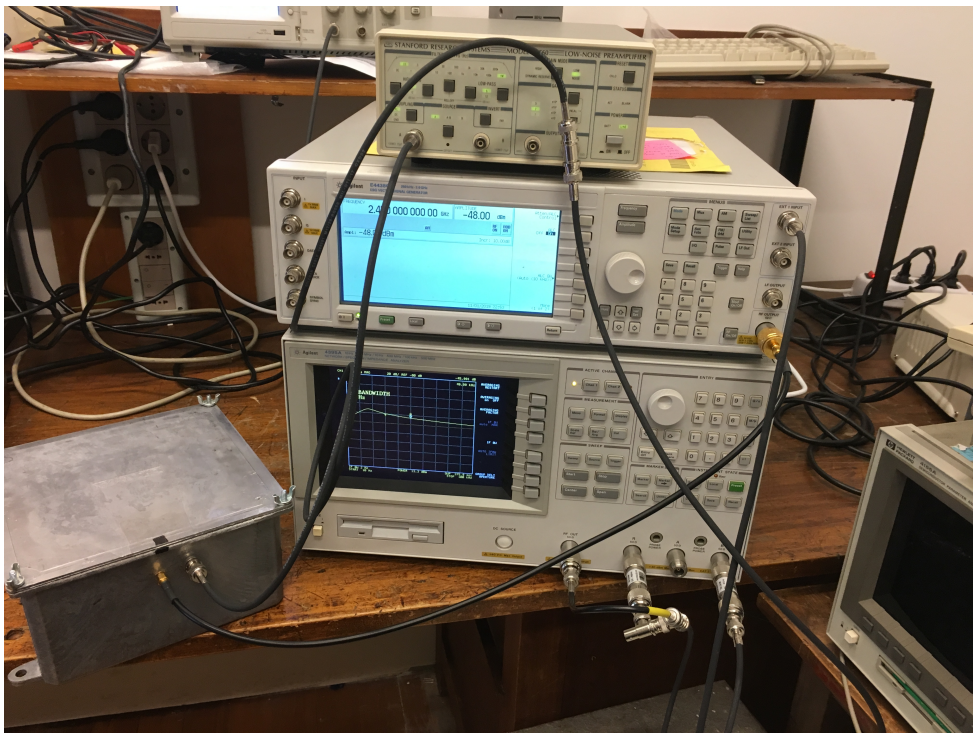

Figure 3.17: Measurement setup.

a network analyzer (Hewlett Packard 4395) to generate the modulating frequency (w_m) sweep and measure the baseband output. A low noise amplifier (Stanford Research SR560) was used to buffer the output to drive the 50 Ω network analyzer input. The output noise power was also measured using the network analyzer. A photograph of the measurement setup is shown in Fig. 3.17.

To avoid external noise in measurements a custom Faraday's box was used. The source voltages and reference currents such as V_{DD}, V_{ref}, I_{ref_Det} and I_{ref_gmf} were generated by custom circuits inside the box and battery powered. The setup circuit details are presented in B.

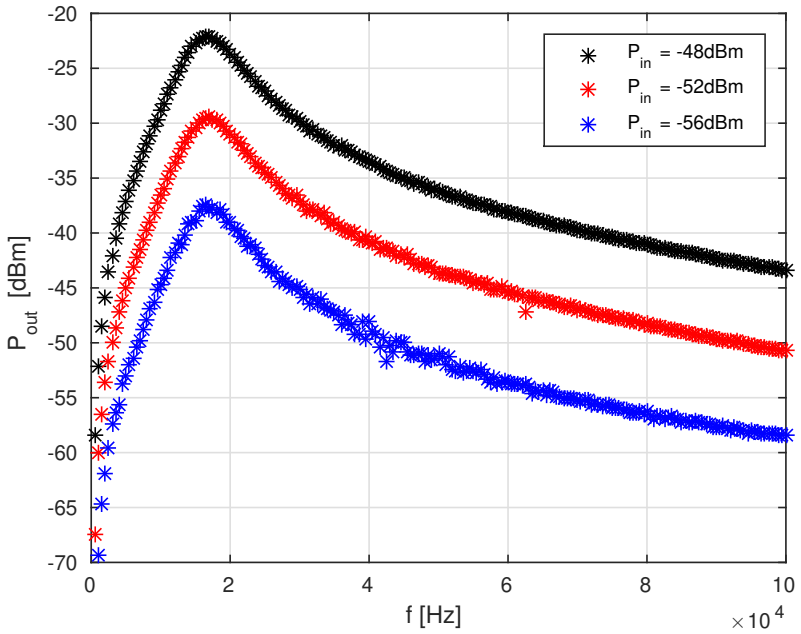

Figure 3.18: Pout vs modulating frequency for an AM input signal with carrier frequency 2.45 GHz, amplitude P_{in} = -48 dBm, -52 dBm, -56 dBm, m = 0.5.

The total measured current consumption of the envelope detector of figure 3.13 and the g_{mf} block of figure 3.14 is 406 nA. It is higher than the estimated (312.5 nA + 47 nA = 359.5 nA) but close to the simulation results (339 nA + 47 nA = 386 nA) which showed a difference in the current copies of the branch of the envelope detector of 8 % with respect to estimate. The power of the baseband output signal (P_{out}) as a function of the modulating frequency is presented in Fig.3.18, which confirms the bandpass characteristic achieved with the proposed architecture of Fig. 3.9.

The current scaling factor derived from Fig. 3.18, for P_{in} = -48 dBm, calculated considering a matching network gain of 2.1 at 2.45 GHz (estimated with test circuits), is k = 9800 1/V 2.5. This k value was derived for m equal to 1 to compare with prior works. The measured central frequency is f_c = 17 kHz.

The current consumption of the envelope detector branch and the transconductance gm_f is 100 nA from a 1.2 V power supply. The measured sensitivity, defined as the necessary input signal power of an AM modulated carrier with modulation index m = 0.5 to have a SNR = 12 dB, is -48.5 dBm. The noise power was integrated in a bandwidth of 30 kHz. Table 3.4 compares these results with prior work showing the improvement in the conversion gain/consumption trade-off.

Table 3.4: Comparison with previously published Envelope Detectors.

	[Wang et al., 2018] JSSC'18	[C. Hambeck, 2011] ISCAS'11	[van Liempd et al., 2012] ISCAS'12	[Cheng and Chen, 2017] TCAS1'17	This Work
Technology	180 nm	130 nm	90 nm	180 nm	130 nm
Carrier Frequency	113.5 MHz	868 MHz	2.4 GHz	2.4 GHz	2.4 GHz
Supply Voltage	0.4 V	1.0V	1.2 V	0.8 V	1.2 V
k	364 [1]1/V	38 [2]1/V	128 [3]1/V	90 [4]1/V	9800 1/V
Current Consumption	20 nA	1μA	1.7 μA	1.7 μA	100 nA
Baseband Bandwidth	300 Hz	1.1 MHz	-	240 kHz	10 kHz
Detector Sensitivity/WuRx Sensitivity	–/-69 [5]dBm	-61 [6]/-71 [7]dBm	-	-50 dBm/–	-48.5 dBm/–
Matching Network Gain/Integrated	25 dB/No	19.8 dB/No	-	12.5 dB/Yes	6.4 dB/Yes

[1] k_{ED} reported in this work is 2.k so the reported value was divided by 2
[2] Calculated from Fig.7 and corrected by $\pi/2$ because the first harmonic of an OOK is considered.
[3] Calculated from Fig.6
[4] Reported in Fig. 13(b).
[5] 32 bits Digital Correlator.
[6] Reported in Fig. 7
[7] 700 bits Correlator.

3.3. Conclusions

In this chapter first, a practical design with sub μA current consumption and integrated matching network was presented and the estimated results were compared to simulation and measurements, obtaining a good agreement. Then a novel envelope detector for wake-up receiver front-end is proposed. The used arrangement for the bias circuitry leads to an intrinsic bandpass characteristic that can be tuned, independently of the conversion gain value of the envelope detector. Also, the estimated results were compared to simulation and measurements, obtaining a good agreement.

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Chapter 4

Ratio Based Distortion Analysis

This chapter extends the approaches of ratio based analog design, presented in chapter 2, showing how to deal with the second and third derivatives of the drain current relevant for distortion analysis of analog circuits.

Some prior works have considered the analysis and modeling of transistor distortion with respect to the inversion level and g_m/I_D ratio.

In [da Silva et al., 2008], using ACM compact physics based model, nonlinearities in MOSFETs are presented as a function of the charge density and compared with simulation and measurements showing an acceptable accuracy. The developed model takes into account the carrier velocity saturation as the only mechanism of current degradation, showing differences with the measured results that are sensitive to the influence of other effects such as channel length modulation and mobility degradation due to the transversal field.

In [Jespers and Murmann, 2015] a long channel analytical model is applied to analyze the distortion terms and results are compared with simulations in a 65 nm CMOS process. In [Chicco et al., 2019] it is shown that a charge-based inversion level-oriented model, suitable for nanoscale MOSFETs, can adequately model the distortion characteristics. However, the aforementioned ratio based approach has not been applied to the higher-order derivatives of the current. Prior works [Jespers and Murmann, 2015] and [Chicco et al., 2019] show the dependency with g_m/I_D or IC, but for a particular transistor without discussing what to expect along the design space when W/L is changed.

In this chapter, the following novel approaches are proposed. First, a formulation based on the ratio approach (similar to what is done in g_m/I_D for the first derivative) is applied to the 2nd and 3rd derivatives of the current. In this way characteristics that are valid for all "practical"transistors of a given length of a given process (letting aside narrow transistors) are obtained. Second, it is shown that the second ($HD2$) and third order ($HD3$) distortion terms, being ratio-based, are also general characteristics determined by L and g_m/I_D. The results are based on analytical derivations and supported by simulations and measurements in a 130 nm CMOS process.

The chapter is organized as follows. Section 4.1 refreshes the concept of ratio-based design in a current process where short channel effects are very significant.

In Section 4.2 the results of extending the ratio design approach to higher-order derivatives are presented. How this translates to second and third order harmonics distortion is analyzed in Section 4.3. Finally, Section 4.4 draws the main conclusions.

The main contributions presented in this chapter are published in [Silveira and Reyes, 2023].

4.1. Ratio based analog design

Following we present an overview of alternatives applied in ratio based analog design in advanced processes.

When short channel transistors are considered, there is a slight dependency of the g_m/I_D curve on the channel length, as mentioned in section 2.3 and shown in Fig. 2.8. This dependency is more pronounced for minimum length transistors, as is already noticeable in Fig. 4.1, even in a 130 nm process. Thus, the need arises to consider the g_m/I_D curve (and other characteristics) for each considered L (o a representative curve for each range of L). Similar dependence could arise for narrow transistors, close to the minimum W, but these are seldom applied in analog design.

Considering this L dependency, an evolution of the original g_m/I_D methodology [Jespers and Murmann, 2017], applies I_D/W as variable instead of $I_D/(W/L)$. Alternatively, a similar approach can be taken when transistors are implemented based on several parallel fingers, as in FinFETs, or several parallel unit transistors. In this case, the ratio of I_D to the number of fingers or unit transistors can be considered as the normalized current. This has the advantage of naturally scaling the current as well as parasitic capacitances with the number of parallel elements. However, normalizing to W or the number of fingers instead of using $I_D/(W/L)$ or IC has the drawback that the g_m/I_D characteristic significantly changes with changing L (see Fig. 4.1). Nevertheless, both approaches (to use $I_D/(W/L)$ or I_D/W) have no significant difference, once a fixed L is considered and leads to equal results regarding what is proposed here. We will consider $I_D/(W/L)$ due to its connection with the IC and the smaller spread of the characteristic curves.

The internal (gate, inversion, and substrate) charges of the transistor, letting aside border effects most prominent in narrow channel transistors, are proportional to $W.L$, which is equal to $(W/L).L^2$. Thus, are also proportional to W/L for a given L. Hence, the first derivatives of the charges, which are the intrinsic small signal capacitive terms, are also proportional to W/L for a given L. The extrinsic capacitances are, in first approximation, proportional to $W = (W/L).L$. Therefore, as discussed in [Jespers and Murmann, 2017] gm/C, being C parasitic capacitances of the transistor is also among the W independent, g_m/I_D dependent ratios. Being the transistor f_T also related to gm/C, the figure of merit $(g_m/I_D)f_T$ proposed in [Shameli and Heydari, 2006] is also an example of a ratio sharing the characteristics of the previous ones. More recently, following the same philosophy, in [Tajalli, 2021], the use of the ratio C/I_D is considered.

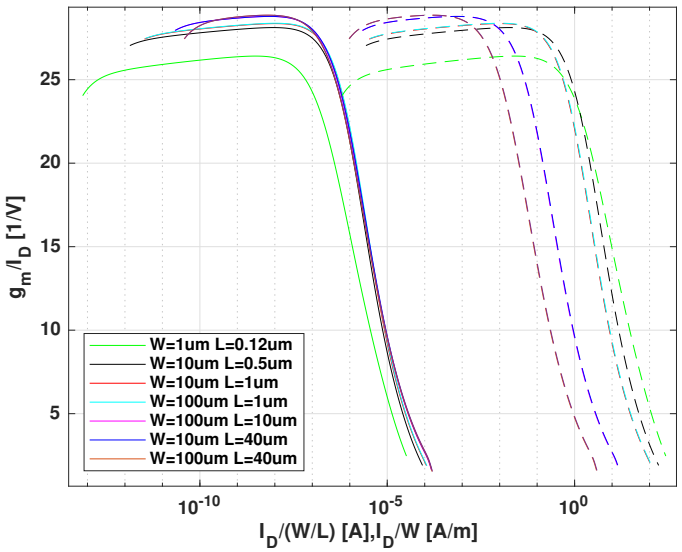

Figure 4.1: g_m/I_D as a function of $I_D/(W/L)$ (solid lines) and as a function of I_D/W (dashed lines), $V_{DS} = 0.6$ V.

4.2. Ratio based variables for higher order drain current derivatives

As shown in chapter 2 nonlinear details of the nanometer transistor I-V characteristic are captured by dc simulations using the foundry simulation model [R. Fiorelli, 2011] or dc measurements.

Figs. 4.2 and 4.3 show the second and third derivatives of the drain current with respect to the gate voltage, calculated from dc simulation and dc measurements data. These will be noted here respectively as g_{m2} and g_{m3}

$$g_{m2} = \left(\frac{\partial^2 I_D}{\partial V_G^2}\right) \tag{4.1}$$

$$g_{m3} = \left(\frac{\partial^3 I_D}{\partial V_G^3}\right) \tag{4.2}$$

The derivatives are plotted as a function of g_m/I_D for several W and $L = 1$ μm in a 130 nm CMOS process. These figures illustrate that these derivatives depend on g_m/I_D but also on W/L (or alternatively I_D). Additionally, in Fig. 4.3 it can be seen the well-known null of g_{m3} [Toole et al., 2004], [W.Sansen, 2018].

To guide the design process, it is convenient to have a variable related to the higher order derivatives that is only determined by g_m/I_D. This is achieved through a ratio based design approach considering the ratio of the higher-order derivatives to the drain current. In chapter 2 proof that the 2nd derivative depends only on g_m/I_D was done. This can be extended to higher-order derivatives with a proof based on the properties of derivatives. Nevertheless, this is readily understood

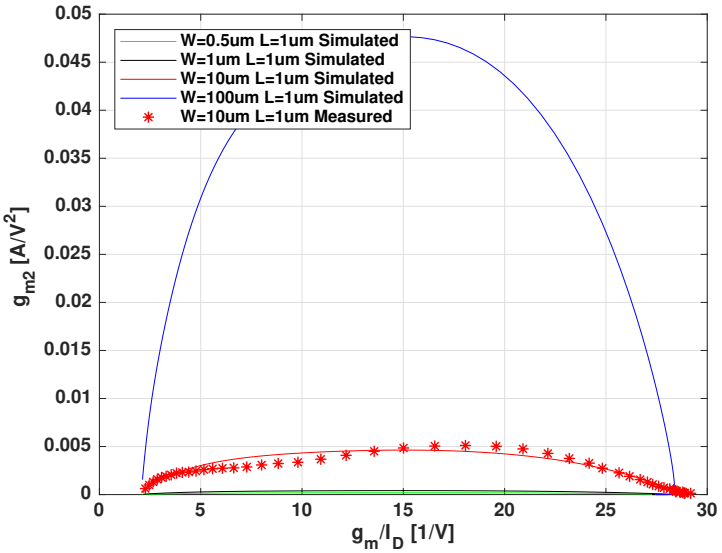

Figure 4.2: Second derivative simulated for W = 0.5 μm, 1 μm, 10 μm, 100 μm, and L = 1 μm and measured for W = 10 μm and L = 1 μm, V_{DS} = 0.6 V.

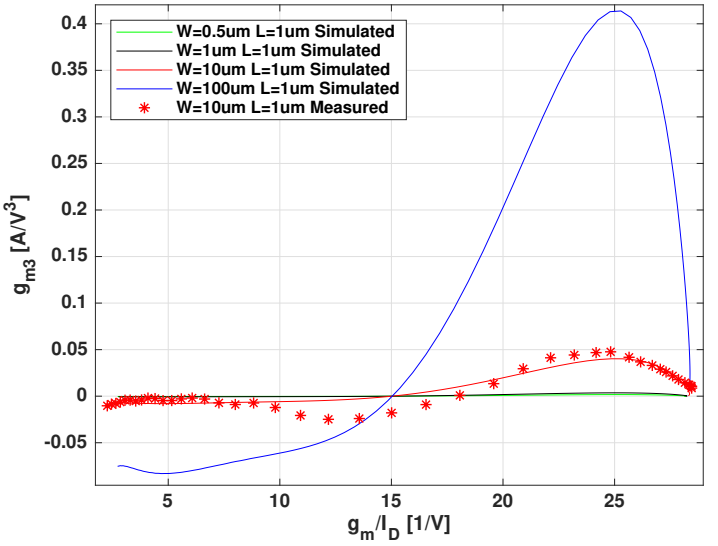

Figure 4.3: Third derivative simulated for W = 0.5 μm, 1 μm, 10 μm, 100 μm, and L = 1 μm and measured for W = 10 μm and L = 1 μm, V_{DS} = 0.6 V.

considering the same reasoning previously done for g_m/I_D. Being I_D proportional to W/L for a given L, the first derivative is also proportional to W/L and, hence g_m/I_D is independent of W/L, being determined only by the terminal voltages and, hence, by $I_D/(W/L)$. This same reasoning applies to the higher order derivatives, and hence the second and third derivatives of the current divided by the current

will be determined by g_m/I_D (or equivalently $I_D/(W/L)$).

The higher-order derivatives simulation and measurement data previously shown in Figs. 4.2 and 4.3 are plotted divided by the corresponding I_D in Figs 4.4 and 4.5. It can be appreciated the dependency on g_m/I_D and the independence of transistor sizes.

Next, we consider the ratio of the second and third derivatives to I_D for transistors with different lengths. The results are shown in Fig. 4.6 for the second derivative and in Fig. 4.7 for the third derivative. Though the dependence with L is visible, especially for the third derivative, it can be seen that this dependence maintains anyway the overall shape of the curves and that these curves are close to each other.

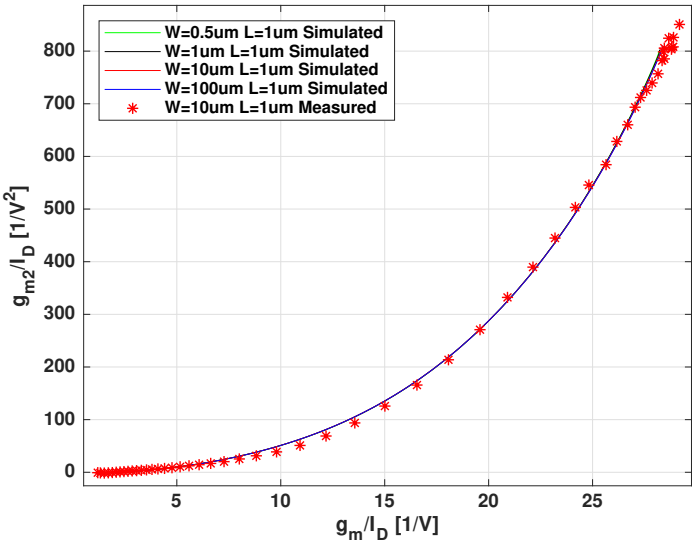

Figure 4.4: Second derivative over I_D simulated W = 0.5 μm, 1 μm, 10 μm, 100 μm, and L = 1 μm and measured for W = 10 μm and L = 1 μm, V_{DS} = 0.6 V.

4.3. Harmonic Distortion

Most analog design techniques are based on the linearity of the small signal characteristic of the transistor. Therefore, distortion characteristics are key to assessing the limits and differences from the small signal, first-order, approximation. In what follows we will only consider the main distortion mechanism related to the non-linearity of the I_D current at constant drain voltage. In an actual circuit, the drain voltage will usually also vary and additional distortion components will arise. The common metrics to evaluate second and third order distortion are $HD2$ and $HD3$ defined as the ratio of the amplitude of the second and third harmonic versus the amplitude of the fundamental respectively. Those are related to the second

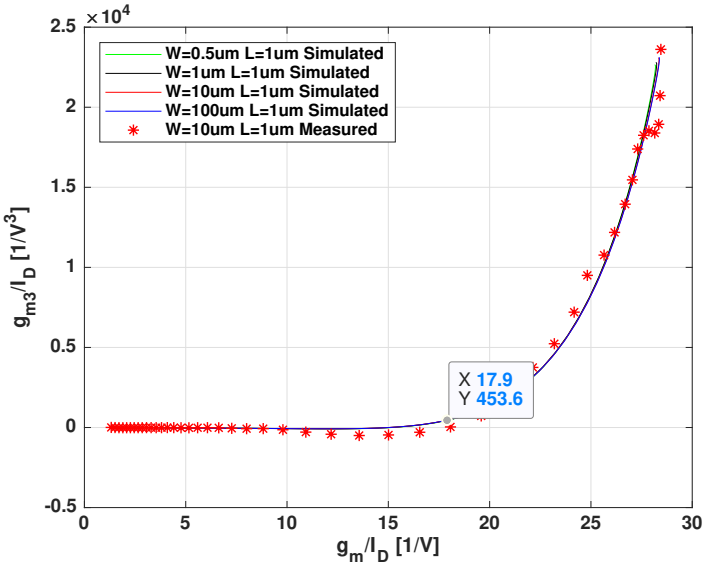

Figure 4.5: Third derivative over I_D simulated for W = 0.5 μm, 1 μm, 10 μm, 100 μm, and L = 1 μm and measured for W = 10 μm and L = 1 μm, V_{DS} = 0.6 V. The point used as an example is marked.

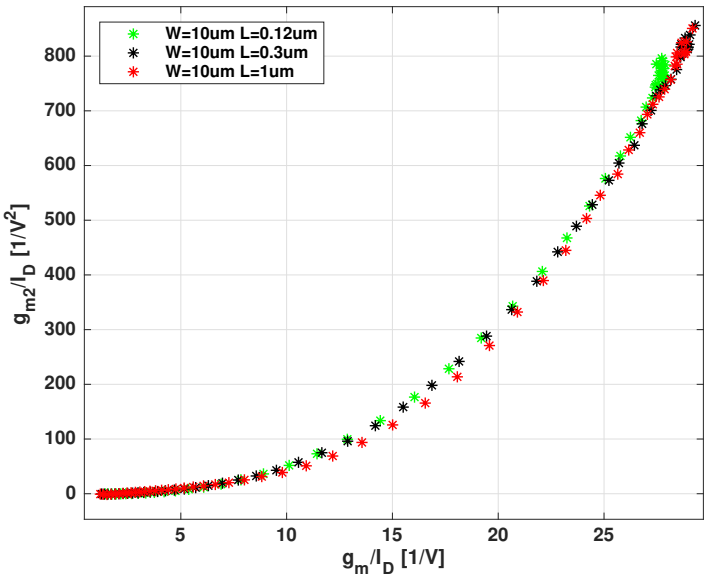

Figure 4.6: Second derivative over I_D from measurements for W = 10 μm, and L = 0.12, 0.3, 1 μm, V_{DS} = 0.6 V.

and third order derivatives of the drain current by the following equations [Chicco et al., 2019].

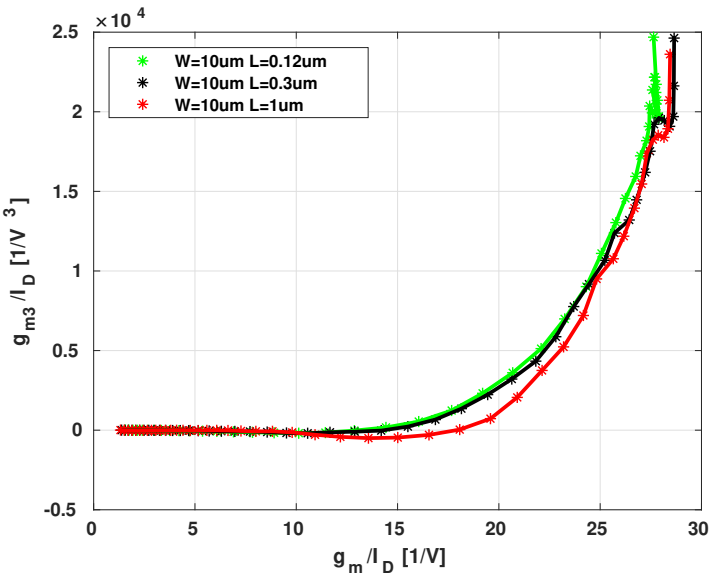

Figure 4.7: Third derivative over I_D from measurements for W = 10 μm, and L = 0.12, 0.3, 1 μm, V_{DS} = 0.6 V.

$$HD2 = \left| \frac{2g_{m2}A}{8g_m + g_{m3}A^2} \right| \approx \left| \frac{g_{m2}A}{4g_m} \right| \tag{4.3}$$

$$HD3 = \left| \frac{g_{m3}A^2}{3\left(8g_m + g_{m3}A\right)} \right| \approx \left| \frac{g_{m3}A^2}{24g_m} \right| \tag{4.4}$$

where A is the sinusoidal signal amplitude.

Since $HD2$ and $HD3$ are based on ratios of current derivatives, they will also be defined by the g_m/I_D value for a given L. This is visible in Fig. 4.8, where it can be appreciated the close coincidence of the HD2 curves even for different transistor lengths, for the HD3 term the plot approximately coincides in transistors with the same length. For different transistor lengths, the difference between curves in HD3 arises mainly because of the variation of λ_c 2.34 with transistor length, which determines the IC (g_m/I_D) value for which the null occurs. [W.Sansen, 2018].

Furthermore, these ratios can be expressed as a function of the high-order derivative over I_D divided by g_m/I_D. Therefore the ratios needed to calculate HDn can be directly obtained from characteristics such as the ones shown in Figs 4.4 and 4.5 for the corresponding L value. For example from figure 4.5 the $HD3$ for the point marked and for a signal amplitude $A = 10mV$ could be directly calculated using Eq. 4.4 and expressed in dB as

$$HD3 = 20 * log_{10} \left| \frac{453.6V^{-3} * (10mV)^2}{24 * 17.9V^{-1}} \right| = -79.5dB \tag{4.5}$$

Fig. 4.9 shows HD3 obtained in two ways. First, simulating with typical model parameters provided by the foundry and applying Eq. 4.4 as shown in the previous

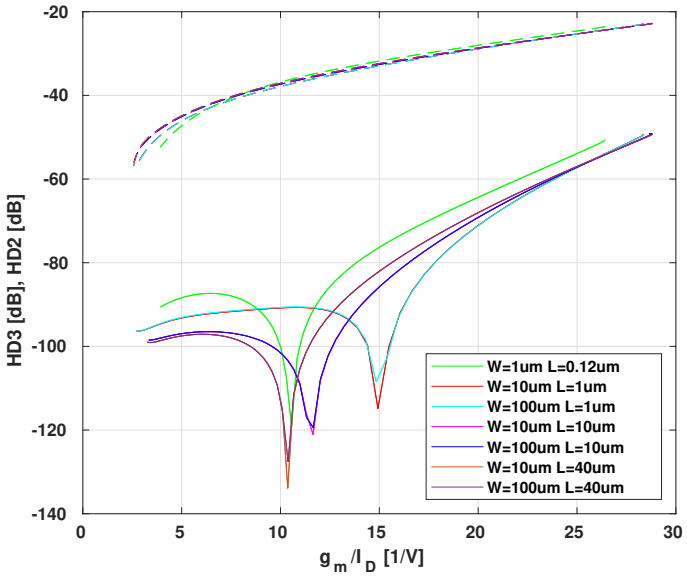

Figure 4.8: Second (dashed lines) and Third (solid lines) Harmonic Distortion terms from simulated data, V_{DS} = 0.6 V and A = 10 mV.

example (solid blue line). Second, the HD3 is directly obtained from QPSS simulation (red points) showing the coincidence between these independent methods.

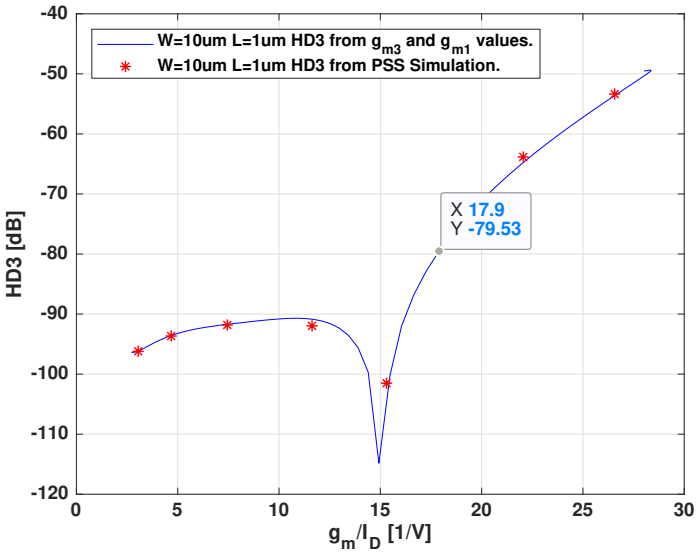

Figure 4.9: Third Harmonic Distortion calculated with Eq. 4.4 and from PSS simulation for W = 10 μm and L = 1 μm, V_{DS} = 0.6 V and A = 10 mV. The example of Eq. 4.5 is marked.

4.4. Conclusions

This chapter first presents an overview of design methodologies that stem from the g_m/I_D method and that can be identified as ratio-based. They take advantage of using the ratio of key parameters that, for each transistor length, are solely defined by the value of g_m/I_D. Then, this general idea was applied to the second and third order derivatives of the drain current. Showing, analytically and supported by simulation and measurement, that the ratio of these derivatives to the drain current, provides characteristic curves that depend only on g_m/I_D for a given transistor length. These characteristic curves can be applied to guide the design process and in particular the harmonic distortion assessment.

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Chapter 5

Conclusions

5.1. Conclusions

This thesis contributes several new design approaches and tools for dealing with the non-linearity of MOS transistor circuits and presents direct applications on an envelope detector design for a WUpRx.

The following paragraphs highlight the main contributions of this work.

- The EKV model for the MOS transistor is presented and used to highlight the physical characteristics that define the behavior of the second derivative $\frac{\partial^2 I_D}{\partial V_S^2}$. This derivative directly impacts the operation and performance of the envelope detector. This resulting behavior is confirmed through simulations and measurements.

- A novel figure of merit to aid the design, showing the efficiency in terms of the second derivative value obtained per current drain value is presented as a function of the g_{ms}/I_D value. It is worth remembering that the value of the second derivative translates directly into the value of the conversion gain 2.4 or scaling factor 2.5 of an envelope detector. It is demonstrated that this figure of merit only depends on the inversion level and is confirmed through simulations and measurements.

- Guided by previously mentioned results a practical envelope detector circuit with sub μA current consumption and integrated matching network, was designed, fabricated, and measured presenting consistent results with the design approach predictions.

- After analyzing the noise present in an envelope detector and considering that under certain circumstances, which may be satisfied in a wide range of cases, the thermal noise of the transistor channel is the dominant contributor a new figure of merit is proposed. This new figure of merit relates to the usual specifications of the circuit, namely signal-to-noise ratio (SNR), current budget (I_D), baseband bandwidth (BW_{BB}), input power (Pin), and a term that is determined by the technology and bias point chosen and can be

obtained as a function of g_{ms}/I_D. Again it also only depends on the inversion level and is confirmed through simulations and measurements.

- Using the last mentioned figure of merit an enhanced envelope detector was designed, fabricated, and measured. An arrangement for the bias circuitry of the envelope detector front-end is proposed that leads to an intrinsic bandpass characteristic that can be tuned, independently of the conversion gain value of the envelope detector, changing a bias current and/or a capacitor. This bandpass response filters the low-frequency noise (1/f), thus improving SNR. Measured results achieve a very high scaling factor of 9800 V^{-1} with a current consumption of 100 nA at 12 dB SNR and -48.5 dBm sensitivity.
- It is shown, based on analytical derivations, simulations, and measurements, how the ratio based analog approach can be extended to include the second and third derivatives of the current and the distortion terms related to them. This contribution provides a tool to guide the design process in aspects related to distortion assessment.

5.2. Future work

- Some further work can be performed to improve the conversion gain, particularly regarding the matching network. A matching network with available tuning would allow adjustment of center frequency deviation due to parasitic variation or component tolerance.
- A complete WUpRx, including the low-frequency baseband amplifier and digital baseband signal processing, e.g. correlation/coding could be built to test, evaluate, and compare the performance with other complete systems. These added blocks would ultimately not generate a significant power consumption penalty because digital circuits fully benefit from the increased performance of advanced processes.
- About the previous point, an optimized bias for low power must be performed, to reduce the current total budget.
- Conduct research regarding the variability of the proposed figures of merit for different technologies.

Appendix A

Corner Simulations

To evaluate the influence of the transistor process variation on the design, the sweep to extract I_D was conducted for each MOS transistor corner model (figure A.1 and the second derivative of this current with respect to source voltage calculated as shown in figure A.2. The variations on the second derivative value are around 10 % for the functional corners ssf, fff (+/- 3 sigma).

In the case of the figure of merit of the second derivative over I_D the variations are much smaller confirming the invariability of this figure, showing that the current and the second derivative are affected in the same way as shown in figure A.3.

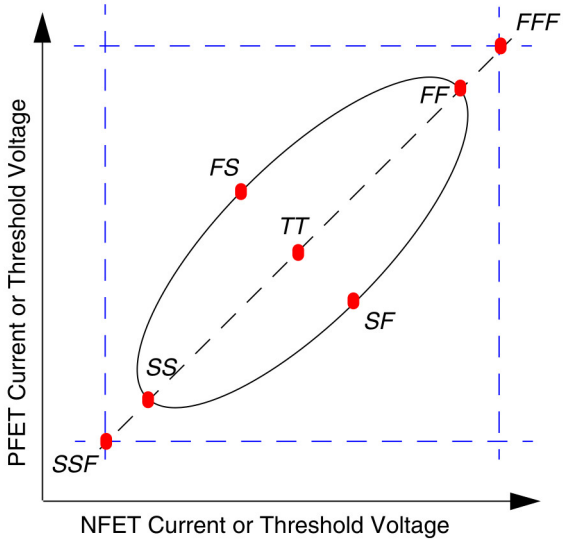

Figure A.1: Graphical Representation of MOSFET Fixed Corners. Specification limits are shown as dashed blue lines, and the various fixed corners are shown as red dots. The ellipse represents a cloud of statistical data. Taken from [IBMCorporation, 2010]

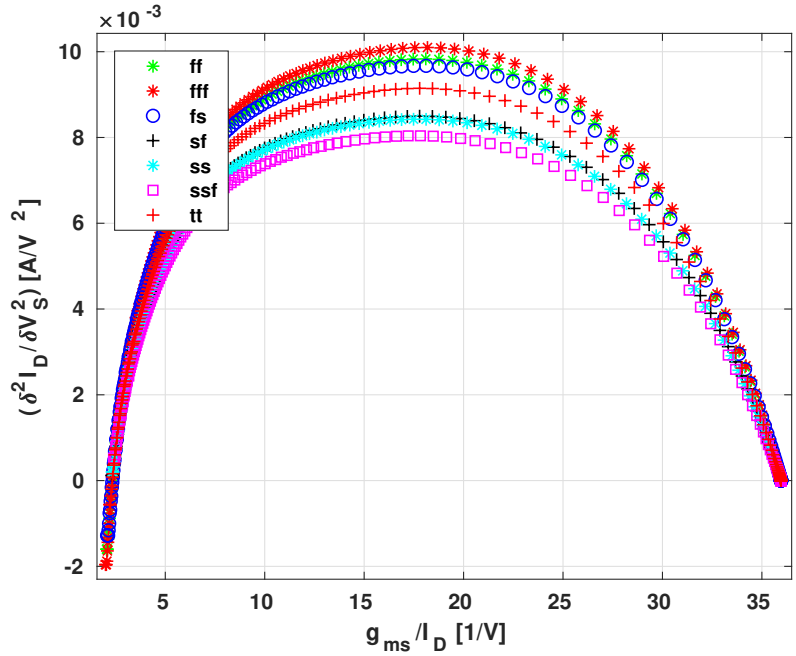

Figure A.2: Simulated second derivative $\left(\frac{\partial^2 I_D}{\partial V_S^2}\right)$ as a function of g_{ms}/I_D for W = 16 μm, L = 1 μm, V_{DS} = 0.6 V and for all corner models.

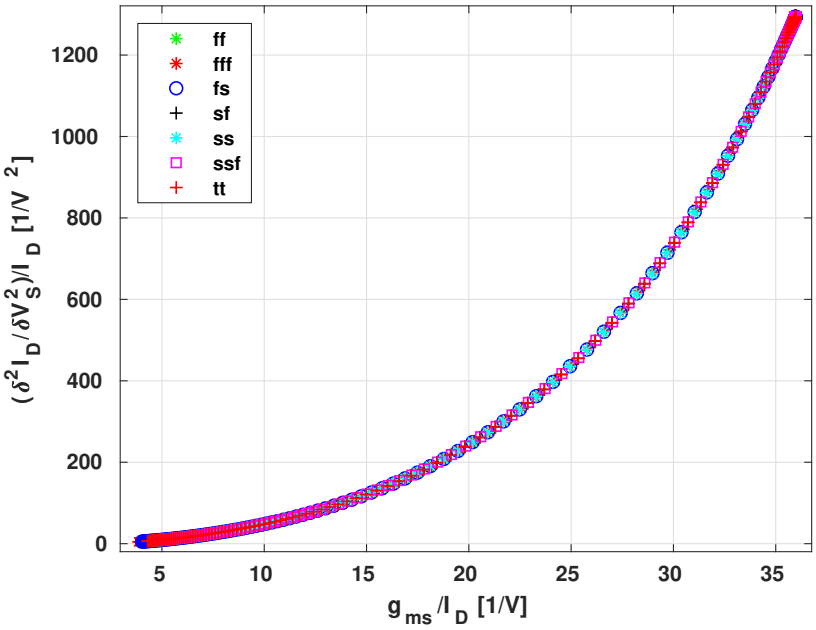

Figure A.3: Second Derivative over I_D as a function of g_{ms}/I_D for for W = 16 μm, L = 1 μm, V_{DS} = 0.6 V and for all corner models.

Appendix B

Measurements Setup

As mentioned in chapter 3, to avoid external noise in measurements the fabricated designs were characterized inside a Faraday's box. The bias and source voltages and currents were generated with battery-powered custom circuits.

In figure B.1 the used circuit to implement the reference currents, taken from [LinearTechnology, 2007], is shown. By varying the dc voltage applied in Vin between ± 5 V, the output current Iout varies between ± 250 nA.

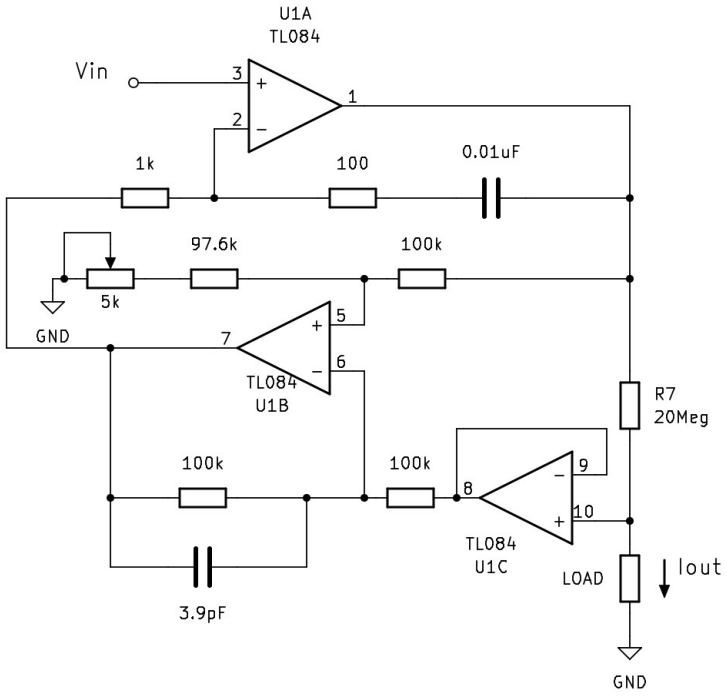

Figure B.1: Current source schematic.

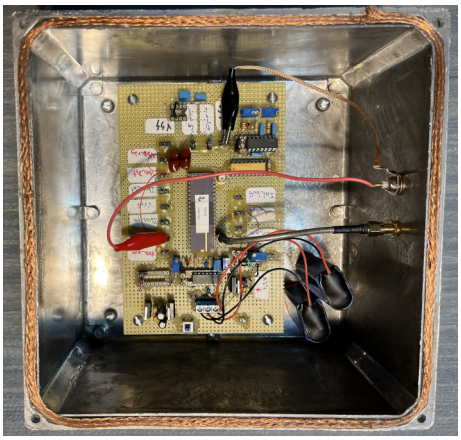

Figure B.2: Setup Box.

In Fig. B.2 the setup board and the custom Faraday's box are shown.

Common Gate Envelope Detector Bias

The measurement setup used to characterize the common gate envelope detector of section 3.1 is shown in figure B.3. The feedback loop formed by the follower, $R1$, $R2$ and Cf fix the DC output value V_{OUT} to

$$V_{OUT} = V_G \frac{R1 + R2}{R2} \tag{B.1}$$

where VG is the dc gate voltage when $I_D = I_{Bias}$. The capacitor C_L represents the input capacitance of the low noise amplifier used to buffer the output.

The seen impedance by the baseband current i_{outbb}, generated by the M1 nonlinearity, has a similar behavior with the circuit analyzed in section 3.2. That is to say, it presents a band-pass behavior.

The small signal model of the circuit of Fig. B.3 is presented in Fig. B.4. There Ro and $g_{m_{M1}}$ are the M1 output resistance and gate transconductance respectively. The seen impedance is

$$Z_v = \frac{v_{out}}{i_{outbb}} = \frac{Ro\left(R_2R_1C_fw + R_1 + R_2\right)}{\left(Rog_{m_{M1}}R1 + \left(R_1R_2C_fw + R_1 + R_2\right)\left(RoC_Lw + 1\right)\right)} \tag{B.2}$$

were $w = 2\pi f$ is the angular frequency. The evaluation of equation B.2 for the values of table B.1 is shown in figure B.5. For the peak value, the impedance is equal to Ro.

$R1$ [MegΩ]	$R2$ [MegΩ]	Ro [MegΩ]	C_f $[nF]$	C_L $[pF]$	$g_{m_{M1}}$ μS
1.5	10	40	470	17	1.5

Table B.1: Setup components and parameters values.

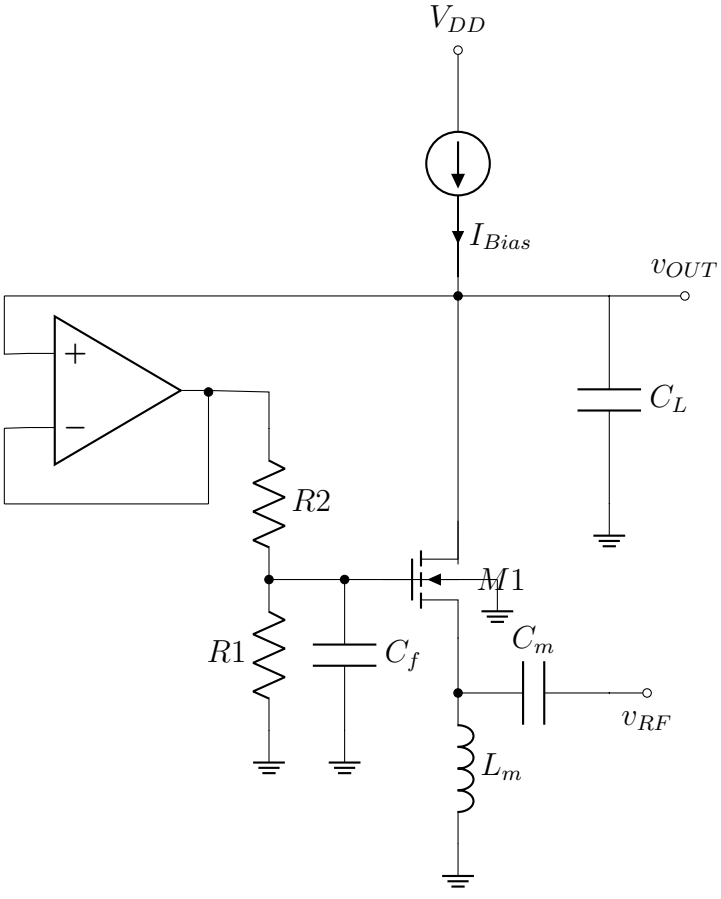

Figure B.3: Common gate envelope detector measurement setup circuit.

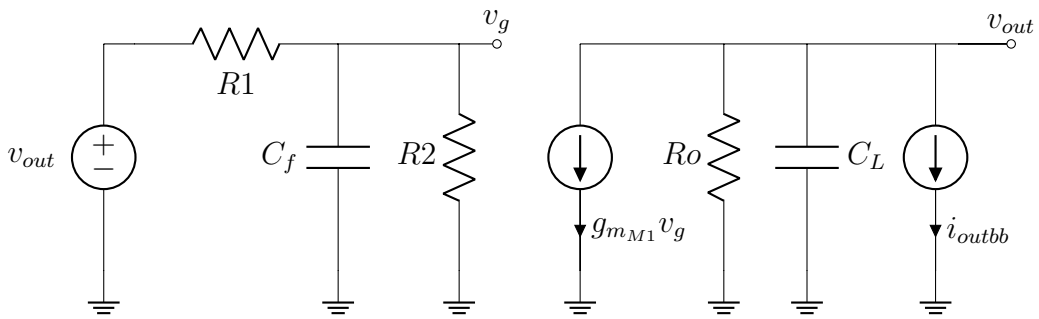

Figure B.4: Small signal model of the circuit of Fig. B.3.

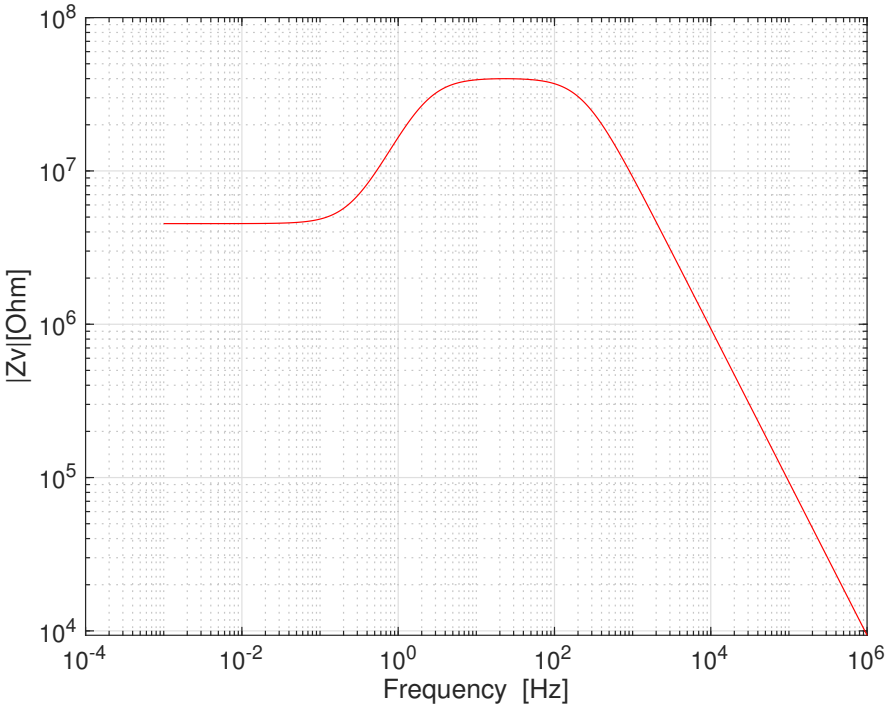

Figure B.5: $|Z_v| = |\frac{v_{out}}{i_{outbb}}|$ for the values of table B.1.

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List of Tables

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List of Figures

Esta es la última página.
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