Gate Drive Losses Reduction in Switched-Capacitor DC-DC Converters

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***Abstract*—Switched-capacitor (SC) DC-DC converters have significant losses due to the gate drive of the switches that implement the converter. This study proposes to use a charge sharing technique that can greatly reduce these losses, thus improving the converter efficiency. First we present a theoretical analysis of the technique to highlight the benefits that can be obtained. The technique was applied in an ultra-low-power SC DC-DC converter simulated in a 130 nm CMOS technology. The technique reduces the gate drive power consumption of the DC-DC converter switches by 40.5%, which accounts for an improvement up to 4% in the overall converter efficiency.**

***Index Terms*—Switched-capacitor DC-DC Converter, Low Energy, Low Power, Charge Recycling, Charge Sharing, Charge Reusing, Gate Drive Losses**

I. Introduction

The demand for portable devices and the continuous trend towards the Internet of Things (IoT) have made energy consumption one of the main concerns in the industry and of researchers. The most efficient way of reducing the energy consumption of digital circuits is decreasing the supply voltage (V_{DD}) since the dynamic energy quadratically depends on V_{DD}. In order to obtain these low supply voltages, on-chip DC-DC converters with high efficiency are needed.

When considering fully integrated DC-DC converters, switched-capacitors (SCs) have shown to be the most efficient [1]. This is mainly because low-dropout (LDO) regulators present low efficiencies at low output voltages and buck converters require inductors that cannot be integrated with high quality factors. Thus, in this work, we focus on SC fully integrated DC-DC step-down converters.

The efficiency of these converters is defined by Eq. (1) where P_L is the power delivered to the load and P_{Losses} are the total power losses. The most important of the latter are the conduction losses, the gate drive losses (due to the switches that implement the converter), parasitic capacitance losses (such as top/bottom plate parasitic capacitances) and additional logic losses.

$$\eta = \frac{P_L}{P_L + P_{Losses}} \tag{1}$$

From a general point of view, a significant part of the energy dissipation in ICs is due to capacitances (C) that are periodically charged to V_{DD} and discharged to GND. This is the case of the aforementioned gate drive losses and parasitic capacitance losses. When they are charged to V_{DD}, a charge $C.V_{DD}$ is taken from the V_{DD} power supply, thus consuming $C.V_{DD}^2$ energy and storing $1/2C.V_{DD}^2$ in C. When C is discharged to GND, the stored energy is lost (dissipated in the discharging circuit). Several techniques have been proposed in order to reduce these energy losses. A group of them involve reusing the charge stored in a capacitor instead of fully discharge it to GND.

The first and more general is known as stepwise charging [2]. It consists of storing on auxiliary capacitors part of the charge and hence the energy that would otherwise be dumped each time a capacitor is discharged. During the charge process, most of the charge is taken from these auxiliary storage capacitors instead of taking it all from the V_{DD} power supply. This technique has been proposed to be used in several applications such as the drive of PADs capacitances [3] and dynamic voltage scaling [4]. The disadvantage of this technique is the complexity added to the capacitor driver as well as the area overhead due to the auxiliary capacitors.

A simplification of stepwise charging involves temporarily storing part of the capacitor charge that needs to be discharged on a single tank capacitor and later reusing it in the charging process of another capacitor. For example in [5] this idea is used in the routing consumption of FPGAs.

Finally, the most simple approach consists of sharing the charge between two capacitors. Instead of discharging a capacitor to ground, a connection is made to another one that simultaneously requires charge, hence the charge is reused and the energy consumption is reduced. For example in [6] they use it in predecoder lines of ROM memories and in [7] in power gated digital circuits. We will call this the charge sharing (CS) technique.

In the particular case of SC DC-DC converters, there are some works that try to reduce the losses due to the charge/discharge of a parasitic capacitance. For example, in [8] we proposed to use a CS technique to reduce the top/bottom-plate parasitic capacitances losses. In [9] it is proposed to use LC tanks to temporarily store the energy consumed by the gate drive circuit of the switches that implement the converter. The main disadvantage is that integrated inductors are needed. Other works, for example [10] proposed to reuse the charge spent during the driving of the switches by delivering it to the load. Finally, in [11] the authors used an auxiliary capacitor in order to recycle this energy. However, the charge sharing approach has not been applied, as far as we know, in the gate drive of switched-capacitor DC/DC converters. In this work we

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propose to use the charge sharing (CS) technique to reduce the energy consumed in driving the switches that implement SC DC-DC converters.

When nMOS and pMOS switches are used in the same phase of the converter, there are capacitances that need to be discharged and charged at the same time. By sharing this charge, the total energy spent can be reduced. This avoids the use of complex driving circuits and additional auxiliary capacitors.

This work is organized as follows. In Section II a general analysis of the CS technique is presented. Additionally, limitations of the technique regarding the capacitances values and the maximum frequency of charge-discharge are discussed. In Section III simulations of a SC DC-DC converter are shown, which demonstrates the benefit obtained by using the proposed driving circuit. Finally, in Section IV conclusions are drawn.

II. Analysis of the Charge Sharing Technique

In this section we present a general analysis of the charge sharing (CS) technique. We address the question on when the use of this technique is suitable and how much energy can be saved. The problem is specified by three parameters, the capacitance $C1$ that needs to be charged (discharged), the capacitance $C2$ that needs to be discharged (charged) at the same time and the time available for the charge/discharge (T_{CD}) process.

In order to compare the classic driving circuit with a driving circuit that implements the CS technique, we can calculate the energy spent in a complete cycle where both capacitors are charged and discharged for both circuits.

In a classic implementation, the energy spent is first due to the charging of the capacitors itself and can be calculated with Eq. 2.

$$E_{C1} = C1 \times V_{dd}^2 \text{ and } E_{C2} = C2 \times V_{dd}^2 \quad (2)$$

The second source of energy consumption is due to the driving of switches that charge (discharge) the capacitors (E_{SW}). First, the resistance of each switch is calculated to fulfill the timing restrictions imposed by the target T_{CD}. Then through electrical simulations the width of the switches (W_{SW}) to obtain that resistance and its gate capacitance (C_{SW}) can be obtained and therefore E_{SW}.

Figure 1 shows the basic idea of the CS technique. When this technique is applied, the time T_{CD} is divided into two phases, the first one where the two capacitors are connected together through the exchange switch (SW_{Ex}) and a second phase where each capacitor is charged/discharged through a classic driver (SW_{CC1}, SW_{DC1}, SW_{CC2}, SW_{DC2}). Figure 2 shows the signals involved in both cases, with and without the CS technique.

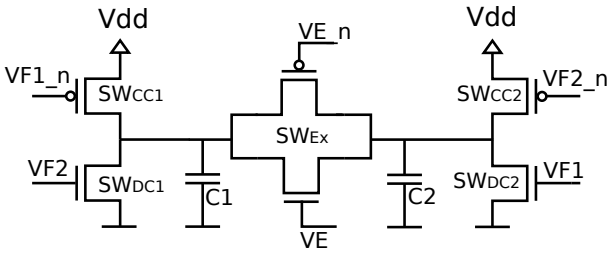

Fig. 1: Charge sharing technique.

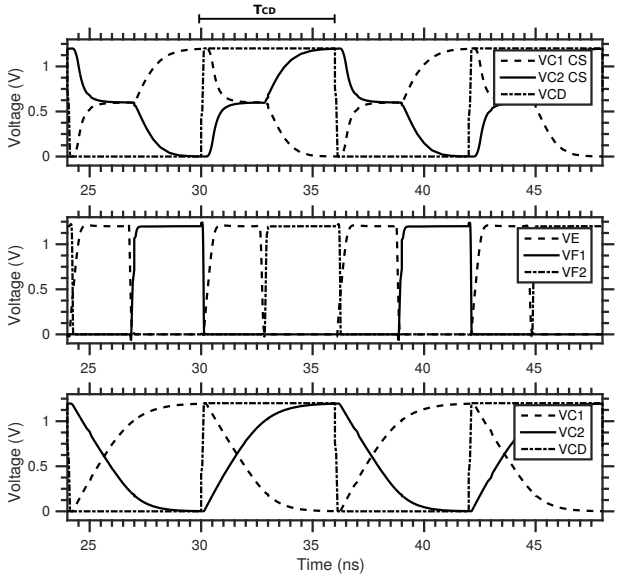

Fig. 2: Charge sharing technique example signals. An edge in VCD indicates that the capacitors have to start charging/discharging. VC1 CS and VC2 CS are the voltage in the two capacitors whereas using the CS technique and VC1 and VC2 are without using the technique. The signals showed in the second graph correspond to the nodes with the same name in Fig. 1.

The energy spent to charge the capacitor is reduced since after the exchange phase each capacitor already has energy stored in it. The energy spent to finish charging each capacitor can be calculated with Eq. 3.

$$E_{C1_{CS}} = \frac{C1^2}{C1+C2} \times V_{dd}^2 \quad E_{C2_{CS}} = \frac{C2^2}{C1+C2} \times V_{dd}^2 \quad (3)$$

Additionally, while using CS the E_{SW} increases since an additional switch (SW_{Ex}) is needed. The procedure to obtain this energy is the same as in the classic driver.

Finally, the technique needs a logic block to generate the signals shown in the second graph of Fig. 2 (VE, VF1, VF2) from the charge/discharge signal (VCD). To generate these signals, a non overlapping pulse generator is needed. Figure 3 shows the architecture used to generate a pulse with a specific width [12]. An edge in signal IN will produce a pulse in signal $PULSE$ (VE). The width of this pulse will be determined by the delay of the inverters between the two inputs of the XOR gate. In this case current starved inverters are used to control the delay. With some simple additional logic VF1 and VF2 can be obtained from the output of this block. The energy spent by this block will be referred as E_{Log}. Although this architecture might be affected by mismatch and process variations, the exact width of the pulses is not critical, they just need to be long enough to allow the charge transfer between the two capacitors.

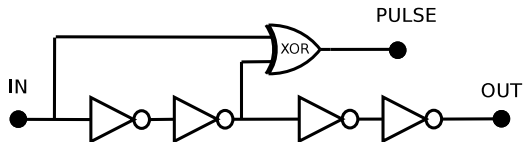

Fig. 3: Architecture selected to generate a pulse.

In order to have a first theoretical limit for the savings obtained while using the CS technique we can consider as if E_{SW} and E_{Log} were negligible. If this was the case, the savings would be determined by Eq. 4.

$$1 - \frac{E_{C1_{CS}} + E_{C2_{CS}}}{E_{C1} + E_{C2}} = \frac{2\gamma}{(1+\gamma)^2} \quad \text{where } \gamma = \frac{C2}{C1} \tag{4}$$

From Eq. 4 it can be seen that the maximum savings are limited to 50% and the two capacitances need to have the same value. As the value of the capacitances differ, the savings start to drop. For example, when $\gamma = 2$ the maximum savings drop to 44%.

However, E_{SW} and E_{Log} are not always negligible. E_{SW} was obtained the same way as in the classic implementation where the resistance and capacitance as a function of the width of the switches were extracted from simulation for a 130nm technology. The energy spent by the logic block (E_{Log}) was extracted from electrical simulations for different pulse widths. The sum of all the energy spent during a complete cycle of charge discharge will be referred as E_{Tot} and $E_{Tot_{CS}}$ for the case of a classic driving circuit and using charge sharing, respectively. Finally, the energy savings were calculated ($1-E_{Tot_{CS}}/E_{Tot}$) for different capacitances values (C1=C2=C) and T_{CD}. Figure 4 shows the savings obtained through this analysis. From the figure we can see that for small capacitances the savings start to drop. This is due to two reasons. Firstly, because the E_{Log} starts having a higher impact in the overall energy consumption of the driver. While E_{SW} and E_{C_i} (E_{C1}, E_{C2}, $E_{C1_{CS}}$, or $E_{C2_{CS}}$) scale down with C, E_{Log} remains the same. Secondly, because the minimum switch width is reached and E_{SW} also stops scaling with C which increases its impact in the total energy consumption.

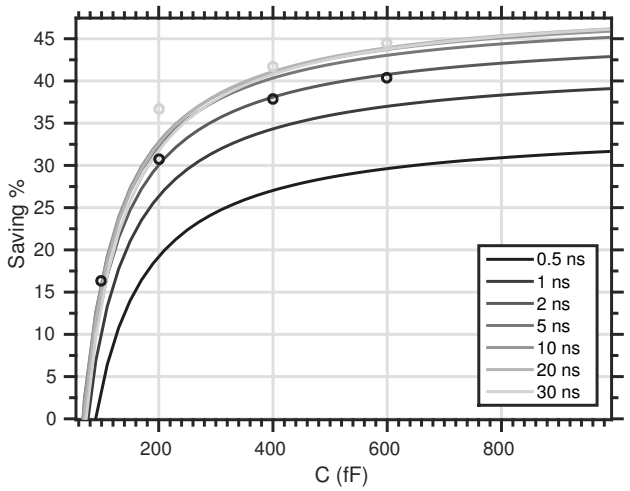

Fig. 4: Savings % vs C1=C2=C for different T_{CD}. The dots correspond to simulation results performed to those points.

On the other hand, when the capacitances value increase, E_{C_i} dominate and the savings tend to the theoretical limit. As can be seen, this is true when T_{CD} is not very demanding and the E_{SW} is negligible (e.g. $T_{CD} = 30ns$).

When T_{CD} is very demanding (e.g. $T_{CD} = 0.5ns$), the E_{SW} starts to be comparable with E_{C_i} which has an impact in the total energy and that is why the energy savings are less than for higher T_{CD}. This is true even if the E_{SW} was the same for both cases, with and without CS. However, E_{SW} is higher when CS technique is implemented mainly because it uses more switches.

Additionally, Fig. 4 shows the simulation results for some capacitances value and T_{CD}. These show that even though approximations were made in the analytical model, this keeps close to the simulation results. In conclusion, in this 130nm process significant savings can be obtained with capacitances higher than 300fF. In the next section we propose to take advantage of this technique to reduce the gate drive losses in SC DC-DC converters.

III. Switched-Capacitor DC-DC Converter

Gate drive losses can be very significant in SC DC-DC converters and reducing them has a direct impact in the converter efficiency. These converters generally operate in two phases (Phi1 and Phi2). Usually, one in which charge is taken from the power source and stored in the capacitors and a second phase were this charge is delivered to the load. Each phase is implemented using MOS switches which depending on the voltage applied to them, are either an nMOS or a pMOS switch.

When both nMOS and pMOS switches are used in the same phase, we have two capacitances where one needs to be charged at the same time that the other needs to be discharged. As it was shown in the previous section this is the necessary condition to use the CS technique.

In this work we present simulation results for a SC DC-DC converter designed in a 130nm technology. The architecture selected is a divide-by-three doubler topology shown in Fig. 5 [13]. It can be seen that, in this topology, when phase Phi1 is finished the gate capacitance of switch SW1 needs to be charged while the gates capacitances of SW2, SW5 and SW7 need to be discharged.

The converter was designed to deliver an output power of $400uW$ while dividing by three the input voltage ($1.2V$) and using a total capacitance of $1.2nF$. The design was obtained following the methodology proposed by [13] and selecting a target output voltage of $390mV$ and a ratio $C_{top}+C_{bottom}/C = 0.02$ where C is the total capacitance and C_{top}, C_{bottom} the parasitic top and bottom plate capacitances respectively. The switches width and its equivalent gate capacitances are shown in Table I.

In phase Phi1, the two capacitances that need to be charged and discharged are $430fF$ (SW1)(Vphi1p) and $800fF$ (SW2, SW5, SW7)(Vphi1n) while in phase Phi2 they are $570fF$ (SW3)(Vphi2p) and $510fF$ (SW4 and SW6)(Vphi2n).

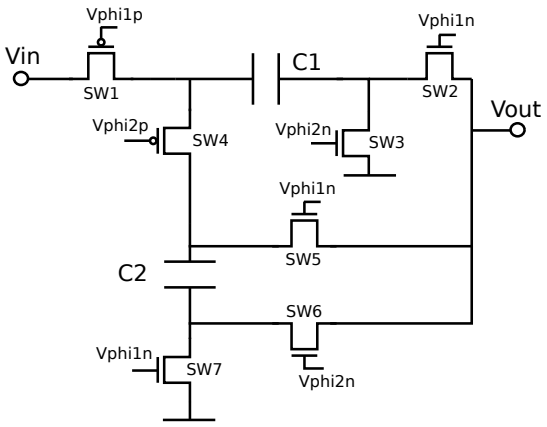

Fig. 5: SC DC-DC Converter Architecture.

TABLE I: SC DC-DC Converter design

Switch	SW1	SW2	SW3	SW4	SW5	SW6	SW7
WSW (μm)	403	270	211	527	270	270	211
CSW (fF)	430	287	225	570	287	287	225

Additionally the maximum converter frequency of operation is $28MHz$. As a consequence, the switches must be turned on at least 10 times faster than this frequency which corresponds to a T_{CD} of $4ns$.

If the CS technique is used in the driving of the switches in each phase, the analysis made in previous section predicts a saving equal to 38% and 42% for phase Phi1 and Phi2 respectively in comparison with a classic driving circuit.

In order to verify these predictions, the converter was simulated using a classic driver circuit and a driver using the CS technique. By using the proposed driver, a 40.5% energy saving was obtained in the gate drive losses of the converter. Depending on the desired output voltage, the relationship between the gate drive losses and the total losses changes and thus how much does the efficiency improve. The simulation results are presented in Fig 6. For example when the output voltage is $380mV$ the efficiency improves from 67.2% to 71.2% while using the CS technique.

IV. Conclusions

In this work we proposed a driving circuit for the switches of SC DC-DC converters that reduces the gate drive losses. In the particular design shown, these losses are reduced by a 40.5%, which can correspond up to 4% efficiency improvement. The proposed driving circuit can be used in any converter where nMOS and pMOS switches are used in the same phase of the converter (or any circuits with large complementary MOS switches).

We also presented a theoretical analysis to show when it is suitable to use the CS technique depending on the capacitances values and the time available for the charge/discharge process. The results show that for capacitances greater than 300fF the energy savings can be significant.

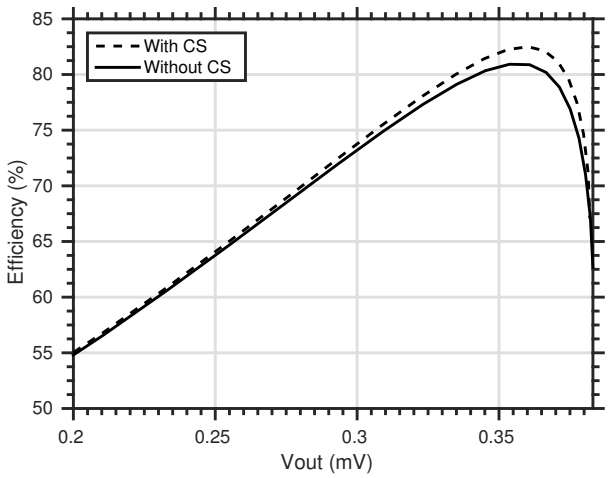

Fig. 6: SC DC-DC Converter Simulation Results. Efficiency vs Output Voltage. With CS (dashed line) and without CS (solid line).

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