Optimum NMOS/PMOS Imbalance for Energy Efficient Digital Circuits

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***Abstract*—In this work we propose an asymmetrical length biasing scheme to be used in advanced nanometer technologies that minimizes the energy per operation consumption of sub/near threshold digital CMOS circuits. Simulation results of two test circuits, a chain of inverters and a Ripple Carry Adder, show that by using this sizing approach, the energy per operation can be reduced in more than 50% in a wide range of target performances. We use a 28nm UTBB FDSOI technology and we show that the combination of supply voltage scaling, back plane biasing and length biasing can be combined to obtain extremely robust (variability is almost halved) and energy efficient digital circuits. We also show simulation results for Predictive Technology Models to show that the technique is also compatible with conventional bulk technologies.**

***Index Terms*—Low Energy, Sub threshold Digital Circuits, Asymmetric Length Biasing, Poly Biasing, NMOS/PMOS Imbalance, Minimum Energy Point**

I. Introduction

The demand of portable devices and the continuous trend towards the Internet of Things (IoT) have made of energy consumption one of the main concerns in the industry and researchers. The most efficient way of reducing the energy consumption of digital circuits is decreasing the supply voltage (V_{DD}) since the dynamic energy quadratically depends on V_{DD}.

However, lowering V_{DD} also impacts the speed of the circuit, making it slower. This increase in the delay increases the leakage energy consumed during a specific operation, because, although the leak power can be reduced due to the decrease in V_{DD}, the energy increases as the power is consumed in a much longer period of time. These opposite trends give rise to an optimal V_{DD}, usually in the sub/near threshold region, where energy per operation is minimized [1], [2]. This point is usually known as the minimum energy point (MEP).

In the beginning of this century, this region of operation was proposed for very low speed ultra low power applications because the performance achieved in the MEP was very low, in the order of the kHz [1]–[5]. However, the advanced nanometer technologies bring new opportunities since the performances obtained in the MEP can cover a much wider range of applications from the kHz to some tens of MHz. The main drawback of advanced technologies is that the variability is worsened and this has a great impact in sub threshold circuits because the drain current exponentially depends on the threshold voltage, supply voltage and temperature [6]–[8]. In [9], [10] the authors present the main challenges of using advanced technologies for sub threshold digital circuits and try to answer the question of whether they are beneficial or not.

In particular, FD-SOI technology has emerged as a solution to attain digital circuits with high energy efficiency, mainly due to the high sub threshold slope and reduced parasitic capacitance [11]–[14]. The variability is greatly decreased, in comparison with bulk technology, since a lightly doped body is used, which makes it suitable for ultra low voltage circuits [15]–[17]. Moreover, the solution proposed by [18] for multi threshold voltage (V_T) transistors in the so called Ultra Thin Body and Box (UTBB) FD-SOI, opens a new degree of freedom by allowing an ultra wide range of back plane biasing (BB) voltage which can be used for fine tuning of the transistor's V_T.

In [19], the authors present one of the first models for the energy per operation consumption near the MEP. Based on the exponential dependence of the drain current in the sub threshold region, a very simple model is derived which provides insight into the dependences of the energy consumption. They show an analytical expression for the optimum V_{DD} and the total energy per operation as it can be seen in Eq. (1). C_{eff} is the effective capacitance of the circuit. W_{eff} is the effective width, relative to the characteristic inverter, that contributes to leakage. K is a delay fitting parameter. C_g the output capacitance of the characteristic inverter. L_{DP} the logic depth of the circuit. U_T is the thermal voltage and n the sub threshold slope.

$$E_T = V_{DD}^2(C_{eff} + W_{eff}KC_gL_{DP}e^{\frac{-V_{DD}}{nU_T}}) \qquad (1)$$

Equation (1) shows that when considering this simple model the energy per cycle is independent of the V_T of the transistor, which means that theoretically by tunning the V_T of the transistor, different performances can be obtained while consuming the same energy. However, this is not the practical case, mainly due to two reasons. Firstly, as it was deeply studied in [20], using different technology flavors (for example general purpose or low power devices) or global V_T selection available in the process (most nanometer technologies have two V_T devices in each flavor), has an impact on other characteristic of the device like capacitance or sub threshold slope that change the minimum energy achieved. The authors also show that using body biasing to change the V_T of the

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device has a negative influence in the energy consumption due to the same reason.

The second reason is that in this model, the same V_T and n value is considered for both nMOS and pMOS transistors. In consequence, the impact of the difference in these parameters is not taken into account. In [21]–[24] it was shown that the imbalance between the nMOS and pMOS transistor's leakage currents has an impact in the leakage energy consumed by the circuit. We present a simple model that takes into account the differences between the nMOS and pMOS transistors and we show that there is an optimum imbalance that minimizes the total energy [24]. We also show that this optimum depends on the circuit topology and the circuit's inputs.

In this work we propose a new sizing approach for logic gates with an asymmetric length biasing that makes the circuit operate in the optimum imbalance of the leakage current [25]. We compare this sizing approach with classic sizing approaches to show that great energy reductions can be obtained for the same performance. We used a FD SOI 28nm technology but we also present simulation results with Predictive Technology Models [26] to show that this technique can be applied in conventional bulk technologies as well.

This paper is organized as follows. Section II develops a simple model for the minimum energy per operation which shows the existence of the optimum imbalance. Then, Section III presents the tests circuits considered to validate the proposed sizing approach. Afterwards, Section IV focuses on the simulation results and a comparison with other sizing approaches. Further on Section V presents how to use an asymmetric back plane biasing to make the circuits work in the optimum imbalance and compare this technique with the asymmetric length biasing that we are proposing. The dependence on circuit's inputs in a Ripple Carry adder is addressed in Section VI. Finally, conclusions are drawn in Section VII.

II. Minimum Energy Point Model

In this section we show a simple model for the total energy per operation consumed by CMOS digital circuits operating near the MEP. We use a transistor model valid for sub threshold operation (weak inversion region) since in general the MEP is achieved in this region. Additionally, we take into account the differences between the nMOS and the pMOS transistors and we show that these differences have an important impact in the MEP.

Equation (2) shows the conventional model for the sub threshold current where I_L was conveniently defined as the OFF current of the transistor. In this case, n stands for the sub threshold slope factor, V_T the threshold voltage and U_T the thermal voltage. In each case with a n or p subindex it is indicated if the parameter corresponds to a nMOS or pMOS transistor.

$$\begin{aligned} I_{sub,n(p)} &= I_{o,n(p)} e^{\frac{V_{GS(SG)} - V_{Tn(p)}}{n_{n(p)} U_T}} \\ &= I_{L,n(p)} e^{\frac{V_{GS(SG)}}{n_{n(p)} U_T}} \end{aligned} \tag{2}$$

We use a basic model for the delay of a gate which is shown in Eq. (3). Here C_g is the output capacitance of the gate and K is a fitting parameter.

$$t_d = \frac{K C_g V_{DD}}{I_{sub}\big|_{V_{GS}=V_{DD}}} = \frac{K C_g V_{DD}}{I_{L,n(p)}} e^{\frac{-V_{DD}}{n_{n(p)} U_T}} \tag{3}$$

The dynamic energy consumed by the circuit per operation can be calculated with Eq. (4), where C_{eff} is the effective capacitance switched during the operation and in consequence it takes into account the activity factor of the circuit.

$$E_D = V_{DD}^2 C_{eff} \tag{4}$$

As for the leakage energy, we include in our model the differences between the nMOS and pMOS transistors. Equation (5) shows the proposed model for the leakage energy. $W_{effn(p)}$ is an estimation of the average width of nMOS (pMOS) transistors, relative to the characteristic inverter, that contribute to leakage. $\tau_{n(p)}$ is the number of inverter's delay in the critical path that depend on a nMOS (pMOS) transistor. $W_{effn(p)}$ depends on which transistor (nMOS or pMOS) defines the leakage current. This depends on the circuit architecture and on the value at the inputs. Similar is the case of $\tau_{n(p)}$, which depends on how many node transitions are driven by an nMOS (pMOS). Therefore these values depend on the circuit architecture as well as on the inputs values. Nevertheless, in Section VI is discussed the impact of changes in the inputs, showing that the proposed technique provides clearly advantageous results.

$$E_L = V_{DD}(W_{effn} I_{L,n} + W_{effp} I_{L,p})(\tau_n t_{d,n} + \tau_p t_{d,p}) \tag{5}$$

If we consider that the sub threshold slope factors of both transistors are similar, $n \approx n_p \approx n_n$, and using Eq. (3) and Eq. (5), the leakage energy can be written as in Eq. (6). Equation 5 depends on the total leakage current and the total delay of the circuit. Each of these (total leakage current and the total delay), has two terms, one that depends on the nMOS parameters and the other in the pMOS parameters. In particularly, the leakage current terms they are obviously directly proportional to the leakage current of each transistor while the delay terms are inversely proportional to the leakage current of each transistor. LF in Eq. (6) reflects these dependences in the multiplication of the total leakage current and the total delay in the leakage energy, Eq. (5).

$$E_L = V_{DD}^2 K C_g e^{\frac{-V_{DD}}{n U_T}} LF$$

where

$$\begin{aligned} LF = \tau_n W_{effn} + \tau_p W_{effp} + \tau_n W_{effp} \frac{I_{L,p}}{I_{L,n}} + \\ \tau_p W_{effn} \frac{I_{L,n}}{I_{L,p}} \end{aligned} \tag{6}$$

The model of Eq. (5) and Eq. (6) is an extension of the simple model applied for analysis of the MEP in several works, e.g. [2], [19], [21]. Here, the model includes the impact of the different leakage components due to the pMOS and nMOS leakage paths.

Therefore, the total energy can be obtained adding Eq. (6) and Eq. (4). Furthermore, the optimum V_{DD} that minimizes the total energy per operation can be obtained by calculating

the derivative of the total energy (Eq. (7)) and equalizing to zero.

$$\frac{\partial E_T}{\partial V_{DD}} = 2V_{DD}C_{eff} + 2V_{DD}LFC_gKe^{\frac{-V_{DD}}{nU_T}} + \frac{-V_{DD}^2LFC_gK}{nU_T}e^{\frac{-V_{DD}}{nU_T}} \quad (7)$$

Equation (8) shows the optimum V_{DD} that minimizes the total energy, where $lambertW$ is the Lambert function which gives the solution to $xe^x = \beta$.

$$V_{DD_{opt}} = nU_T(2 - lambertW(\beta)) \qquad \beta = \frac{-2C_{eff}}{LFC_gK}e^2 \quad (8)$$

From Eq. (6) and Eq. (4) we can see that the total energy depends on the imbalance between the nMOS and pMOS leakage currents represented in the equation by $I_{L,n}/I_{L,p}$. In order to find the optimum imbalance that minimizes the total energy per operation LF must be minimized [24]. Equation (9) shows the derivative of the total energy with respect to the imbalance and Eq. (10) shows the optimum imbalance.

$$\frac{\partial E_T}{\partial \frac{I_{L,n}}{I_{L,p}}} = KC_ge^{\frac{-V_{DD}}{nU_T}}\left(W_{effn}\tau_p - W_{effp}\tau_n\frac{1}{(\frac{I_{L,n}}{I_{L,p}})^2}\right) \quad (9)$$

$$\left(\frac{I_{L,n}}{I_{L,p}}\right)_{opt} = \sqrt{\frac{W_{effp}\tau_n}{W_{effn}\tau_p}} \quad (10)$$

The optimum imbalance depends on the architecture and the state of the circuit through W_{eff} and τ. Additionally, it is easy to see that if we want to consider the differences between the sub threshold slope of each device, the new optimum imbalance can be calculated by Eq. (11). Further on we will discuss when is important to consider this difference.

$$\left(\frac{I_{L,n}}{I_{L,p}}\right)_{opt} = \sqrt{\frac{W_{effp}\tau_n}{W_{effn}\tau_p}e^{\frac{V_{DD}}{U_T}(\frac{1}{n_p}-\frac{1}{n_n})}} \quad (11)$$

III. Test Circuits

We used a 28 nm UTBB FD-SOI technology which has two V_T flavors. A regular V_T transistor (RVT) where the back planes are implemented with conventionally doped wells (p-well for the nMOS and n-well for the pMOS) and low V_T transistors (LVT) where the wells are flipped [13].

The first test circuit (Test Circuit 1) is an inverter chain, which is a simple circuit, yet representative of the performance trade-offs of more complex circuits. It was chosen a 25 inverter chain with an activity factor of 0.1 (i.e ten 25 inverter chain, one switching with just in time operation frequency and the other nine with a fixed input) (Fig. 1). If it is not specified otherwise, the devices used were LVT. This circuit is used in Section IV and Section V to evaluate the benefits of the proposed technique.

The second test circuit (Test Circuit 2) is an 8-Bit Ripple Carry Adder, which is a commonly used block representative of medium sized combinatorial blocks. This circuit was used to confirm the benefits of asymmetric length biasing and to show the impact of the different inputs in the optimum imbalance. These results are shown in Section VI.

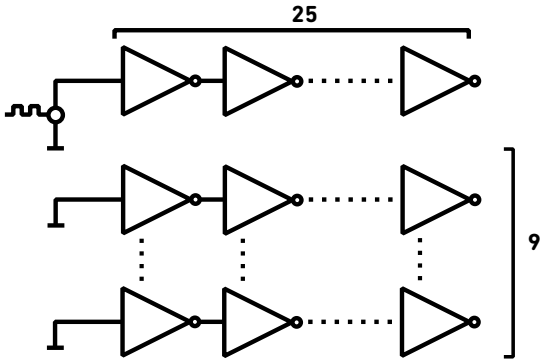


Fig. 1. Test Circuit 1. Chain of inverters with an activity factor of 0.1.

IV. Asymmetric Length Biasing

Length biasing was proposed as a knob to mitigate several disadvantages of advanced nanometers technologies, specially for sub threshold digital circuits [9], [12]. In [9], the authors show how an increase in the length of the devices can improve the sub threshold slope and the DIBL coefficient. Figure 2 shows the sub threshold slope factor n as a function of the length for the nMOS LVT device of the technology used.

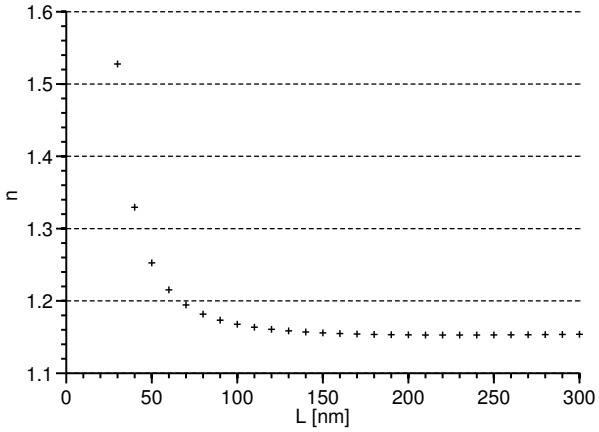


Fig. 2. nMOS LVT sub threshold slope factor as a function of transistor's length.

Additionally, in [9] it is shown that in the sub threshold regime and for advanced technologies the output capacitance of the digital gates is mostly dominated by fringing capacitances which are almost independent on the transistor's length. This is why a moderate increase in the length of the devices has little impact on the dynamic energy consumption. Finally, the impact in the overall cell area of a moderate increase in the length of the devices is very small due to the almost negligible contribution of the active area to the total area.

In this work we propose to use an asymmetric length biasing (ALB) to achieve the optimum imbalance for leakage currents that minimizes the leakage energy, as shown in the previous section. Figure 3 shows the simulation results for the energy per operation (black solid contour lines) of the first test circuit as a function of V_{DD} and the length of the nMOS devices (Ln). In this case the length of the pMOS was maintained at the minimum size, leading the leakage current of the pMOS

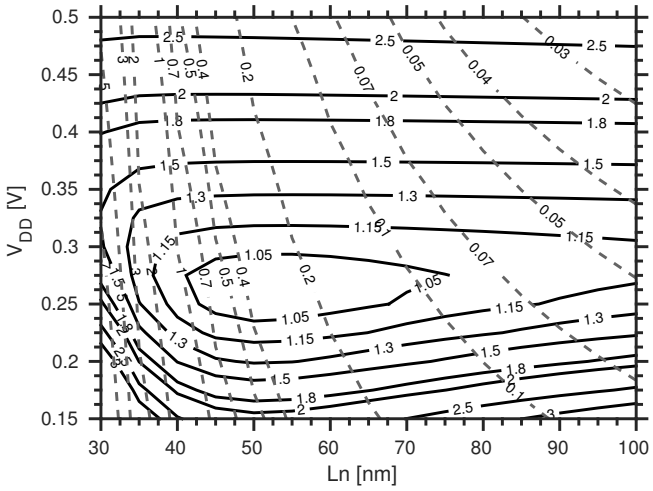


Fig. 3. Asymmetric Length Biasing (ALB). Energy per operation (solid black lines) normalized to the minimum energy and leakage current imbalance ($I_{L,n}/I_{L,p}$) (dashed grey lines) as a function of V_{DD} and Ln (length of nMOS). LVT devices. $Lp = 30nm$. $Wp = Wn = 80nm$. Test circuit 1.

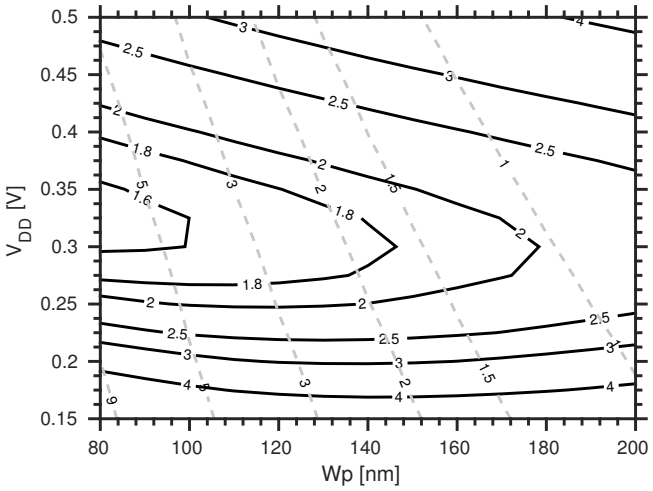


Fig. 4. Energy per operation (solid black lines) normalized to the minimum energy achieved with ALB and leakage current imbalance ($I_{L,n}/I_{L,p}$) (dashed grey lines) as a function of V_{DD} and Wp (width of pMOS). LVT devices. $Lp = Ln = 30nm$. $Wn = 80n$. Test circuit 1.

devices to be fixed. Then, by changing L_n we vary the leakage current of the nMOS device and we can adjust the leakage currents imbalance to the optimum shown in Eq. (10).

The energy contours shown in Fig. 3 are normalized to the minimum energy achieved. This minimum energy is achieved at a $V_{DD} = 250mV$ and a $Ln = 50nm$. In the classic symmetric case, with $Ln = Lp = 30nm$, the minimum energy per operation is achieved at a $V_{DD} = 325mV$ and it consumes 50% more energy than the optimum asymmetric case as it is shown in Fig. 3.

Additionally, Fig. 3 also shows the leakage imbalance between the nMOS and pMOS (dashed grey contour lines) as a function of V_{DD} and the length of the nMOS devices (Ln). The optimum imbalance is near 0.4. In this simple test circuit, it is easy to see that $W_{effp} \approx W_{effn}$ and $\tau_p \approx \tau_n$. However, since we have an upsized L_n, the sub threshold slope of the nMOS is different from the pMOS, which makes the optimum imbalance move from 1 (See Fig. 2 and Eq. (11)).

Another approach would be to use the width of the pMOS device to adjust the imbalance between the leakage currents of the two devices. This is the classic approach while designing above threshold standard cells to equalize rise and fall times. However, the increase in the width of the devices has a high impact in the output capacitance of the gates.

Figure 4 shows the same energy per operation and leakage imbalance contours as Fig. 3 but as a function of the width of the pMOS device (Wp). The energy is normalized to the energy obtained with the optimum ALB from Fig. 3. We can see that although the imbalance moves towards the optimum, the energy per operation does not decrease. This is because the dynamic energy increases due to the increase in the output capacitance of the gates. This is why the classic sizing approach for above threshold digital gates is not appropriate for sub threshold design.

The energy reduction obtained with ALB is due to three factors. First, as it was shown with the model presented in Section II, we are working in the optimum imbalance between the leakage currents and thus reducing the leakage energy. Additionally, increasing the length of the nMOS devices improves the sub threshold slope which also reduces the leakage energy (See Eq. (6)). Finally, these two factors reduce the optimum V_{DD} (See Eq. (8)) and in consequence this reduces the dynamic energy consumed.

Asymmetric Length Biasing with back plane biasing

The comparison made between ALB and the classic minimum sizing is not a totally fair comparison since the performance achieved in both cases are different. In order to evaluate the energy reductions of ALB at the same performance, we used the unique body biasing opportunities available in this technology for threshold voltage tunning.

The back plane voltage is electrically isolated from the source and drain of the devices so the voltage range is only limited by the diode between the different wells used for the nMOS and pMOS back planes. This allows to fine tune the threshold voltages of the devices to achieve the desired performance. For example, in LVT devices the back plane voltage can be used to reduce the V_T of the devices in a wide range. Due to the dopping type of the back plane, these voltages (V_{BPn} and V_{BPp}) are usually used considering $V_{BPn} = -V_{BPp} = VB$.

Figure 5 shows the energy per operation contour (solid black lines) as a function of V_{DD} and the back plane voltage (VB) for the two cases, with the minimum size devices ($Ln = Lp = 30nm$) and with the ALB ($Ln = 50nm$ and $Lp = 30nm$). The energy per operation is normalized to the minimum energy achieved with $Ln = 50nm$ and $Lp = 30nm$. We also show performance contours (dashed grey lines) in order to compare the energy reductions obtained with ALB at the same performance. These values are in MHz.

From Fig. 5 we can see the energy reduction obtained with ALB jointly with the expected performance. For example,

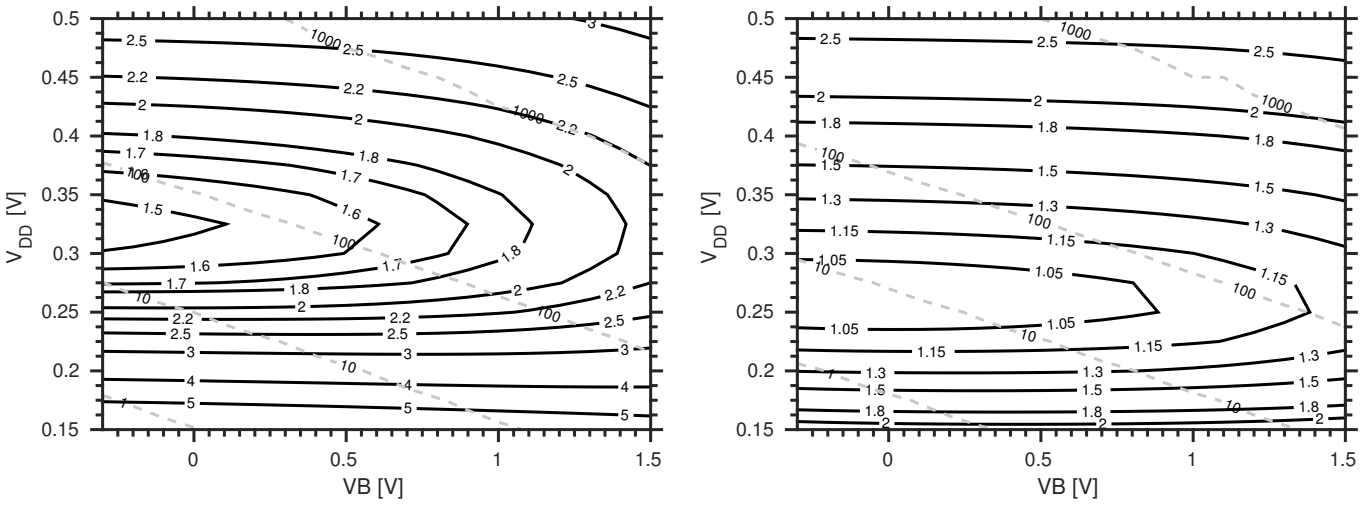


Fig. 5. Symmetrical Minimum Sizing vs ALB. Energy per operation (solid black lines) normalized to the minimum energy achieved with ALB (Fig. 3) and performance contours (dashed grey lines) (in MHz) as a function of supply voltage and back plane voltage. LVT devices. a) $Ln = Lp = 30nm$ b) $Ln = 50nm$ $Lp = 30nm$ Test circuit 1.

for low performances (1 MHz), the energy obtained with symmetric lengths can be up to 4 times higher than with an ALB. As performance requirements increase, the energy benefits obtained by ALB decrease. Nevertheless, for example, at 10 MHz and 100 MHz the energy consumed with symmetric lengths is 70% and 35% higher than in the ALB case. The energy savings depend on the ratio between the leakage energy and the total energy. For very low performance the total energy is almost all due to leakage energy while for high performance the total energy is almost all dynamic. Since the ALB reduces the leakage energy, the benefits are higher when targeting lower performances. This shows that there is a very wide range of applications that can benefit from ALB.

Finally, we can implement the ALB, but with an upsized length for the pMOS. This improves the sub threshold slope factor reducing even more the energy per operation consumption. Figure 6b shows the energy per operation and performance contours as presented before but for $Ln = 110nm$ and $Lp = 40nm$. In this case, the total energy consumption can be further reduced in a wide range of target performances but the increase in dynamic energy makes the circuit consume more total energy in high performance scenarios. Additionally, Fig. 6a shows the energy per operation and performance contours as presented before but for a symmetric length biasing $Ln = 50nm$ and $Lp = 50nm$. In these last two cases the energy contours are normalized to the minimum energy achieved in Fig. 5b. It can be noted that if a symmetric upsized approach is used the energy consumption is still higher than the ALB case with minimum Lp because the circuit is not working in the optimum imbalance.

In summary, we showed that by using ALB, very significant energy reductions can be achieved while maintaining the same performance.

Variability in Asymmetric Length Biasing

Another important concern while building sub threshold digital circuits with advanced nanometers technologies is the variability. This is because the drain current of the transistors depends exponentially on the threshold voltage, supply voltage and temperature. In order to assess the impact of ALB in the variability of the circuit, we performed 1000 Monte Carlo simulations of mismatch and process for the energy per operation with each of the sizing approaches discussed in the last section.

Table I shows the Monte Carlo results for each sizing approach. It points out the supply voltage, the mean energy per operation and the standard deviation obtained from simulation.

TABLE I
MONTE CARLO SIMULATION RESULTS

Size	V_{DD} [V]	Mean Ene/Op [aJ]	Std Dev [aJ]	Std Dev/Mean
$Ln = 30nm$ [1] $Lp = 30nm$	0.325	629	77.2	0.12
$Ln = 50nm$ [2] $Lp = 30nm$	0.250	449	54.0	0.12
$Ln = 50nm$ [3] $Lp = 50nm$	0.300	494	73.6	0.15
$Ln = 110nm$ [4] $Lp = 40nm$	0.225	343	31.7	0.092
$Ln = 30nm$ [5] $Lp = 30nm$	0.300	689	116.6	0.17
$Ln = 50nm$ [6] $Lp = 30nm$	0.300	419	28.2	0.067
$Ln = 110nm$ [7] $Lp = 40nm$	0.300	355	13.2	0.037

[1] Symmetric Length @ V_{DD} of MEP
[2] Asymmetric Length Biasing @ V_{DD} of MEP
[3] Upsized Symmetric Length Biasing @ V_{DD} of MEP
[4] Upsized Asymmetric Length Biasing @ V_{DD} of MEP
[5] Symmetric Length Biasing @ V_{DD_3}
[6] Asymmetric Length Biasing @ V_{DD_3}
[7] Upsized Asymmetric Length Biasing @ V_{DD_3}

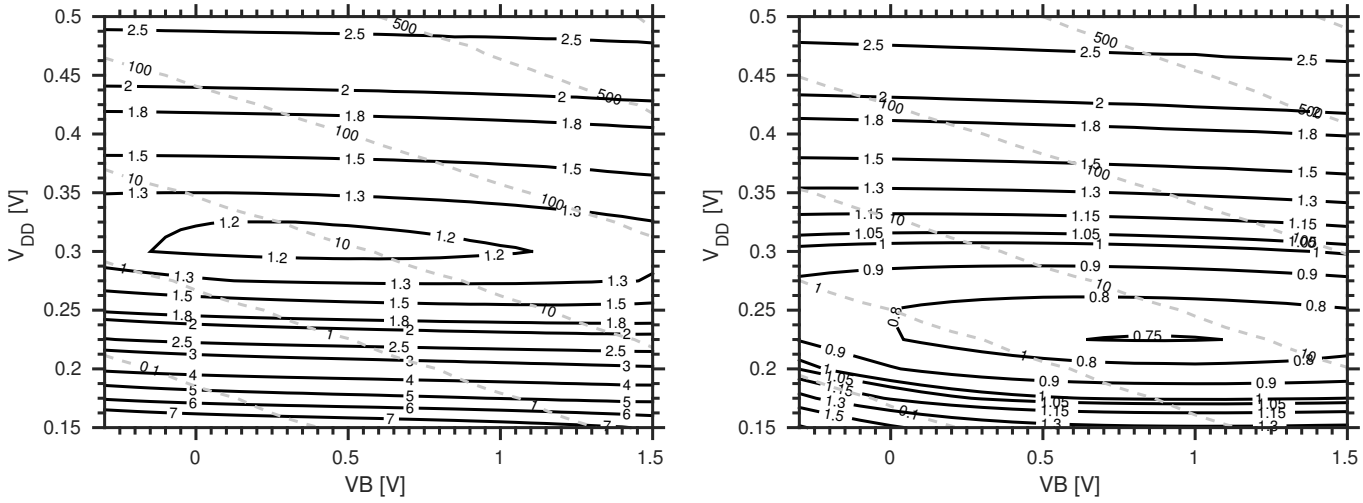


Fig. 6. Symmetrical Upsizing vs ALB Upsizing. Energy per operation (solid black lines) normalized the minimum energy achieved with ALB (Fig. 3) and performance contours (dashed grey lines) (in MHz) as a function of supply voltage and back plane voltage. LVT devices. a) $Ln = Lp = 50nm$ b) $Ln = 110nm$ $Lp = 40nm$ Test circuit 1.

For each sizing approach the simulation results are shown with the optimum V_{DD}. Additionally, in some cases an increased V_{DD} is also shown. We can see that ALB significantly improves the variability, particularly when the optimum V_{DD} considering variability [8] is used, i.e. case 6 and 7 compared to case 1 and 3 of Table I. This is due to two reasons. The first one is that the upsized length reduces the variability of the devices since the active area is bigger. This is achieved with very little total area penalty. The second reason is that because with ALB we are working at optimum imbalance that minimizes the energy, small variations in the imbalance have little impact in the energy consumption. This is related to the fact that we are considering variations around a local minimum which in 6b can be seen that it has a wide flat area around it.

Temperature dependence in Asymmetric Length Biasing

Since we are working in the sub threshold regime, temperature dependence is stronger due to the exponential dependence on the drain current of the devices. However, here we show that the optimum length is not strongly affected by temperature. The optimum length directly depends on the optimum imbalance which depends with temperature through the thermal voltage, as shown in Eq. 11. From Eq. 11 we can note that how much does the temperature impacts in the optimum imbalance depends on the difference between the sub threshold slopes of the nMOS and pMOS devices and the supply voltage. To assess this impact, we did the same simulation as in Fig. 3 for different temperatures, the results are shown in Fig. 7. We can see that, even in the extreme cases of 125 °C and -40 °C, the optimum length is not significantly changed. If we select the optimum for room temperature ($L_n = 50nm$) the savings obtained with ALB are almost the same for all the industrial temperature range.

Asymmetric Length Biasing in bulk technologies

It is important to notice that this technique can be applied in conventional bulk technologies. In order to have a first glance of the benefits that can be achieved in these technologies, we simulated the same test circuit with Predictive Technology Models [26] from 90nm down to 32nm node.

Table II shows the simulation results for each node. This includes the Ln min, the Ln optimum (that minimizes the energy per operation), the energy per operation in each case

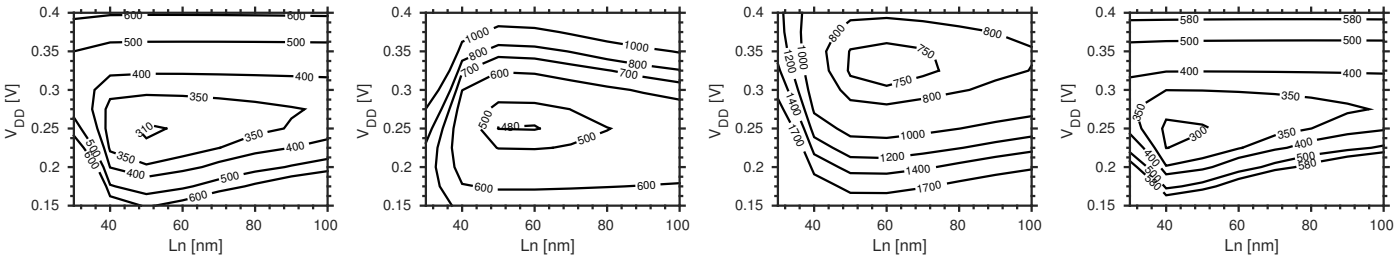


Fig. 7. Energy contours [aJ] as a function of V_{DD} and the length of the nMOS (Ln) for different temperatures. $V_{BPp} = V_{BPn} = 0V$. LVT

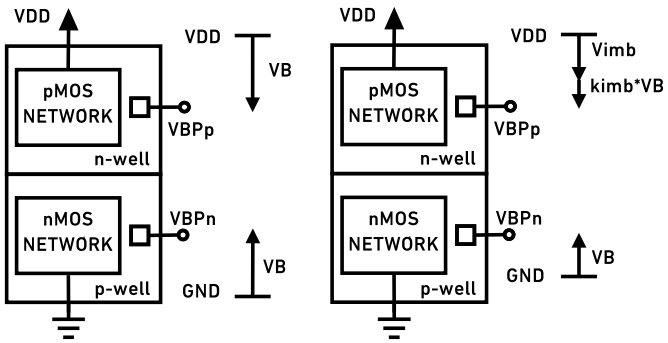
TABLE II
PTM SIMULATION RESULTS

Node	Ln min [nm]	Ln op [nm]	Wn=Wp [nm]	Ene/Op @Ln min [fJ]	Ene/Op @Ln op [fJ]	Ene/Op @Ln min/Ene/Op @Ln min
90 nm	90	120	135	1.139	1.039	1.0962
65 nm	65	85	100	0.8852	0.7571	1.1692
45 nm	45	61	67	0.6347	0.5201	1.2203
32 nm	32	42	48	0.4350	0.3816	1.3279

and finally the relationship between these two energies. The Lp was maintained at the minimum. We can see that as we move to a more advanced technology node, the savings obtained with ALB increase. This is in agreement with the discussion given for the dominant output gate capacitances. As the technology node decreases, the fringing capacitances are more dominant in the output capacitances of the digital gates and thus the increase in the length to achieve the optimum imbalance has less impact in dynamic energy.

V. ASYMMETRIC BACK PLANE BIASING

In this section we present another alternative that could be considered to make the circuits work in the optimum imbalance. Currently, the application of back plane biasing (BB) in digital circuits has been proposed to manage the trade-off between leakage current and performance [13], [27], [28]. Lined with this approach, either both the pMOS and nMOS are symmetrically forward biased (FBB) or reverse biased (RBB). We will call this approach the classic symmetric back plane biasing scheme (SBB). Figure 8a and Eq. (12) summarize the classic symmetric back plane voltage scheme for RVT devices.



(a) Classic symmetric back plane biasing scheme. FBB for $VB > 0$, RBB for $VB < 0$.

(b) Optimum back plane biasing scheme.

Fig. 8. Back plane biasing schemes.

$$V_{BPp} - V_{DD} = -V_{BPn} \tag{12}$$

On the other hand, in [24] we used the unique feature of the UTBB FD SOI process, the wide range of BB to adjust the V_T of the nMOS and pMOS transistors, to work with the optimum imbalance shown by Eq. (10). To tune the V_T properly we needed to find a relationship between the back plane voltage and the imbalance. Equation 13, which is derived from Eq. (2), shows the relationship between the imbalance and the transistor's threshold voltage while Eq. (14) shows the model used for the V_T modulation through the back plane voltage.

$$\frac{I_{L,n}}{I_{L,p}} = \frac{I_{o,n}}{I_{o,p}} e^{\frac{-V_{Tn}}{n_n U_T} + \frac{V_{Tp}}{n_p U_T}} \tag{13}$$

$$V_T = V_{T0} - \gamma V_{BS} - \eta V_{DS} \tag{14}$$

With these two relationships we can find the optimum back plane biasing (OBB) scheme that maintains the imbalance constant, in the optimum, while the V_T is tuned to adjust the performance of the circuit. Equation 15, derived from Eq. (13) and Eq. (14), shows the relationship that must satisfy the V_{BPn} and V_{BPp} in order to maintain a constant imbalance. Figure 8b and Eq. (15) summarize the optimum back plane voltage scheme.

$$V_{BPp} - V_{DD} = -k_{imb} V_{BPn} - V_{imb}$$

where

$$k_{imb} = \frac{\gamma_n n_p}{\gamma_p n_n}$$

and

$$V_{imb} = \frac{V_{T0n} n_p - V_{T0p} n_n}{\gamma_p n_n} + V_{DD} \frac{\eta_p n_n - \eta_n n_p}{\gamma_p n_n} + \frac{n_n n_p}{\gamma_p n_n} U_T ln\left(\frac{I_{Lp} I_{on}}{I_{Ln} I_{op}}\right) \tag{15}$$

To evaluate the energy reductions obtained by optimum back plane biasing and compare them with the ones obtained by asymmetric length biasing we simulated the same test circuit but with the OBB explained above. In this case we show the OBB scheme with symmetric length biasing, $Lp = Ln = 50nm$. Figure 9 shows the energy per operation as a function of V_{DD} and V_{BPp} while the $V_{BPn} = 0V$. The energy is normalized to the minimum energy achived with the ALB of Fig. 3.

From the simulation result we can see that with the OBB scheme the energy can be reduced almost the same as in the upsized ALB (Fig. 6b). This is because the OBB with upsized devices benefits from the improvements of length biasing as well. Additionally, the upsized ALB still not affects the output capacitance of the gates which does not increase the dynamic energy.

However, the main disadvantage of the OBB is that all the black plane voltage range is used to achieve the optimum imbalance. In consequence, the only knob available to adjust performance is the V_{DD} which has an important impact in

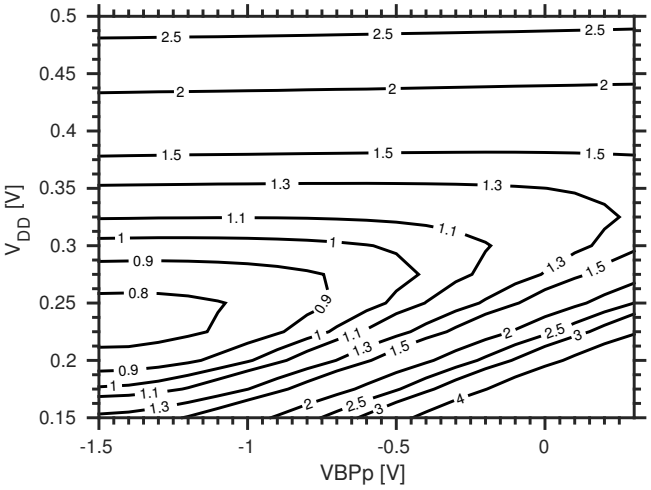


Fig. 9. Optimum Back Plane Biasing (OBB). Energy per operation (solid black lines) normalized to the minimum energy achieved with ALB (Fig. 3) as a function of V_{DD} and V_{BPp}. LVT devices. $Lp = Ln = 50nm$. $Wp = Wn = 80n$. $V_{BPn} = 0V$. Test Circuit 1.

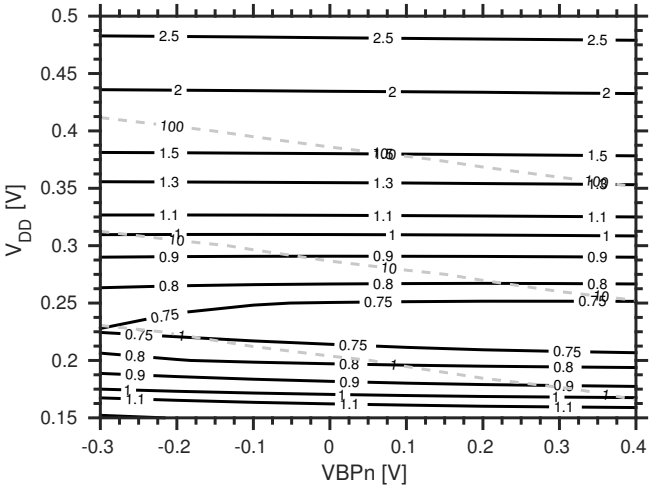


Fig. 11. Joined application of OBB and ALB. Energy per operation (solid black lines) normalized the minimum energy achieved with ALB (Fig. 3) and performance contours (dashed grey lines) (in MHz) as a function of V_{DD} and V_{BPn}. LVT devices. $Lp = 50nm$ $Ln = 65nm$. $Wp = Wn = 80n$. V_{BPp} according to Fig. 8b and Eq. (15). Test Circuit 1.

the energy consumption. To see this we simulated the OBB scheme based on Eq. (15), the results are shown in Fig. 10.

Finally, an hybrid approach between OBB and ALB can be used to have the maximum benefits from each technique. To do this, the optimum imbalance is partially achieved by ALB and OBB. Figure 11 shows the energy per operation with the OBB and with an asymmetric length biasing of $Ln = 65nm$ and $Lp = 50nm$. The simulation results show that with this hybrid approach we can obtain the minimum energy when targeting some performances, for example 1MHz. In conclusion, by using asymmetric length biasing and/or asymmetric back plane biasing, extremely robust and energy efficient digital circuits can be achieved.

As a general guideline in order to use the optimum ALB or OBB scheme, we need to take the following steps. First, we need to obtain the optimum imbalance that minimizes the energy consumption. To do this we need to find the parameters of Eq. (11). W_{effp}, W_{effn}, τ_p and τ_n can be obtained from a logic simulation of the circuit and need to take into account the inputs probabilities.

Second, the dependence of the sub threshold slope with the length and the back plane voltage of the devices needs to be studied in order to see if Eq. (10) or Eq. (11) is more suitable. With this, the optimum imbalance can be obtained.

Finally, electrical simulations of one nMOS and one pMOS device must be done in order to obtain which lengths and back plane voltages must be used to achieve the optimum imbalance. Depending on the application and how much the optimum imbalance changes, is how the techniques might be combined since the OBB can be done dynamically while the ALB is fixed.

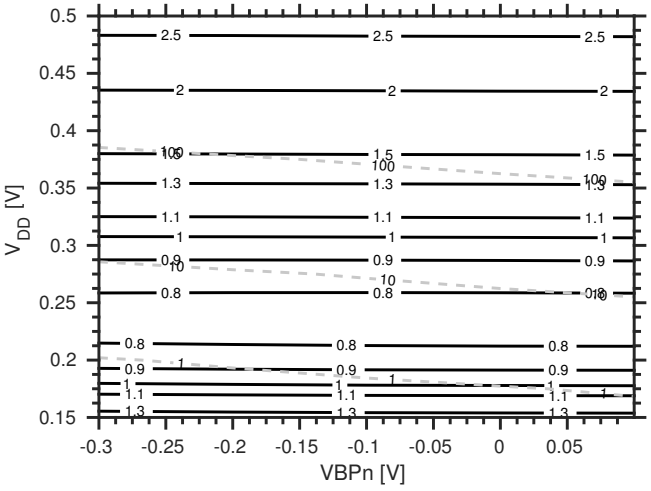


Fig. 10. OBB and performance. Energy per operation (solid black lines) normalized the minimum energy achieved with ALB (Fig. 3) and performance contours (dashed grey lines) (in MHz) as a function of V_{DD} and V_{BPn}. LVT devices. $Lp = Ln = 50nm$. $Wp = Wn = 80n$. V_{BPp} according to Fig. 8b and Eq. (15). Test Circuit 1.

VI. RCA Adder Simulations

In order to confirm the benefits of asymmetric length biasing we simulated an 8-Bit Ripple Carry Adder (RCA).

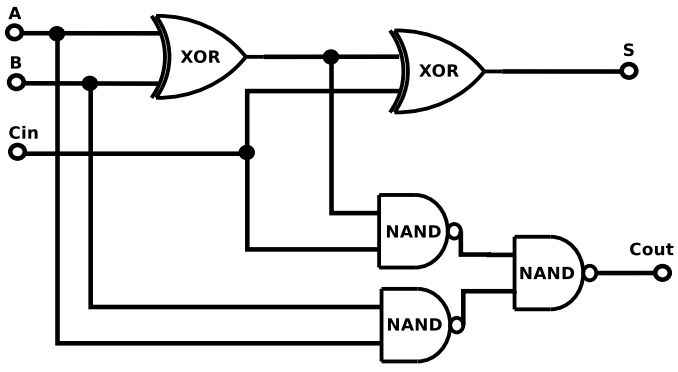


Fig. 12. Architecture of 1-bit section of the full adder. Test Circuit 2.

The architecture selected for the full adder is shown in Fig. 12.

In Section II we presented a model for the energy per operation consumed by digital circuits working near the minimum energy point and we saw that the optimum imbalance between the leakage currents of the nMOS and pMOS that minimizes the energy consumption, depends on the architecture and the inputs of the circuit. In particular, we want to evaluate how much does the optimum imbalance change for different inputs in a RCA. More important, we want to see if the energy benefits obtained by ALB are achieved with different inputs.

In order to answer these questions, we simulated an 8-bit RCA where each gate was built with minimum widths ($Wn = Wn = 80nm$) and minimum length for the pMOS ($Lp = 30nm$). Then we simulated the energy per operation contours as a function of V_{DD} and the length of the nMOS devices (Ln) for different inputs. In all the cases, the maximum frequency allowed by the critical path was used.

From Eq. 11, we can see that the only parameters that depend on inputs are W_{effp} and W_{effn}. These parameters depend on the static probability of each node of the circuit and the gate that is driving the node. However, by means of a logic simulation, the term $\sqrt{W_{effp}/W_{effn}}$ from Eq. 11 can be calculated for each possible input. The results are shown in Fig. 13.

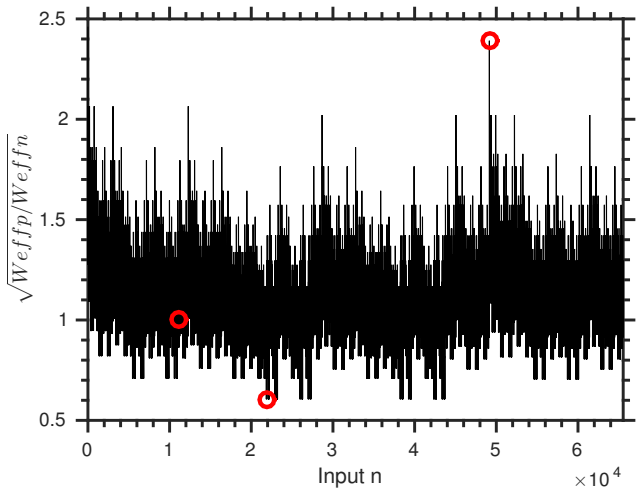


Fig. 13. Relationship between the number of nMOS and pMOS that are imposing the leaking vs the different possible inputs. Test Circuit 2.

In order to assess how much the optimum ALB changes with the input, we selected the three pairs of inputs marked in Fig. 13 and simulated the energy contours as a function of V_{DD} and L_n. We selected one input with the maximum $\sqrt{W_{effp}/W_{effn}}$ ($W_{effp} > W_{effn}$) and another with the minimum ($W_{effp} < W_{effn}$) in order to get a worse cases, and the last one with $W_{effp} \approx W_{effn}$. The results are shown in Fig. 14a, Fig. 14b and Fig. 14c, respectively.

From Fig. 14 we can see that although the optimum length does change in the three cases, selecting one of them, for example 50 nm, achieves almost the same savings as the optimum in comparison with classic symmetric length biasing.

Additionally, depending on the input, the activity factor will change and thus the optimum supply voltage that minimizes energy. From Eq. 11 we can see that the supply voltage also affects the optimum imbalance. In consequence in order to evaluate this we simulated three inputs with different activity factors to see how much did the optimum length change. In the first one, the activity factor is very low (LAF), only one of the seven outputs (S_i) is switching. The second one, with an intermediate activity factor (MAF), the carry is propagated to the output but each of the S_i outputs is not switching. Finally, the third input with a high activity factor (HAF) in which all S_i are switching and the carry is propagated to the output. The simulation results are shown in Fig. 15a, Fig. 15b and Fig. 15c, respectively.

From the simulations we can see that the optimum asymmetric length biasing is $Ln = 50nm$ in the case of HAF and MAF and $Ln = 45nm$ in the case of LAF. However, the energy obtained with either of the two lengths is much less than the energy obtained with a symmetric length ($Ln = 30nm$). So by selecting either of them the energy reductions in comparison with symmetric length are almost the same.

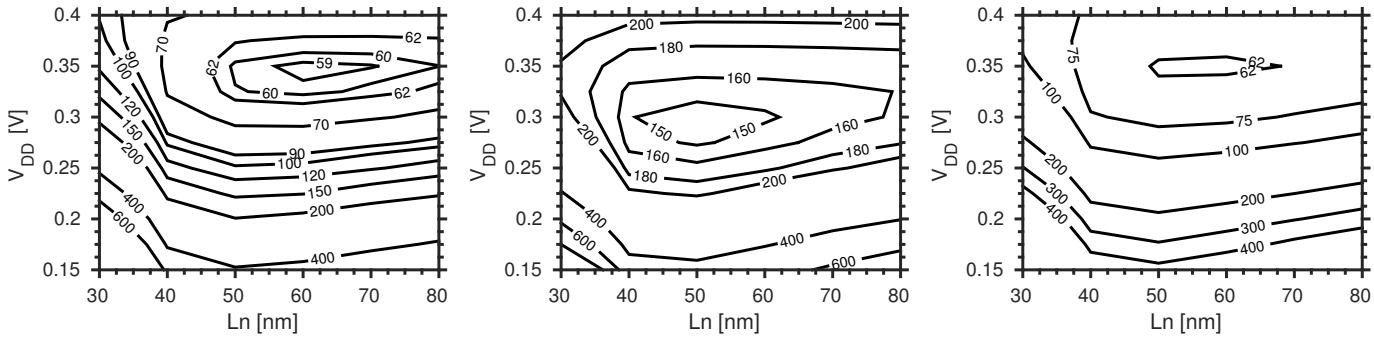
The exact energy reductions depend on the V_{DD} selected for the circuit. For example, if we select a $V_{DD} = 200mV$ in order to minimize the energy of the HAF input which is the one that consumes the most (due to a high dynamic energy), the energy reductions for the other inputs are very high (more than 60% energy reductions). This is because in the MAF and LAF cases with a $V_{DD} = 200mV$ the energy consumption is almost all due to leakage energy which is minimized by asymmetric length biasing.

On the other hand, if we select a $V_{DD} = 350mV$ to minimize the LAF case, the benefits obtained by asymmetric length biasing in the case of the other inputs are very small because, in these cases and for that V_{DD}, the energy consumption is almost entirely dynamic. However, this is not a good decision since the energy consumed by the HAF input, which is the one that consumes the most, is much higher since it is outside its optimum V_{DD}.

In conclusion, we saw that a fixed optimum ALB can be set (e.g. 50 nm in this case) and the energy savings in comparison with the classic symmetric approach are maintained close to the optimum across the different possible inputs of the circuit.

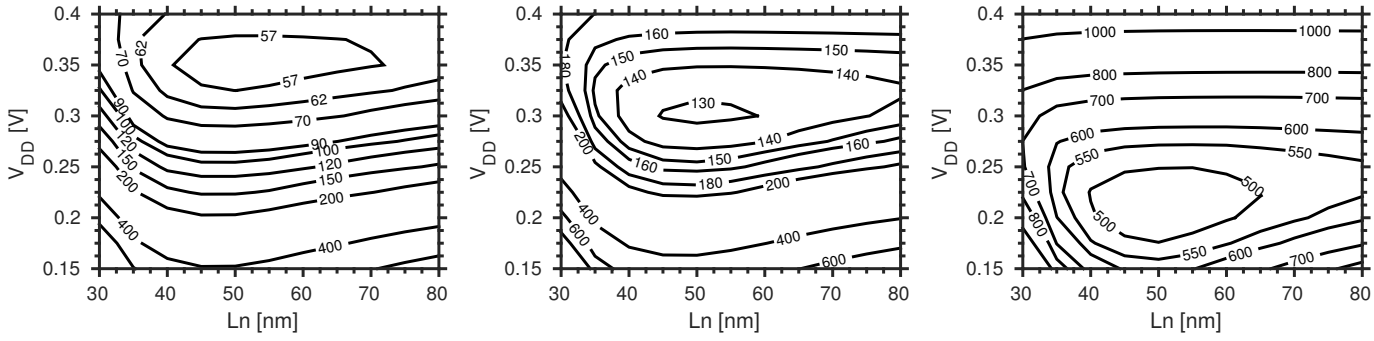
VII. Conclusions

In this work we showed that by using an asymmetric length biasing, the energy per operation consumed by digital circuits can be reduced more than 50% in a wide range of target performances. We presented simulation results for two circuits, a chain of inverters and a Ripple Carry Adder implemented in a FD SOI 28nm technology. The energy reductions are due to two reasons. The first is the dependence of the leakage energy on the imbalance between the leakage current of the pMOS and nMOS devices, as shown with the energy per operation model presented in Section II. The second is that in advanced nanometer technologies, increasing the length of the devices improves the devices parameters (such as sub threshold slope and DIBL coefficient) with very little capacitance increase, since the dominant capacitances are fringing. We also used the



(a) $W_{effp} > W_{effn}$ (b) $W_{effp} < W_{effn}$ (c) $W_{effp} \approx W_{effn}$

Fig. 14. Energy contours [aJ] as a function of V_{DD} and the length of the nMOS (Ln) for three different inputs. $V_{BPp} = V_{BPn} = 0V$. LVT. Test Circuit 2.



(a) Low Activity Factor (b) Medium Activity Factor (c) High Activity Factor

Fig. 15. Energy contours [aJ] as a function of V_{DD} and the length of the nMOS (Ln) for three different inputs. $V_{BPp} = V_{BPn} = 0V$. LVT. Test Circuit 2.

back plane voltage to adjust the speed of the circuits in order to make fair comparisons at different target performances. We presented simulation results with Predictive Technology Models to show that asymmetric length biasing can be used in conventional bulk technologies and as technology scales, the benefits of using asymmetric length biasing increase.

We addressed the impact of asymmetric length biasing in the variability of the energy consumption of the circuit. We saw that asymmetric length biasing almost halved the variability of the devices since they are bigger allowing to build more robust and energy efficient digital circuits. Additionally, since with asymmetric length biasing the circuit is working in the optimum imbalance for the leakage current of the pMOS and nMOS devices, process variations have less impact in the energy consumption.

Then we consider another technique to make the circuits work in the optimum imbalance which consisted in using an asymmetric back plane biasing. We compared this technique with asymmetric length biasing and we showed that in most of the cases ALB and OBB consume almost the same, for example at 1 MHz and 10 MHz. However, at high frequency, OBB spent part of the range of the BB to adjust the optimum imbalance so to achieve 100 MHz is necessary to tune the V_{DD}, increasing the energy consumption (Fig. 6b and Fig. 10). We also showed how both techniques could be combined and we see that energy consumption can be reduced a little more by combining both techniques.

Finally we studied the dependence of the optimum imbalance on the inputs. To do so, we simulated an 8-Bit Ripple Carry Adder. We saw that for different inputs, with different static probabilities and with different activity factors, a fixed asymmetric length can achieve very good energy reductions in spite of the small changes in the optimum imbalance.

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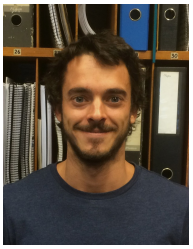

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