Settling time-based Design of a Fully Differential OTA for a SC Integrator

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***Abstract*—This paper optimizes the design of an OTA for a Switched Capacitor (SC) Integrator in a discrete time Sigma-Delta Modulator based on the total settling time requirement and by application of the g_m/I_D method. One of the main constraints when implementing SC Sigma-Delta ADCs for high sampling rates is the requirement for the transition frequency and settling behavior of the operational transconductance amplifier. Extensive analysis has been carried out concerning the settling time, however an optimum regarding the distribution between the slew and linear periods is yet to be defined. The g_m/I_D method is used to sweep the design space of an OTA in order to find a minimum in power consumption thus an optimum slew/linear distribution. The method is validated through the design of three 2.5ns settling time OTAs for two design scenarios with different slew/linear distribution in a 130nm CMOS process. Results show that consumption savings of up to 60% are achieved when compared to the optimum design.**

***Index Terms*—OTA, g_m/I_D, transition frequency, settling time, SC integrator, Sigma-Delta modulation.**

I. Introduction

Discrete-time (DT), switched-capacitor circuits are a widespread tool for implementing $\Sigma\Delta$ data converters. These data converters are pushed by an increasing demand for higher rates and lower consumption i$\Sigma\Delta$ data converters in order to handle, e.g. current mobile high bandwidth communication systems. In SC circuits higher sampling rates leads to higher consumption due to the need of achieving acceptable settling at the output of the OTAs in each clock phase.

The settling time of an amplifier, t_s, is defined as the minimum time required for its output voltage to settle within an error tolerance of its steady-state value [1]. Two distinct periods determine the settling time: the slewing period and the linear settling period. During the slew period, the variation of the output is restricted to a maximum value (slew rate) caused by a limited current. In the linear period the amplifier behaves linearly according to its small signal frequency response (transition frequency and phase margin) [2]. Extensive analysis has been carried out on what considerations have to be made in order to have robust implementations. In [3]- [4] the metho- dology to design process-insensitive integrators taking special notice to the settling behavior was presented. In a similar manner the impact of the switch resistance on the settling time has been studied [5]. However, in general, in SC applications the period where the amplifier slews is chosen arbitrarily as a part of the total settling time available. However, it has been shown [2] that an optimum exists. In this paper we assess what is the reduction that can be achieved in power consumption by trying to take advantage of this optimum. Differently from reference [2], this is done in the practical context of a fully differential SC integrator for a high rate (200MHz) $\Sigma\Delta$ data converter in a 130 nm CMOS process. Furthermore, a complex Complementary Folded Cascode Feedforward Compensated (CFCFC) OTA is considered and the settling based design methodology for this OTA is presented.

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The g_m/I_D methodology addresses several problems of analog design such as power consumption and yields a pers- pective different to the classic one where the MOS transistors either worked on weak inversion or strong inversion. More- over, this method gives the designer a series of degrees of freedom of which he/she has control over, enabling the design of robust and low power consumption systems. Itself, the g_m/I_D ratio is a measurement of the efficiency to translate current into transconductance (higher the value, higher the transconductance for a constant current). Furthermore, the g_m/I_D ratio can be extensively exploited during the analog circuit design phase by creating an exploration of the available options attainable according to this parameter (power con- sumption, gain, transition frequency). The data to implement the g_m/I_D method can be obtained analytically, using a MOS transistor model that provides a continuous representation of the current and small-signal parameters in all regions of operations, or from measurements or simulations on a typical transistor [6]- [7]. This last approach is applied here.

In this work, a design methodology for OTAs in SC Inte- grators based on the total settling time requirement for a given sampling period is presented. By means of the g_m/I_D method a sweep of the design space is implemented in order to find the optimum power consumption thus the best distribution for the slew and linear periods of the settling time. The integrator under study is the Front-end of a 4th Order DT $\Sigma\Delta$ Modulator similar to that shown in [8], with a sampling frequency, f_s, of 200MHz for a bandwidth of 10MHz and a 3-Level Quantizer.

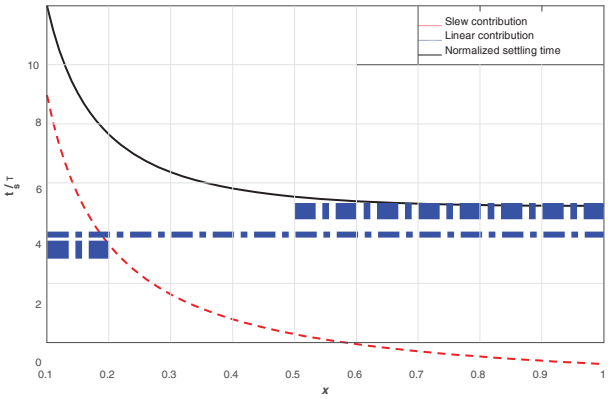

Fig. 1. Normalized settling time and slew/linear contributions

II. Settling Time-based Synthesis

The time constant, τ, for the amplifier in closed loop configuration is given by:

$$\tau = \frac{1}{2\pi\beta f_T} \quad (1)$$

where β is the feedback factor and f_T the transition frequency of the amplifier. As depicted in [2] the settling time taking into account the linear and the slewing parts is written as:

$$t_s = \tau \left(\ln\left(\frac{1}{D}\right) + \ln\left(\frac{\tau \cdot SR}{V_{step}}\right) + \frac{V_{step}}{\tau \cdot SR} - 1 \right) \quad (2)$$

$$= \tau \left(\ln\left(\frac{1}{D}\right) + \ln(x) + \frac{1}{x} - 1 \right)$$

$$x = \frac{\tau \cdot SR}{V_{step}} \quad (3)$$

where SR is the slew rate of the amplifier, D the error bound, V_{step} represent the output step, which is the input step divided by β, and x corresponds to the fraction of the total step where we have linear settling. The first two terms of (2) represent the linear part of the settling while the rest the slewing one;
their contributions to the normalized settling time according to x are shown in Fig. 1.

III. Front-end SC Integrator

The OTA design is based on the front-end SC Integrator architecture shown in Fig. 2, which is fully differential since is the key for designing a robust implementation (reduces the common mode noise due to the power supply and substrate, clock feedthrough, charge injection and eliminates even-order harmonic components) [9]- [10]. The feedback D/A Converter is a 3-Level implementation that along with φ_2 create the control signal for the switches. Since the gain of the input signal and feedback path are the same, the sampling capacitor, C_s is shared, reducing the switch and capacitor count. The feedback factor is defined as:

$$\beta = \frac{C_f}{C_s + C_{in} + C_f} \quad (4)$$

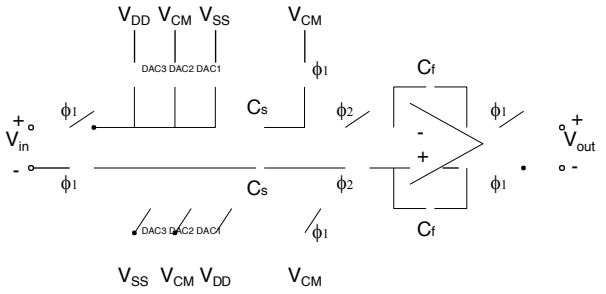

Fig. 2. Front-end SC Integrator

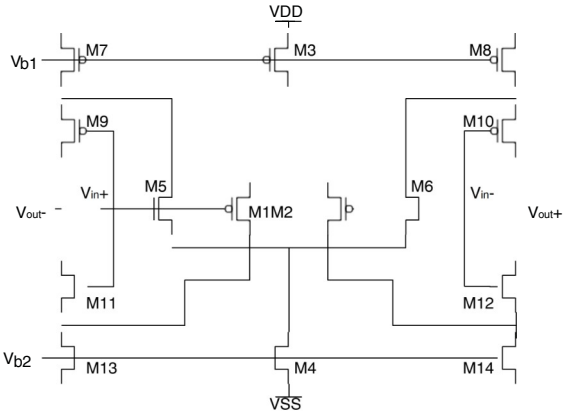

Fig. 3. CFCFC OTA [11], [12]

where C_f is the integration capacitor and C_{in} represents the parasitic capacitances of the input transistors [3]. Depending on the values of C_s and C_f the input parasitic capacitance can have a noticeable impact on the feedback factor, especially when the required transition frequency is high (the increase on the transconductance requires wider transistors, resulting in big parasitic capacitances). The equivalent load seen at the output of the front-end integrator during the integration phase can be written as:

$$C_L = C_o + \frac{(C_s + C_{in})C_f}{C_s + C_{in} + C_f} \quad (5)$$

where C_o represents the output node capacitances (intrinsic to the OTA's architecture and implemented Common Mode Feedback Circuit).

IV. OTA Design

The chosen OTA architecture is the Complementary Folded Cascode Feedforward Compensated shown in Fig. 3, in which the cascode stages provide high gain and fast operation even when low power supply is used (as low as ±0.6V) [11]. The feedforward technique lends itself for low supply folded cascode amplifiers since the DC bias for the cascode and input transistors is the same, that is the middle point between the positive and negative voltage supply (in this case 0V), allowing
the gate connection.

A. CFCFC OTA: g_m/I_D Design

The transition frequency and slew rate of the CFCFC OTA are defined as:

$$f_T = \frac{1}{2\pi}\frac{g_{m,eff}}{C_L} \tag{6}$$

$$SR = \frac{2I_{D-In}}{C_L} \tag{7}$$

From (1), (3), (6) and (7) the fraction where we have linear settling can be found to be a function of g_m/I_{D-In} and the input step:

$$x_{in} = \frac{\left(\frac{g_m}{I_D}\right)^{-1}}{V_{step\_in}} \tag{8}$$

Two study cases were defined for the definition of the input step for the SC Integrator: the first one without taking into account the feedback signal of the DAC where the step is defined as the maximum change that the input signal (f_{in}) can have in a sampling period for a rail-to-rail implementation (V_{max}):

$$V_{step\ in} = \frac{2\pi f_{in} V_{max}}{f_s} \tag{9}$$

resulting in $V_{step\ in} = 0.188V$. In the second one the step is defined as a worst case where the integrator has to process V_{DD} or V_{SS} ($\Sigma\Delta$ Integrator), resulting in $V_{step\ in} = 0.6V$.

Combining (1) and (2), we have that the needed transition frequency is a function of the required settling time:

$$f_T = \frac{\ln\left(\frac{1}{D}\right) + \ln(x) + \left(\frac{1}{x} - 1\right)}{2\pi\beta t_s} \tag{10}$$

Once the transition frequency and load of the amplifier have been defined for the system at hand, the transconductance is obtained according to:

$$g_{m,eff} = 2\pi f_T C_L \tag{11}$$

where $g_{m,eff}$ is the sum of transconductances of both input pairs.

According to the different role that every transistor has, the g_m/I_D ratios can be chosen, giving the designer a tool to optimize the circuit. As an example, the g_m/I_{D-In} ratio for the complementary input pairs can be chosen to be high in order to achieve the f_T with a low bias current. The cascodes' ratios (g_m/I_{D-Cas}) could provide the circuit with gain without sacrificing phase margin (especially M9-M10), achieved in the moderate inversion. The current sources (M3- M4) can be designed in strong inversion (low g_m/I_{D-Sou}) to minimize the area consumption. For M7-M8/M13-M14, which have an impact both in gain and non-dominant pole (parasitic capacitances), the moderate inversion region can be chosen. However, since the input pairs' parasitic capacitances have an impact on the feedback factor and load, these changes must be taken into consideration while on the design stage.

The procedure that explores the design space (Fig. 4) is as follows:

1) The lengths of the transistors are taken to the minimum value (which can be later changed to increase the DC gain). The integrator's capacitors, the requirement for settling time, the error bound and the magnitude of the input step are defined.
2) Values for the g_m/I_D of all transistors are chosen.
3) The load, feedback factor and x are calculated, from which the required transition frequency is obtained.
4) The current flowing through the input transistor is found according to the transconductance (with the g_m/I_D curves) and W is deduced with the previously defined L. This action is carried out for every transistor of the amplifier.
5) The parasitic capacitances are obtained according to the dimensions of the transistors (with the g_m/I_D curves) from which the load and β (thus f_T) are recalculated.
6) If the relative difference between the synthesized values with the initials is less than a given error then the procedure is finished.
7) The design space is explored by systematically sweeping the g_m/I_D ratios of the transistors for the required settling time.

V. Results

For a SC Integrator the settling of the output voltage must occur in half the sampling period ($T_s = 5ns$) which leads to a maximum allowed settling time of $2.5ns$. Using this parameter as a design goal when implementing the afore-mentioned methodology a minimum in current consumption for the two cases of study is found as shown in Fig. 5 ($g_m/I_{D-In} = 17$ - $g_m/I_{D-Cas} = 13$ and $g_m/I_{D-In} = 11$ - $g_m/I_{D-Cas} = 13$, in all cases units are V^{-1}). Therefore, the optimum slew/linear distribution for the two cases for the system under study are 34.6%/65.4% and 62.15%/37.85% of the total settling time respectively. Three OTAs per case were designed to compare the results between slew/linear distribution: the optimum power consumption design and two OTAs where the suggested slew allotments of 10% and 25% are implemented [13]- [14] (Table I). In the case of the second integrator, for the considered g_m/I_D range, the minimum slew allotment achieved is 14.5%. This value is considered in placed of the 10% criterion. Therefore the actual savings will be even higher. The results show that the optimum distribution for the slew/linear periods brings a power saving of 37%/60% when compared with the allotment of around 10% and 10%/43% when compared to the one of 25%.

VI. Conclusions

The optimization of the slewing/linear settling period for a given complete settling time in the design of an SC integrator for a Sigma Delta converter has been analyzed. It has been shown that this design approach, instead of aiming at arbitrary chosen slew rate values, allows to have an optimum in power consumption without other penalties and, when compared with fixed slew allotment of 10%, the savings can be as high

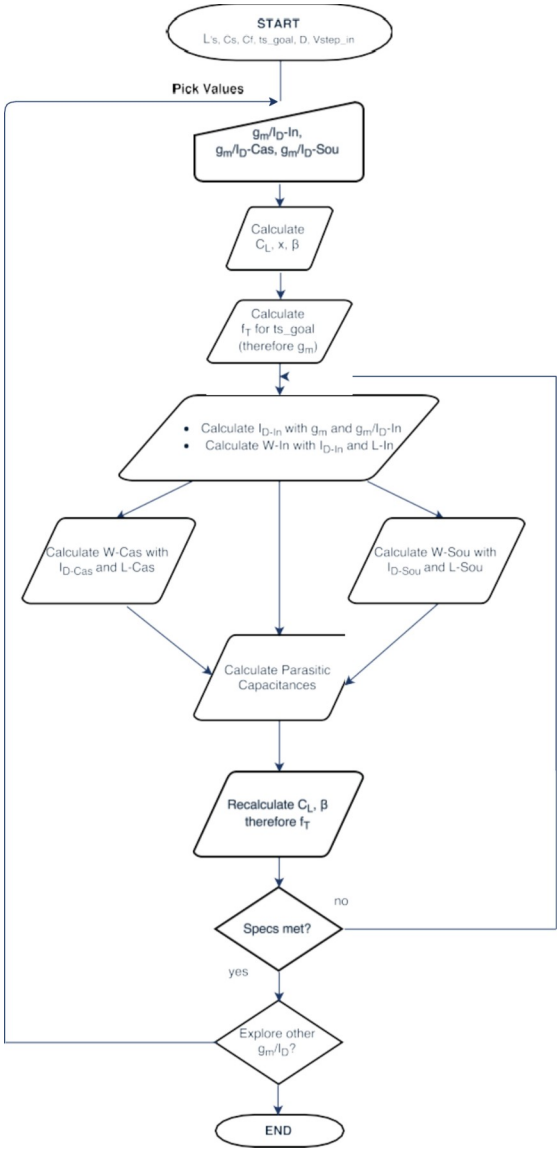

Fig. 4. Settling time-based Step by Step CFCFC OTA Design

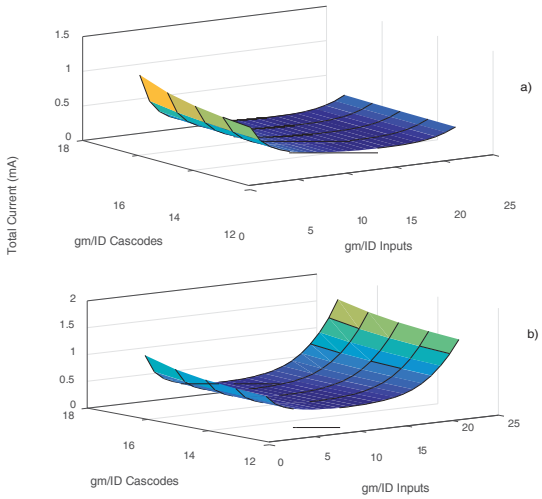

Fig. 5. Current Consumption sweep for the required settling time: a) Stand Alone integrator with $V_{step\ in} = 0.188V$, b) ΣΔ Integrator with $V_{step\ in} = 0.6V$

TABLE I
COMPARISON BETWEEN DIFFERENT SLEW/LINEAR DISTRIBUTIONS
($D = 0.5\%$, $C_s = 200fF$, $C_f = 800fF$, $g_m/I_{D-Sou1,2} = 12, 10$)

Equation based						Electrical Simulation
g_m/I_D $In - Cas$	f_T (MHz)	C_L (fF)	I_{total} (μA)	$Slew$ $(\%)$	SR $(V/\mu s)$	t_s (ns)
Case 1: Integrator ($V_{step-in} = 0.188V$)						
8 – 14	438	203	229.7	9.37	343	2.85
13 – 15	481	214	161.3	24.7	232	2.6
17 – 13	535	234	145.1	34.6	197	2.43
Case 2: Integrator with feedback DAC ($V_{step-in} = 0.6V$)						
3 – 15	444	200	784.9	14.5	929	2.77
4 – 14	470	200	546.8	24	738	2.55
11 – 13	749	222	312.7	62.1	427	2.23

as 60%. The design method for this optimization has been summarized.

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