Is intrinsic noise a limiting factor for subthreshold digital logic in nanoscale CMOS?

Francisco Veirano*, Fernando Silveira* and Lirida Naviner†
*Instituto de Ingeniería Eléctrica, Facultad de Ingeniería, Universidad de la República
Montevideo, Uruguay.
{fveirano, silveira}@fing.edu.uy
†Institut TELECOM, TELECOM ParisTech, LTCI-CNRS
Paris, France.
lirida.naviner@telecom-paristech.fr

***Abstract*—Intrinsic noise has been predicted as a limit to CMOS scaling. If this is the case, the effect would be more severe at low supply voltages, such as the ones applied in subthreshold digital circuits. In this work the effect of intrinsic noise in subthreshold digital nanoscale CMOS is analysed for the first time. Key issues such as variability and the actual bandwidth of the studied circuits are taken into account. Most of previous works overestimate the impact of intrinsic noise due to the use of simplified models of the MOS transistor. BSIM4 transistor model and PTM model files are used in order to correctly calculate noise RMS voltage at the output node of an inverter, which has not been done before in the subthreshold region. Technology scaling impact is explored by simulating technology nodes from 130 nm down to 16 nm and considering variability down to 32 nm. Simulation results show that variability strongly increases the minimum operating voltage of subthreshold digital nanoscale CMOS and thus making intrinsic noise not a problem, at least down to 32 nm, since commutation voltage maintains high enough to achieve negligible failure rates.**

I. Introduction

In the past two decades, important efforts have been established to attain a lower boundary for digital CMOS technology scaling. Several works have pointed out that a physical limit would arise due to the false bit flip generated by intrinsic noise sources such as thermal, shot and flicker noise [1]–[4].

In [1] Stein derived a relationship between the minimum energy per logical operation consumed by an ideal CMOS inverter and the bit error rate due to random fluctuations introduced by thermal noise which obeys a Gaussian distribution. Moreover, he compared these minimums energies with fundamental limits of CMOS presented in [5] by Swanson et al. and stated that minimum energy per logical operation is limited by intrinsic noise when considering acceptable bit error rates. This analysis was extended by Natori et al. in [2] considering the effect of a subsequent gate using as case study a chain of idealized inverters. This approach limited the noise frequency range that could propagate through the next logic gate. Under these conditions the authors suggested that the scaling limit lied around 10-20 nm. A similar result was achieved by Kish in [3] where he pointed out that serious problems would emerge around 25 nm due to thermal noise.

The key problem with these approaches is that they all use an idealized model for the CMOS inverter consisting of a constant drain source resistance and a constant output capacitance, therefore considering the noise power spectral density (PSD) of a resistor. On the contrary, in [4] Kleeberger et al. used BSIM4 transistor model [6] and Predictive Technology Models (PTM, available under http://ptm.asu.edu) files in order to account the noise PSD at the output of a CMOS inverter down to the 16 nm node. The authors conclude that previous works overestimate noise root-mean-square (RMS) voltage up to a factor of 4 stating that intrinsic noise will not be a problem until at least 8 nm.

These prior works considered operation at nominal, above the threshold supply voltage (V_{dd}). However, sub/near threshold logic has emerged as a solution for energy constrained applications since the dynamic energy consumption is quadratically reduced with V_{dd}. Prior studies show that the minimum energy consumption is generally achieved while working in this region [7]–[11]. Additionally, technology scaling makes sub/near threshold digital circuits even more attractive since the gate delay is greatly decreased by using nanometer technologies. This allows implementing sub/near threshold digital circuits with low and medium performance constraints. Nevertheless, while working with sub/near threshold circuits, variability becomes critical mainly due to the exponential dependence between the transistors drain current and the threshold voltage, supply voltage and temperature [12]–[14].

In this work we address the question on how does intrinsic noise affects sub/near threshold digital circuits. As V_{dd} is reduced the commutation voltage (V_m, voltage where $V_{in} = V_{out}$ in the static characteristic of an inverter) decreases and variability is worsen making the added effect of variability and intrinsic noise a potential problem. In order to formally account for the intrinsic noise in sub/near threshold digital circuits, we used the BSIM4 transistor model and PTMs parameters to determine the noise PSD at the output of an inverter. Additionally, the bandwidth of the subsequent gate was considered in order to obtain the noise RMS voltage at the output node of an inverter. Then, the failure rate of the circuit can be obtained as the mean frequency of crossing a

given threshold voltage.

This paper is organized as follows. Section II presents the proposed methodology used to characterize the output noise of an inverter and the failure rate of the circuit. Simulations results are presented in Section III. Finally, conclusions are drawn in Section IV.

II. Model and method

A. Characterizing noise RMS voltage

In this section the model and methodology used to determine the noise RMS voltage at the output of an inverter is presented. Previous works [1], [3] used a simplified model for the MOS transistor consisting of a drain source resistance and an output capacitance. Using this model and considering the noise PSD of a resistance, the output noise RMS voltage can be determined by

$$V_N = \sqrt{\frac{kT}{C}} \tag{1}$$

where k is the Boltzmann's constant, T the temperature and C the output capacitance of the aforementioned model. This approach does not take into consideration how would the noise propagate through a subsequent gate and thus not takes into account the bandwidth of the next gate. In [2] this effect is included, considering the same simplified model for the following gate (an inverter in this case), thus limiting the noise PSD to $f = 1/(2\pi R_o C_o)$, where R_o is the drain source resistance and C_o the output capacitance of the next gate. This bandwidth also overestimates noise RMS voltage. A different methodology was presented in [4] were the noise PSD was obtained from electrical simulations and integrated up to 6 THz to obtain noise RMS voltage. In this case neither the bandwidth of the subsequent gate is taken into account, instead an arbitrary large bandwidth is considered.

In this work we used as characterization circuit an inverter and as subsequent gate an inverter of the same size. A chain of inverters were added to guarantee real input logic levels. The noise RMS voltage was determined by integrating the noise PSD at the output of the inverter considering a first order filtering characteristic for the subsequent gate. Electrical simulations were performed to calculate the noise PSD at the output node of the inverter ($N(f)$). The bandwidth (f_{3db}) of the subsequent inverter was also obtained from electrical simulations biasing it with $V_{in} = V_m$, Fig. 1 shows the setup used for the bandwidth characterization. The center inverter is the test one. The first shorcircuited inverter allows to bias the test inverter input at V_m, while the last one sets the load for the test inverter. Therefore, the bandwidth is extracted as the -3dB frequency of $H(f) = V_{out}/V_{in}$ (Fig. 1). In order to verify the assumption that the bandwidth biased in this point was an acceptable estimation for the filtering characteristic of the subsequent gate, simulations were performed with a square input signal slightly higher than V_m. Then, by varying the frequency of this signal it was seen that for frequencies higher than this bandwidth, the subsequent gates would filter the input while for lower frequencies a bit flip would occur in a following gate. In Fig. 2 the simulated inverter's bandwidth as a function of the supply voltage for each technology node is shown. Finally, as the noise PSD is dominated by white noise, the noise RMS voltage can be evaluated as

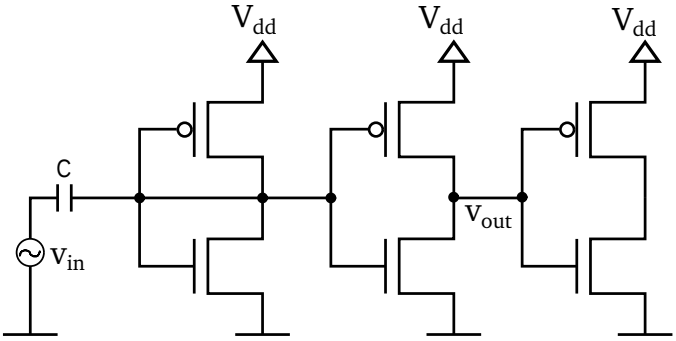

Fig. 1. Inverter's bandwidth characterization setup.

$$V_N = \sqrt{\int_0^\infty N(f) \left| \frac{1}{(f/f_{3db})j + 1} \right|^2 df} \approx \sqrt{N_0 f_{3db} \frac{\pi}{2}} \tag{2}$$

B. Characterizing circuit failure rate

After characterizing the amplitude noise RMS voltage, the circuit failure rate must be evaluated. In [1], [2] the circuit failure rate is determined as the probability that the noise exceeds a given threshold voltage (V_{TH}) which can be calculated using

$$P_{err} = \frac{1}{2} ercf\left(\frac{V_{TH}}{\sqrt{2}V_N}\right) \tag{3}$$

where V_N is the noise RMS voltage. On the other hand, [3] characterizes the failure rate of the circuit by the mean frequency of crossing a given threshold voltage (V_{TH}). If the noise process corresponds with band limited white noise, this

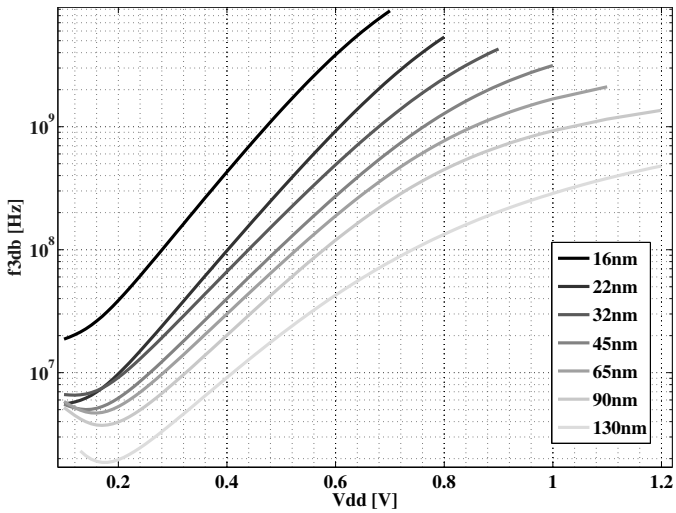

Fig. 2. Inverter's bandwidth simulation as a function of the V_{dd} for all the technology nodes.

mean frequency can be calculated as

$$f_{mean} = \frac{2}{\sqrt{3}} exp\left(\frac{-V_{TH}^2}{2V_N^2}\right) f_c \tag{4}$$

where f_c is the cut-off frequency used during the integration of the noise PSD.

In both approaches, the failure rate of the circuit is mainly determined by the relationship between the given threshold voltage (V_{TH}) and the noise RMS voltage (V_N). This can be seen in Fig. 3 where the relationship between the failure rate and the relationship $S = \frac{V_{TH}}{V_N}$ using 4 is depicted for three different f_c.

An acceptable failure rate depends on the application for which the circuit is intended to be used and the size of this, but from Fig. 3 it can be seen that large changes in f_c or acceptable failure rate (as the circuit size changes) change only slightly the required S. Reasonable criterion for S is [3]

$$S = \frac{V_{TH}}{V_N} > 9..12\ . \tag{5}$$

The V_{TH} is the minimum noise voltage required to generate a false bit flip ahead in the logic chain. This threshold voltage is calculated as

$$V_{TH} = V_{OH} - V_m \tag{6}$$

when the output logic level is high and

$$V_{TH} = V_m - V_{OL} \tag{7}$$

when the output logic level is low, where V_{OH} and V_{LH} are the output logic levels of the inverter. The threshold voltage is calculated like this since a lower noise voltage amplitude would be filtered by the regenerative property of the CMOS logic. Additionally, the output logic levels must be calculated taking into consideration the effect of the subthreshold static currents of the MOS transistor which make the outputs logic levels to move from their ideal values V_{dd} and gnd.

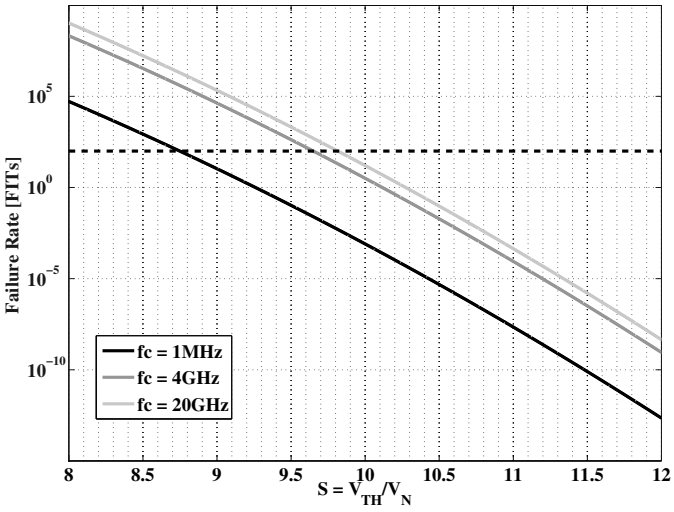

Fig. 3. Failure rate vs relationship $S = V_{TH}/V_N$ using 4.

In summary, in order to determine whether the intrinsic noise is a problem or not, first we should determine from electrical simulations the noise PSD, V_m, V_{OH}, V_{OL} and the bandwidth of the subsequent gate biased with $V_{in} = V_m$. Then, calculate the noise RMS voltage considering the bandwidth of the subsequent gate and finally compare it with the threshold voltage V_{TH} in order to evaluate the failure rate of the circuit. Additionally, variability effects should be considered in the calculation of the noise PSD, V_m, V_{OH}, V_{OL} and the bandwidth.

III. Simulation Results

A. Impact of intrinsic noise in nanoscale CMOS digital circuits

In this section simulation results are shown in order to address the question on how does intrinsic noise affects sub/near threshold digital logic in nanoscale CMOS using the methodology presented in the previous section. In order to model the CMOS inverter, the BSIM4 transistor model was used. The input parameters for this were taken form the PTM model files from 90 nm down to 16 nm nodes. Additionally, an industrial process design kit was used for 130 nm technology node simulation.

The sizing of the inverters was done so that the V_m was close to $V_{dd}/2$ under nominal V_{dd} and thus maximizing the V_{TH}. Table I shows the sizes of the inverters for each technology node.

TABLE I
Transistor's Size

Node	L_n=L_p	W_n	W_p/W_n
16 nm	16 nm	16 nm	2
22 nm	22 nm	22 nm	2.5
32 nm	32 nm	32 nm	2.5
45 nm	45 nm	45 nm	3
65 nm	65 nm	65 nm	3.5
90 nm	90 nm	90 nm	3.5
130 nm	120 nm	160 nm	4

Fig. 4 shows the simulation results for the noise RMS voltage as a function of V_{dd} for all the considered technology nodes. In this case simulations were performed with a temperature of 120 °C and with an input low logic level. The figure shows the same trends pointed out in previous works, that at nominal V_{dd}, the noise RMS voltage increases with technology scaling. However, due to the limited bandwidth of the next inverter, the amplitude of the noise RMS voltage is reduced, around 50%, in comparison with previous published predictions.

When V_{dd} is decreased, the bandwidth of the inverter decreases and so does the noise RMS voltage. This holds until the increase of the noise PSD, due to the increase of the on resistance of the transistor and thus the increase of the thermal noise, makes the noise RMS voltage starts to increase again in the subthreshold region.

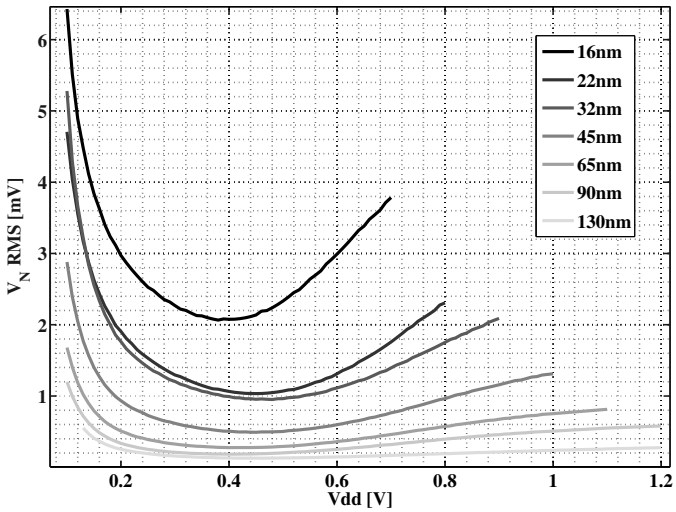

Fig. 4. Noise RMS voltage vs V_{dd} for different technology nodes. $T = 120\,^{\circ}\mathrm{C}$. $V_{in} = 0$.

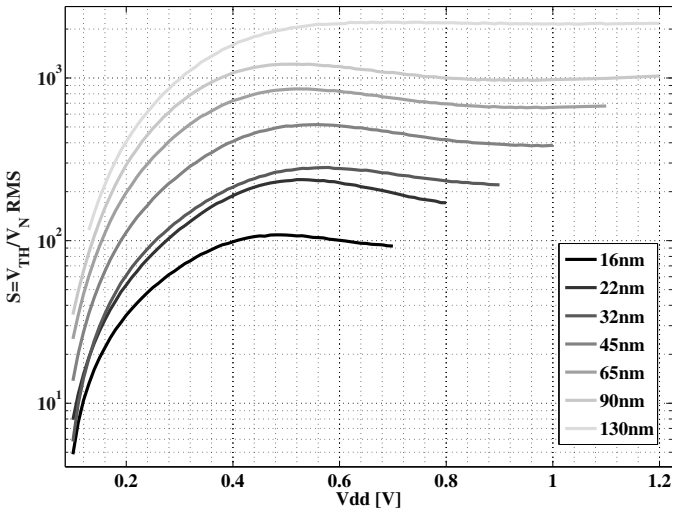

Fig. 5. $S = V_{TH}/V_N$ vs V_{dd} for different technology nodes. $T = 120\,^{\circ}\mathrm{C}$. $V_{in} = 0$.

Further on, to evaluate the failure rate as a function of V_{dd}, the relationship S from Eq. (5) needs to be calculated. In order to do this the DC parameters of the inverter V_m, V_{OH} and V_{OL} were simulated. In this simulation, the output logic levels were calculated taking into account the effect of the subthreshold static currents of the MOS transistor which make the outputs logic levels to move from their ideal values V_{dd} and gnd. The simulation results of S as the supply voltage is varied are shown in Fig. 5 for the different technology nodes. As it can be seen in the figure, at nominal supply voltage, the failure rate is very small ($S >> 9..12$) and thus making intrinsic noise not a problem, at least until 16 nm and without considering variability.

On the contrary, while decreasing V_{dd}, S decreases dramatically when entering the subthreshold region. This was to expect as the noise RMS voltage increases in the subthreshold region while V_{TH} decreases since V_m decreases and the output logic levels move from their ideal values. For the 32 nm node, when the V_{dd} is decreased to $100\ mV$, the relationship between the V_{TH} and V_N decreases to 5. However, we need to consider if it is feasible that a circuit works under this V_{dd} and thus calculate the minimum V_{dd} for the logic gate. Moreover, variability effects must be taken into consideration.

B. Variability effect on intrinsic noise analysis

To consider variability effects in the intrinsic noise analysis, the PTM corner model files were used. For the time being only corner model files are available up to the 32 nm technology node. In order to calculate the minimum operating supply voltage ($V_{dd_{min}}$) we used the methodology presented in [8]. The $V_{dd_{min}}$ depends on the transistor sizing, the process variations and the gate under consideration. In this case, the transistor sizing is fixed so the $V_{dd_{min}}$ is the one that maintains V_{OH} higher than $0.9V_{dd}$ and V_{OL} lower than $0.1V_{dd}$ for the worst case process variations [8]. Table II shows the minimum operating V_{dd} for each technology node. As it was pointed out in [13], variability is worsen with technology scaling which makes minimum V_{dd} to increase as technology shrinks. Although other criteria might be considered to determine the $V_{dd_{min}}$, Table II shows that with the chosen criterion the resulting $V_{dd_{min}}$ is well above the V_{dd} range where noise is a concern. Therefore, is likely that this is also the case for slightly different criteria to determine $V_{dd_{min}}$.

The same noise characterization analysis was done, but considering the minimum operating voltage and the variability effects in the noise PSD, bandwidth, V_m, V_{OH} and V_{OL}. In Fig. 6 the noise RMS voltage simulated for the 32nm node is shown with their respective corners. It can be seen that the FS corner increases the noise RMS since the input voltage is low making the noise PSD to increase due to the decrease of the on resistance of the PMOS transistor. In the same way, the SF corner decreases the noise RMS voltage.

However, in spite of the increase of the noise RMS voltage, S is maintained high enough to achieve a low failure rate as can be seen in Fig. 7. This can be explained because the minimum operating voltage is too high and the threshold voltage is still high.

The presented analysis used fixed transistor sizes which were selected in order to obtain a better V_{TH}, though, in energy constrained applications where the minimum energy point is below this minimum operating voltage, the designer

TABLE II
MINIMUM OPERATING V_{dd}

Node	Minimum V_{dd} [mV]
32nm	240
45nm	190
65nm	160
90nm	150
130nm	135

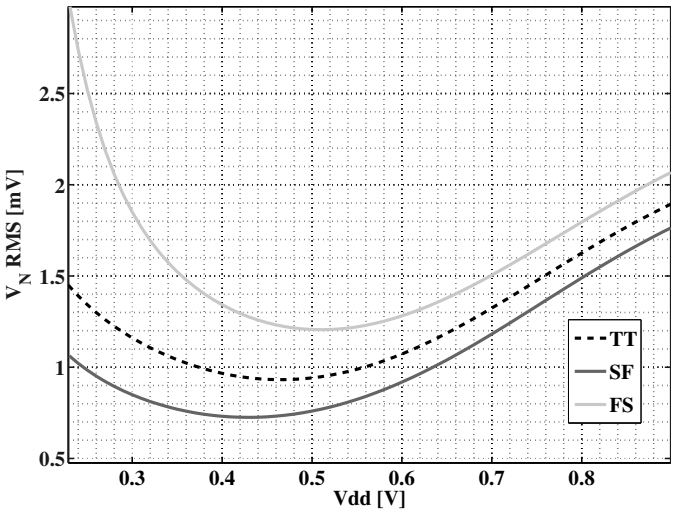

Fig. 6. Noise RMS voltage vs V_{dd} for 32 nm with corner simulations. $T = 120\,^{\circ}\mathrm{C}$. $V_{in} = 0$.

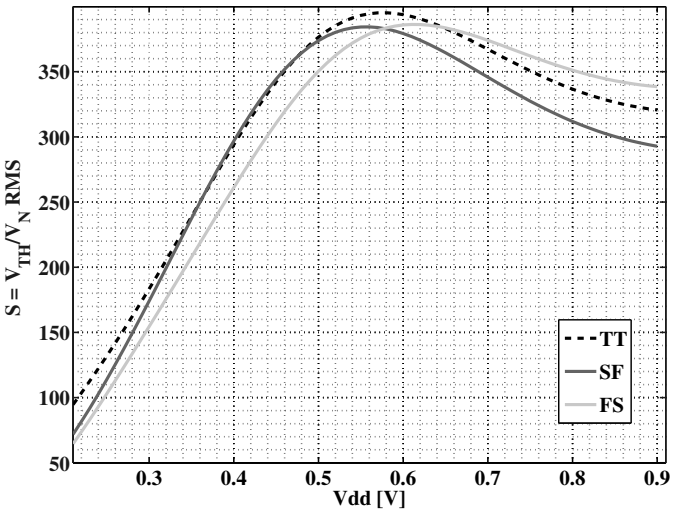

Fig. 8. $S = V_{TH}/V_N$ vs V_{dd} for 32 nm with corner simulations. $T = 120\,^{\circ}\mathrm{C}$. $V_{in} = 0$. $W_p = 4.5W_n$.

might choose a higher W_p/W_n in order to achieve a lower energy consumption. In that case, V_{TH} decreases. Fig. 8 shows S, for an inverter sized to reach the minimum operating voltage of the technology node. Even though the V_{TH} decreased, the noise RMS voltage was also decreased due to the reduction in the bandwidth of the following inverter whose output capacitance increased. Thus, S is maintained almost equal to the previous sizing criterion.

IV. Conclusions

In this work we propose a procedure for assessing the impact of intrinsic noise, which enhances the state of art by:

- Extending previous intrinsic noise analysis to digital circuits working in the subthreshold region.
- Improving the characterization of the noise RMS voltage by considering a realistic bandwidth for a subsequent gate.
- Considering the actual threshold voltage including the effects of the subthreshold static currents on V_{OH} and V_{OL}.
- Accounting variability effects and minimum operating voltage in the calculation of the noise PSD, inverter's bandwidth, V_m, V_{OH} and V_{OL}.

To summarize we can state that intrinsic noise is not a problem in nanoscale CMOS subthreshold logic down to 32 nm, and the main reason is that variability effects make these technologies not compatible with ultra low supply voltage. If a modified circuit structure would allow operate at lower voltages, the impact of noise in this structure should be assessed through the technique presented in this work.

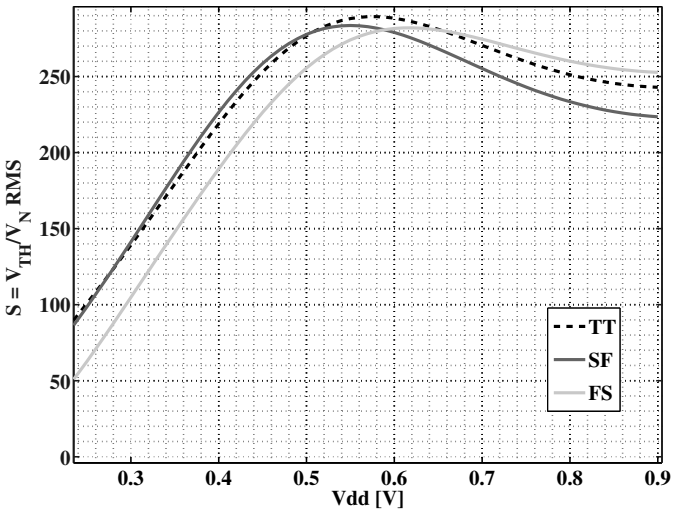

Fig. 7. $S = V_{TH}/V_N$ vs V_{dd} for 32 nm with corner simulations. $T = 120\,^{\circ}\mathrm{C}$. $V_{in} = 0$.

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