Trilateral South-American project: a reference system for measuring electric power up to 100 kHz - progress report

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Abstract. Three countries in South America are jointly developing a reference system for measuring electric power up to 100 kHz. The objective is the construction of three similar measuring systems, one for each institute. The measuring system is described and its design requirements are presented. This project will contribute to provide calibration services in measuring ranges still not covered by the three institutes.

1. Introduction

In the last decades, the increased use of nonlinear loads in power distribution networks has caused a significant increase in the waveform harmonics degrading the quality of the power delivered to the customer. The reliable measurement of waveform harmonics requires refined techniques.

The nonlinear loads include the new technologies of compact lighting and the use of switching converters. The latter are used both in transmission and distribution networks in power electronics applications. Such loads also include switched-mode power supplies (SMPS) used in computers. SMPS switch voltages (in the order of 400 V) in frequencies in the range of kilohertz producing harmonics beyond 1 MHz.

Comparisons on harmonic power are being planned at the level of the Consultative Committee on Electricity and Magnetism (CCEM) and of the Inter-American System of Metrology (SIM).

To address this concern, the Instituto Nacional de Metrologia, Qualidade e Tecnologia (Inmetro), in Brazil, the Instituto Nacional de Tecnología Industrial (INTI), in Argentina, and the Administración Nacional de Usinas e Transmisiones Eléctricas (UTE), in Uruguay, are jointly developing a reference system for measuring electric power up to 100 kHz. The objective is the construction of three similar measuring systems, one for each institute. The project is supported in part by the Conselho Nacional de Desenvolvimento Científico e Tecnológico (CNPq), in Brazil.

This project will contribute to provide calibration services in measuring ranges still not covered by the three institutes. The project will also contribute to improve the traceability not only of electric power but also of related quantities like ac-dc transfer, voltage ratio, phase angle, ac voltage and ac current.

2. Measuring system

Calibration systems for harmonic power analyzers and power quality measuring instruments generally consist of a digital generator with two independent channels (one for voltage and one for current). Arbitrary voltage and current waveforms are programmed and applied to the instrument under calibration. The amplitude ratio and phase displacement of the two signals can be adjusted by changing the generator settings. Voltage dividers and current shunts with flat responses in all the frequency range of interest are used to convert with high accuracy the high voltages and currents to the relatively low voltages required by the digitizer inputs. The harmonic parameters of such waveforms and the electric power are estimated from the digitized data and the resulting estimates are compared with the readings of the device under calibration.

The reference measuring system comprises (see figure 1): an arbitrary waveform function generator with two synchronized channels, a power amplifier, a transconductance amplifier, a resistive voltage divider, a current shunt and a digitizer with two synchronized channels.

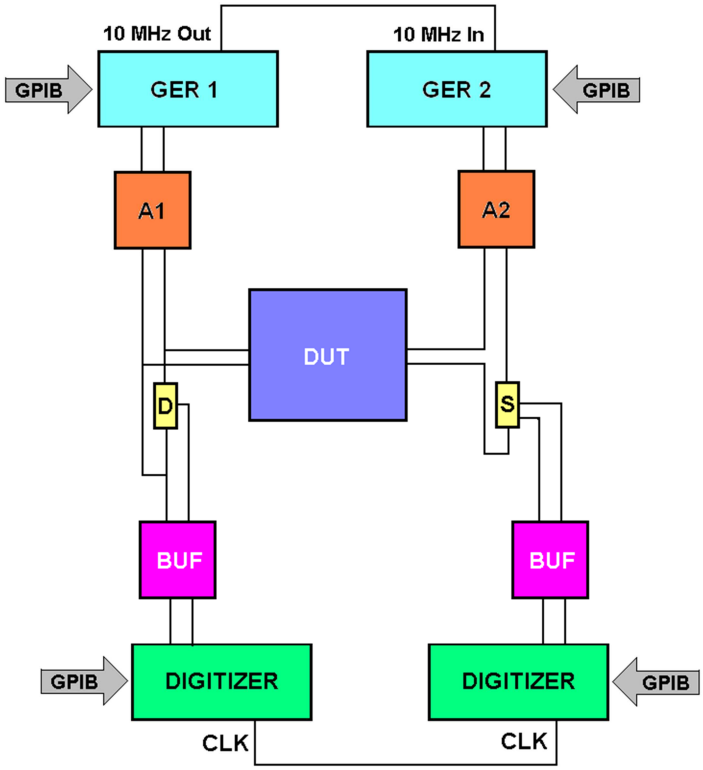

Figure 1. Simplified block diagram of the reference measuring system. (GER1 – channel 1 of the arbitrary waveform function generator, GER2 – channel 2 of the arbitrary waveform function generator, A1 – power amplifier, A2 – transconductance amplifier, D – resistive voltage divider, S – current shunt, BUF – buffer, DIGITIZER – two-channel digitizer, CLK – clock, and DUT – device under calibration)

2.1 Arbitrary waveform function generator

Arbitrary waveform function generators based on direct digital synthesis (DDS) present many advantages in comparison with other techniques. The DDS technique consists in the digital processing to generate signals at different frequencies and phases selectable by software from a reference clock. It shows a higher frequency resolution and a lower harmonic distortion than those obtained through other techniques (for instance, phase-locked loop). The frequency stability in the DDS technique depends only on the external reference oscillator employed, thus allowing multiple devices to be synchronized.

The design requirements are [1, 2, 3]: (a) two synchronized channels; (b) low total harmonic distortion: –80 dBc (@ 0.23 V, 1 kHz); (c) frequency resolution: 1.4 nHz; (d) frequency stability: 3.9 µHz (@ 0.23 V, 62.5 Hz, single-tone signal); (e) frequency stability: 25 µHz (@ 0.23 V, 1 kHz); (f) amplitude stability: 2.0 µV (@ 0.227902 V, 62.5 Hz, single-tone signal); (g) amplitude stability: 13 µV/V (@ 0.23 V, 1 kHz); (h) frequency range: DC to 150 kHz (with a slight increase in distortion); (i) internal reference clock: 400 kHz +/– 20 Hz; (j) output amplitude: 1 V, 2 V, 5 V and 10 V peak-to-

peak; (k) output signal waveforms: single-tone sinusoidal, two-tone sinusoidal, distorted sinusoidal, squarewave, triangular and saw-tooth.

The generator circuits are currently being designed by INTI. The circuit components will be purchased by Inmetro as soon as the component listing is defined.

2.2 Power amplifier

The power amplifier is used to boost the output of a channel of the dual-channel generator to a nominal of 120 V rms or 240 V rms. In addition, the amplifier is designed to supply up to 100-mA rms current to accommodate the burden requirements without causing any significant error. A prime goal is to maintain the excellent short-term amplitude and phase stability inherent in the digital generator. In addition, there is a general need for a precision power amplifier that will provide an output swing of several hundred volts at moderate power levels while maintaining good dc characteristics, stable gain, and wide bandwidth.

The design requirements are [4]: (a) voltage gain: 40 (nominal); (b) maximum output swing: +/– 485 V, (340 V rms); (c) maximum output current: +/– 145 mA, (100 mA rms); (d) frequency response: DC to 100 kHz, 3 dB (240 V rms, 100 mA rms); (e) load regulation: 20 ppm change (null load to full load @ 120 V rms, 1 kHz); (f) output noise: less than 50 mV rms (100 kHz bandwidth); (g) input impedance: 10 kΩ; (h) maximum slew rate: 400 V/μs.

The amplifier circuits are currently being designed by Inmetro. The circuit components will be purchased by Inmetro as soon as the component listing is defined.

2.3 Tranconductance amplifier

A transconductance amplifier ideally produces a current in a load proportional to an input voltage and maintains that current independent of the load terminal voltage. A total of 4 (four) transconductance amplifiers are being designed each covering the following ranges (full scale): 20 mA, 200 mA, 5 A, and 20 A.

The design requirements are [5, 6, 7]: (a) transconductance stability (10 min): +/– (0.005% reading + 0.005% range) @ 10 Hz to 10 kHz and +/– (0.010% reading + 0.010% range) @ 10 kHz to 100 kHz; (b) input voltage range (full scale): 5 V; (c) frequency range: 10 Hz to 100 kHz; (d) compliance voltage: 7 V rms; (e) total harmonic distortion: –60 dB @ 10 Hz to 10 kHz, –50 dB @ 10 kHz to 40 kHz, –40 dB @ 10 kHz to 100 kHz; (f) input impedance (differential input): 500 kΩ from each input terminal to chassis ground; (g) output impedance: 20 mA – 10 kΩ // 1.4 nF, 200 mA – 10 kΩ // 1.4 nF, 5 A – 10 kΩ // 30 nF, 20 A – 2.5 kΩ // 120 nF.

The transconductance amplifiers will contain only analog circuits to reduce electrical noise. Linear power supplies are utilized in all amplifiers except the one that covers the 20-A range also to reduce electrical noise. Vishay Z-Foil resistors (VTA) with TCR of ±0.05 ppm/°C are employed in critical circuit locations to increase the output stability of the amplifier.

The amplifier circuits were designed by Inmetro. The printed circuit board (PCB) layout has been started by Inmetro. The circuit components are currently being purchased by Inmetro.

2.4 Resistive voltage divider

There are 9 (nine) resistive voltage dividers to be used one at a time whose (binary) nominal value (from 4 V to 1024 V) depends on the test voltage selected [8]. An additional 1024-V divider is being also designed with different power consumption for evaluation purposes. The (binary) input resistances range from 1 kΩ @ 4 V to 256 kΩ @ 1024 V. Their input capacitance is always 33 pF. Thus the power amplifier output current is always 0.004 A. The divider output resistance is always 200 ohms. Thus the nominal output voltage of the dividers is always 0.8 V.

The rated voltages were selected with binary ratios to ease the step-up calibration of the amplitude and phase errors with the dual-channel digitizer and a standard binary inductive voltage divider. The nominal ranges of the dividers are obtained from the voltage ratios 5, 10, 20, 40, 80, 160, 320, 640, and 1280, and the 0.8-V output voltage.

To get high accuracy in all ranges of voltage and frequency, it is necessary that the divider behaves as a linear device. The most important nonlinear effect in voltage dividers is dielectric losses, The voltage dividers employ Vishay Z-Foil audio resistors (VAR) with low dissipation factor whose dissipated power in each resistor does not exceed 100 mW. It was confirmed by UTE that the nonlinear effects are reduced considerably by soldering such resistors on PTFE PCBs [8]. Such boards have a very low dissipation factor. Once nonlinear effects have been minimized, stray capacitances are the most relevant linear parasitic effect. In this work a different shielding technique for nulling radial electric fields is explored [8].

The voltage divider circuits were designed by UTE. The circuit components were purchased by Inmetro and transported to UTE. The PCB layout has been started by UTE.

2.5 Current shunt

There are 12 current shunts to be used one at a time whose nominal value (20 mA, 50 mA, 100 mA, 200 mA, 0.5 A, 1 A, 2 A, 5 A, 10 A, 20 A, 50 A and 100 A) depends on the test current selected [9, 10]. Their input resistances range from 40 Ω @ 20 mA to 0.008 ohm @ 100 A. Thus the nominal output voltage of the shunts is always 0.8 V.

The current shunts employ Vishay Z-Foil resistors (Z201) with TCR of ±0.05 ppm/°C whose dissipated power in each resistor does not exceed 0.33 W.

The current shunt circuits were designed by INTI and Inmetro. The circuit components were purchased by Inmetro and are waiting an authorization from Argentinian customs to be embarked to INTI. The PCB layout was finished by INTI and the PCBs are currently being manufactured in Brazil.

2.6 Dual-channel digitizer

A high-resolution, digital sampling system based on a Sigma-Delta analog-to-digital converter (Σ–Δ ADC) has been developed and characterized [11]. The system has been modified to accommodate two synchronized channels.

The "equivalent sampling rate (ESR)" is the frequency with which the samples are outputted. As the Σ–Δ ADC works through oversampling, ESR = *f*s/OSR, where *f*s is the clock frequency and OSR is the oversampling ratio. The ADC allows a maximum clock frequency of 20 MHz and an OSR between 32 and 256, that is, 20 MHz / 32 = 625 kHz is the maximum ESR.

The design requirements are [11]: (a) two synchronized channels; (b) dynamic regime - total harmonic distortion (THD): < −80 dBc (@ −51 dBFS (4.382 mV), 1 kHz); signal-to-noise ratio (SNR): > 55 dBc (@ −51 dBFS (4.382 mV), 1 kHz); signal-to-noise-plus-distortion ratio (SINAD): > 55 dBc; effective number of bits (ENOB): 16 bits; intermodulation distortion (IMD): < −75 dBc (@ −57 dBFS (2.180 mV), f_1 = 1 kHz and f_2 = 1.25 kHz); settling time: 24 samples or 375 μs (@ OSR = 256, ESR = 64 kHz); (c) stationary regime – noise referred to input (rms): < 10.25 LSB or 1.2 μV (@ ESR = 64 kHz); noise-free code resolution: 18 bits; (d) overall bandwidth of the digital sampling system (ADC + digital filters): 250 kHz; (e) input impedance: 10 MΩ // 60 pF; (f) other important characteristics: flat frequency response, high linearity, minimum temperature dependence, minimum dc offset, and auto-calibration.

The digitizer circuits were designed by INTI. The PCB layout has been started by INTI. The circuit components were purchased by Inmetro and will have been transported to INTI by the time this article is published.

3. Project management

The project is coordinated by Inmetro, who is responsible for the purchase and transportation of the components and parts needed to the construction of the modules, and for the transportation of the modules needed to the assembly of the measuring systems, in each partner country.

Inmetro is also responsible for the development of the wideband power and transconductance amplifiers and of new digital sampling algorithms. INTI is responsible for the development of the arbitrary waveform function generator, the dual-channel digitizer and the current shunts (and their

calibration). UTE is responsible for the development of the resistive voltage dividers (and their calibration).

The project activities include the design, layout and documentation of the printed circuit boards of the modules, the design and documentation of the electronic packaging of the modules, the calibration of resistive voltage dividers and current shunts, the design and documentation of the software and firmware, and the measuring system integration, testing and documentation.

Acknowledgments
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References

[1] Adad W 2010 *Investigación sobre la generación de señales arbitrarias por el método de síntesis digital directa para su aplicación a la metrología eléctrica*, Tese de Ingeniería, Facultad de Ingeniería, Universidad de Buenos Aires.
[2] Adad W and Iuzzolino R 2012 Arbitrary function generator using direct digital synthesis *CPEM Digest (Washington)* 622 ISBN 978-1-4673-0440-5
[3] Adad W and Iuzzolino R 2012 Low distortion signal generator based on direct digital synthesis for ADC characterization *ACTA IMEKO* **1** 59
[4] Laug O B 1987 A precision power amplifier for power/energy applications *IEEE Trans. Instrum. Meas.* **36** 994
[5] Laug O B 1985 A wide-band transconductance amplifier for current calibrations *IEEE Trans. Instrum. Meas.* **34** 639
[6] Laug O B 1996 A 100 A, 100 kHz transconductance amplier *IEEE Trans. Instrum. Meas.* **45** 440
[7] Hess D T and Clarke K K 1998 Evaluation of 100 Ampere, 100 kHz transconductance amplifiers *CPEM Digest (Washington)* 611
[8] Slomovitz D, Trigo L, Aristoy G, Brehm M and Kyriazis G A 2015 Wideband resistive voltage divider for a standard wattmeter *IOP Journal of Physics: Conference Series (JPCS) – this issue*.
[9] Yasuda E, Di Lillo L and Kyriazis G A 2015 Design and construction of new shunts for a wideband sampling wattmeter *Proc. Metrologia 2015 - XI SEMETRO (Bento Gonçalves)* ISBN 978-85-86768-10-1
[10] Rydler K -E and Tarasso V 2008 Extending ac-dc current transfer measurement to 100 A, 100 kHz *CPEM Digest (Boulder)* 28 ISBN 978-1-4244-2399-6
[11] Iuzzolino R 2011 *Josephson waveforms characterization of a Sigma-Delta Analog-to-digital converter for data acquisition in metrology*, Dr.-Ing. Dissertation, Technische Universität Braunschweig TU-BS Diss. ISBN 978-3-86387-095-9.