A Series-Parallel Switched Capacitor Step-Up DC-DC Converter and its Gate-Control Circuits for Over the Supply Rail Switches

Pablo Pérez-Nicoli, Pablo Castro, Fernando Silveira
Instituto de Ingeniería Eléctrica, Facultad de Ingeniería
Universidad de la República, Uruguay.
{pablop, pcastro, silveira}@fing.edu.uy

***Abstract*—An efficient control of the gate voltage of switches that operate outside the supply range is a problem that occurs in circuits such as step-up DC/DC converters and stimulation circuits for implantable devices. This paper proposes solutions to this problem, using as case study a 3x, ultra low-power, step-up DC/DC converter with series-parallel architecture. The proposed gate control strategy results in minimizing the gate swing of the switches and recycling of the gate charge in one of the cases, thus reducing the energy spent in driving the switch. The designed converter achieves an 84% simulated efficiency (without the control circuitry) @$V_{in} = 400mV$ and $5\mu A$ load current and operates down to $V_{in} = 200mV$.**

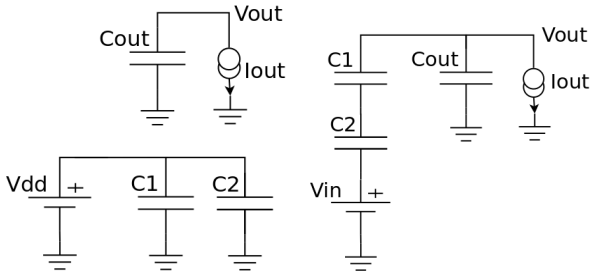
I. Introduction

Current portable devices are usually powered by batteries. In several applications such as smart sensors or biomedical implants, batteries not only limit the life of the device but also increase the size. Nowadays there are some devices which can harvest energy recharging their battery or just powering themselves. Different energy sources can be used like solar, mechanical, thermal or even natural potential differences which exist across a tree [1].

The voltage obtained from these sources is often lower than the needed for the circuit to work, so this kind of applications use a DC-DC converter to increase and stabilize the supply voltage.

This step-up DC-DC converter should be capable of start-up without any additional power source and work efficiently delivering at least some micro watts as many ultra low power applications have this consumption level, e.g. [2] proposes an intraocular pressure/temperature monitor that consumes $2.3\mu W$. Many converters have been developed trying to satisfy these specifications, which are difficult to fulfil having sub-threshold input voltage and achieving good efficiency with such low output power.

Inductor based converters reach very low start-up voltage but usually need external inductors and tend to generate higher electromagnetic radiated fields that could cause interference. [3] reaches a $35mV$ start-up voltage with 58% end-to-end efficiency while using external components. Light weight and small volume are also greatly important in many of these applications, so design of an all integrated converter has been the main goal of many works. This kind of converters generally use only capacitors to raise the voltage and most of them are based on the Dickson charge pump [4] converter. [5] presents an improved Dickson type charge pump which achieves a minimum start-up voltage of 270mV, however, a reasonable efficiency is obtained when the input voltage is over $350mV$ reaching a maximum efficiency of 65%. Another charge pump not so often used are series-Parallel, in [6] a series-Parallel charge pump is presented, the architecture there shown allows different conversions ratios.



(a) Phase 1 (b) Phase 2

Fig. 1. Series-parallel step-up DC-DC converter

Additionally the series-Parallel charge pump has traditionally been the main architecture for stimulation circuits in many implants, such as cardiac pacemakers ([7], [8], [9]), where an external, stimulation tank capacitor of some microFarads is charged to a voltage that may be higher than the battery voltage. Therefore the results presented in this work are also applicable in this context.

Either using a Dickson type charge pump architecture or a simple series-Parallel converter (Fig. 1), a key issue lies on how to design the switches [10]. The simplest use of an ordinary switch (Fig. 2) requires to have available a power supply equal to the highest voltage to be handled by the switch, i.e. it operates within the power supply rails. Otherwise it cannot be turned off and/or it will present a high impedance when it is on. NMOS and PMOS has different behaviours. PMOS gate has to be higher than both A and B node (Fig. 2) in order to turn it off, but can be easily turned on connecting its gate to ground. NMOS however, needs a voltage over A or B to be turned on while it is turned off just setting its gate to ground. Furthermore, the PMOS substrate connection must be connected to a voltage higher than A and B, in order to avoid direct conduction of the drain-substrate or source-substrate junctions. As a result, ordinary switches cannot be driven from the input voltage on a step-up converter.

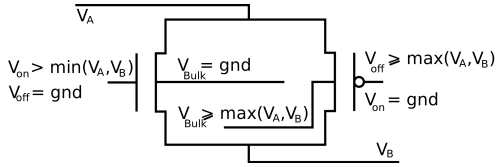


Fig. 2. Ordinary switch voltage ranges. V_A and V_B are supposed to be above ground. Conditions consider also conduction in weak inversion (sub-threshold) regime.

Ordinary switches can be used in a step-up converter only if an auxiliary step up converter is applied or if the drive circuits are supplied from the output voltage. The first alternative, auxiliary step-up, presents an efficiency problem while the latter will need energy stored or an additional circuit or a mechanism to assure start-up. Some alternatives of the first type have been proposed, [11] shows a bootstrapped gate transfer switch which elevates the power switch gate using several transistors. Dickson type charge pumps, initially used diodes, nowadays ad-hoc connections are made using the internal charge pump nodes [12] [13] to turn on and off each switch. These ad-hoc connections are all actually based on the gate control strategies described in [14]. Some works combine ordinary switches supplied from the output voltage with others connected in parallel to start-up [5]. All these different architectures are basically trying to solve the same problem: to be able to guarantee effective turn on and off of the switches.

This work present a step-up DC-DC converter that multiplies by three the supply voltage, based on series-parallel architecture (Fig. 1). The switches presented apply the same general structure as in [14], but specialized for the context of series-Parallel converters architecture. They are driven from the input voltage and do not need an auxiliary charge pump. Their design improves the efficiency by recycling charge and optimizing the gate swing. The converter can start-up with the load connected without any extra mechanism.

The paper is organised as follows. Section II presents the series-parallel architecture studying the requirements of each switch. In Section III the proposed switches are presented. Simulation result and comparisons with others works can be found in Section IV. Finally, Section V summarizes the main conclusions.

II. Series-parallel Architecture

Fig. 3 shows the architecture of a series-Parallel x3 step-up converter. In Phase 1 (Fig. 1(a)), when charge is taken from the source, $SWVdd1,2$ and $SWgnd_{1,2}$ are turned on while $SWi_{1,2}$ and $SWVout$ are turned off. On Phase 2 Fig. 1(b), charge is being delivered to the load, $SWVdd1,2$ and $SWgnd_{1,2}$ are turned off whereas $SWi_{1,2}$ and $SWVout$ are turned on. Therefore, just two signals are needed to control the switches, one drives $SWgnd_{1,2}$ and $SWVdd1,2$ while the other drives $SWi_{1,2}$ and $SWVout$. In order to avoid short circuits, these two signals must be non-overlapping.

In order to define the requirements of the drive signal for each switch, Table I shows the maximum (which is the worst case) terminal voltages (A and B nodes) (Fig. 3) of each switch in both Phases. In some cases (e.g. terminal B of $SWgnd_1$ in Phase 1) this maximum value occurs at the start of the Phase. If $SWgnd_1$ is implemented by a NMOS, it can be easily turned off by setting its gate to gnd in any situation and is possible to turn it on using Vdd as node A is lower ($V_A = gnd$ see Table I). Using the same argument $SWgnd_2$ can be also implemented by a single NMOS, therefore a special design for these switches is not necessary.

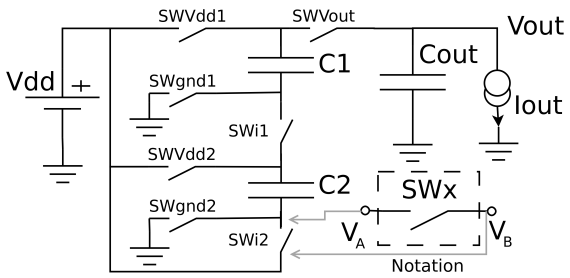


Fig. 3. Series-Parallel step-up x3 converter

Table I indicate that $SWi_{1,2}$ can be implemented using one transistor too. In this case, a PMOS fulfils the requirements as it can be turned off connecting its gate to Vdd ($V_A = gnd$, $V_B = Vdd$ see Table I). As it was explained before, to turn it on is not a problem. The substrate can be connected to B node (the bottom node Fig. 3) since this node is always higher than A.

Consequently, the only switches whose design is tricky are $SWVdd_{1,2}$ and $SWVout$ and they are studied in Section III

TABLE I. Switch terminals maximum voltages

	Phase 1			Phase 2		
Switch	State	A	B	State	A	B
$SWgnd_1$	ON	gnd	2Vdd	OFF	gnd	2Vdd
$SWgnd_2$	ON	gnd	Vdd	OFF	gnd	Vdd
$SWVdd_1$	ON	Vdd	Vdd	OFF	Vdd	3Vdd
$SWVdd_2$	ON	Vdd	Vdd	OFF	Vdd	2Vdd
$SWVout$	OFF	Vdd	3Vdd	ON	3Vdd	3Vdd
SWi_1	OFF	gnd	Vdd	ON	2Vdd	2Vdd
SWi_2	OFF	gnd	Vdd	ON	Vdd	Vdd

III. Switches Design

Firstly, the design of $SWVdd_{1,2}$ is detailed as it is easier to understand. Then in Section III-B the most challenging switch, $SWVout$, is analysed. The proposed architecture have the following features: it recycles the $SWVout$ gate charge, thus reducing losses. Losses are further decreased by minimizing the gate swing for both switches, since the lowest possible voltage is used to turn them off.

A. Switches to V_{dd}

The proposed switch for $SWVdd_{1,2}$ is depicted in Fig. 4. The power transistor is $M1$ while $M2$ and $M3$ drive $M1$ gate. When $Vin = Vdd$, $M3$ discharges the $M1$ gate, thus turning it on. As in this Phase B node is lower than Vdd (Table I), $M2$ remains off. Therefore, B node is charged to Vdd in this cycle.

At the end of Phase 1, switches $SWVdd_{1,2}$ and $SWgnd_{1,2}$ are turned off before $SWi_{1,2}$ and $SWVout$ have been turned

on. Firstly, when $Vin = gnd$, $M2$ charges $M1$ gate to the voltage available in node B, thus $M1$ is now working as a diode. Then, after $SWi_{1,2}$ are turned on, B node increase but the $M1$ connection prevent this charge from coming back to the source. If the chosen working frequency causes that B node is not completely charged during Phase 1, charge may go through $SWVdd_{1,2}$ even during Phase 2 (from A to B) until the steady state is achieved. However, instead of being a problem, this behaviour makes the output node to rise faster, as charge is being taken from the source in both phases during the transient state.

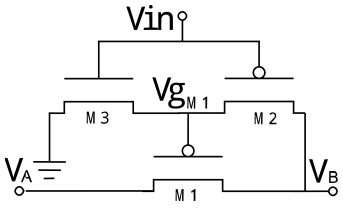


Fig. 4. Proposed switch for $SWVdd_{1,2}$

Although two extra transistor have been added to set up the switch, its extra parasitic capacitances do not affect the converter efficiency as an inverter chain has to be implemented anyway to control the $M1$ gate. Vin node has lower capacitance than Vg_{M1} since $M2$ and $M3$ can be smaller than $M1$. As can be noticed, the $M1$ gate is always at the minimum voltage necessary to be off, reducing its swing and improving the efficiency.

B. Switch to V_{out}

First we are going to analyse why the switch designed to $SWVdd_{1,2}$ cannot be used to implement $SWVout$. If the switch shown in Fig. 4 is being used for $SWVout$, $M2$ will be never off as its maximum Vg ($Vin = Vdd = Vg_{M2}$) is lower than node B ($3Vdd$, the output node). Consequently, in Phase 2 when it is on, the node B will be discharged to ground through $M2$ and $M3$.

In order to avoid this problem, the gate of $M2$ is connected to node A as is shown in Fig. 5. For the time being, assume that Vin is driven by the logic and node D is connected to ground. $SWVout$ is turned on only when V_A is higher than V_B, otherwise the output node (V_B) will be discharged. Therefore, when $SWVout$ is on ($Vin = Vdd$), $M2$ remains off as $V_A > V_B$ and there is not a direct path from the output node to ground like in the case described before.

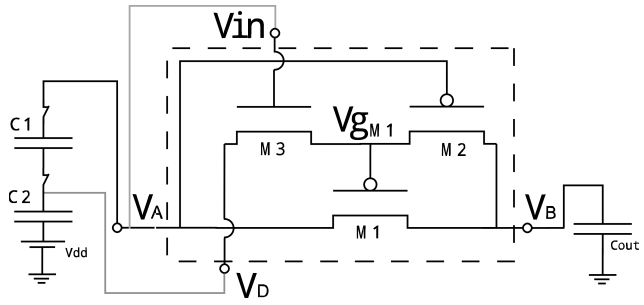


Fig. 5. Proposed switch for $SWVout$

At the end of Phase 2, $V_A \simeq V_B$ and Vin is set to ground so $M3$ turns off, hence Vg_{M1} remains discharged but now floating. When the Phase 1 starts again, V_A of $SWVout$ decrease, turning on $M2$ ($V_A < V_B$) and charging $M1$ gate, thus $SWVout$ is off as it was desired.

The charge used to drive $M1$ gate can be reused by connecting Vin and V_D as is shown in Fig. 5. So during Phase 1 $M3$ is off ($Vin = V_D = Vdd < Vg_{M1} = 3Vdd$) and $M2$ in on ($Vg_{M2} = V_A = Vdd < V_B = V_{out} = 3Vdd$), as a result $SWVout$ is off ($Vg_{M1} = Vout = 3Vdd$). At Phase 2, $M3$ is on ($Vg_{M3} = 3Vdd > V_D = 2Vdd$) and Vg_{M1} is discharged to $2Vdd$ so $M1$ is turned on since V_A and V_B are higher ($V_A = V_B = 3Vdd$ see Table I). The sequence described is shown in Fig. 6. Summarizing, Vg_{M1} will vary between $2Vdd$ and $3Vdd$. Instead of dumping the M1 gate charge to ground each time that Vg_{M1} changes from $3Vdd$ to $2Vdd$, this charge is used to refill C2. Therefore, $SWVout$ is self-controlled and its gate charge recycled.

It is worth noting that in the case of switches $SWVdd_{1,2}$ the gate charge cannot be recycled since the gate node needs to be at ground in order to turn the switch on.

In switches $SWVdd_{1,2}$ and $SWVout$, the NMOS and PMOS substrates are connected to ground and the V_B node, respectively.

Using the proposed switches, any integer step-up level can be achieved just changing the number of capacitors used. With additional $SWVout$ switches, a multiple output converter can also be implemented.

IV. Simulation Results

The proposed step-up DC-DC converter was simulated in a $130nm$ CMOS twin-well technology, the result proves that the switches are working as desired. The performance achieved by the converter is compared with the state of art in Table II.

In order to demonstrate the behaviour of $SWVout$, Fig. 6 shows the simulated signals V_A, V_B, V_D and Vg_{M1}. This simulation was done with $Vdd = 400mV$, a switching frequency of $1MHz$ (selected by simulation to achieve maximum efficiency) and an output current of $5\mu A$. The total capacitance used was $600pF$. As can be seen in Fig. 6 the output voltage is almost $1.1V$. The efficiency simulated was 84%, although the non-overlapping pulse generator power consumption was not considered, the gate parasitic capacitance switching loss of all transistors was took into account. The design of the non-overlapping signal generator is out of the scope of this work and two ideal non-overlapping pulses were used for the logic signals that control the converter. If the non-overlapping pulse generator is considered, the efficiency is not significantly affected: in [15] we proposed a non-overlapping pulse generator which consume $284nW$ at $1MHz$ (with $Vdd = 1.2V$). [5] shows an example of ring oscillator clock generator operating at Vdd down to $270mV$.

Another important issue is the start-up voltage. To reduce this some works add boost converters, use low V_{th} transistors or even mechanical mechanisms. None of these methods was used, however, the proposed converter presents low start-up voltage as is shown in Table II.

TABLE II. COMPARISON WITH THE STATE OF ART

Reference	[3]	[12]	[13]	[16]	[5]	This work
Technology (CMOS)	$350\ nm$	$130\ nm$	$180\ nm$	$250\ nm$	$130nm$	$130nm$
Start-up voltage	$35mV$	$125mV$	$700mV$	$300mV$	$270mV$	$200mV$
External component	INDUCTOR	NO	NO	NO	NO	NO
Output voltage	$1.8V$	$\simeq 350mV$	$1.5V$	$3.2V$	$1.4V$	$1.07V$ (x3) $@V_{in} = 400mV$ $@5\mu A$ $500mV$ (x3) $@V_{in} = 200mV$ $@100nA$
Output power/current	$\simeq 300\mu W$ $@V_{in} = 100mV$	$100nA$	$4\mu A$	$1\mu W$	$5\mu A\ @V_{in} = 450mV$	$5\mu A\ @V_{in} = 400mV$ $100nA\ @V_{in} = 200mV$
Switching frequency	$28.4KHz$	$360KHz$	$5MHz$	$1MHz$	$800KHz$	$1MHz\ @V_{in} = 400mV$ $50KHz\ @V_{in} = 200mV$
Maximun efficiency	58%	62%	55%	68%	$65\%\ @V_{in} = 450mV$	$84\%\ @V_{in} = 400mV$ $@5\mu A$ $67.5\%\ @V_{in} = 200mV$ $@100nA$

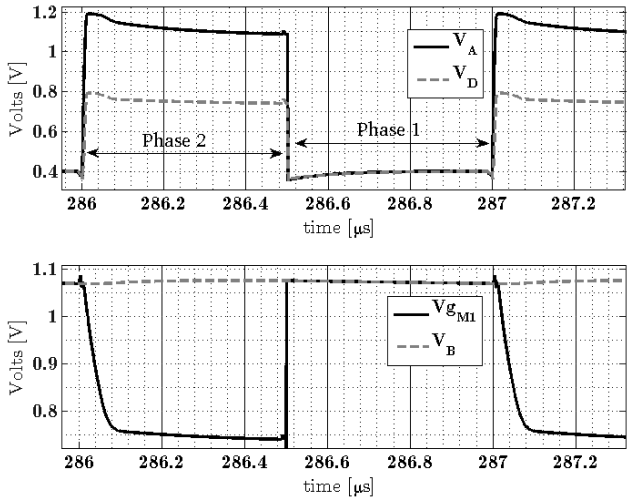


Fig. 6. Simulated signals of $SWVout$

V. CONCLUSIONS

The design of the gate control strategy for switches operating above the power supply rail has been presented in the particular case study of a series - parallel, 3x, ultra low power, step-up DC/DC converter. A systematic procedure for identifying the requirements of each switch has been first presented. Then the switches that required special solutions have been addressed. It has been shown how, starting from a basic structure, the gate and drain-source terminal voltages of the auxiliary switches can be handled so that the gate swing of the main switch is minimized, thus saving energy. Additionally, the gate charge of the main transistor in one of the proposed switches is recycled, thus providing further energy savings. The designed converter was shown to operate correctly in simulation, achieving an 84% simulated efficiency (without the control circuitry) $@V_{in} = 400mV$ and $5\mu A$ load current and operating down to $V_{in} = 200mV$.

VI. ACKNOWLEDGMENTS

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