Integrated programmable analog front-end architecture for physiological signal acquisition

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***Abstract*—A versatile front-end capable of acquiring a wide range of physiological signals, thus reusing the same design and hardware in different contexts, is a valuable goal both for biomedical research and medical devices. In this work we present such an "all-terrain" programmable integrated front-end architecture and the trade-offs associated to its design. A low noise preamplifier is implemented using a novel architecture based on a differential-difference amplifier which applies gm-C techniques for fixing the cut-off frequencies. Moreover, this architecture is extended to be applied to the other stages of the front-end. The main design trade-offs (noise-power, gain-power, noise-gain and linearity-gain) of the front-end architecture are discussed and their impacts in the design of the processing chain in terms of assignment of gain, noise, linearity and programmability to each stage are shown. The front-end is designed in a $0.5\mu m$ CMOS process. The gain is programmable between $57dB$ and $99dB$, the high cut-off frequency is programmable between $116Hz$ and $5.2kHz$, the low cut-off frequency is $18Hz$, the maximum power consumption of the front-end is $11.2\mu A$ and its maximum equivalent input-referred noise voltage is $1.87\mu V_{rms}$.**

***Index Terms*—ultra-low-power, bio-potential acquisition, neural front-end.**

I. Introduction

In the last decade we have seen a significant growth of research and potential applications of electronic circuits that interact with the nervous system, both for research in neuroscience and for medical purposes. The main technical challenge that presents acquiring and processing these neural signals is to observe a high number of channels, while maintaining a low-noise ultra-low-power operation. Besides, this has several additional challenges. First, high CMRR is required in order to block higher level of surrounding signals such as mioelectric signals and electromagnetic interference. Second, high time constants need to be integrated within reasonable silicon area. Third, input DC values much higher than the signal levels must be blocked.

If the capability of acquiring different kinds of neural signals is joined with the acquisition of other biopotentials, a powerful tool is obtained. This tool can be applied for biomedical research and for reconfigurable medical devices for portable physiological signal acquisition.

In this work we present an integrated programmable analog front-end architecture focused in acquiring a wide range of physiological signals, such as Electrooculogram (EOG), Electroencephalogram (EEG), Electromyogram (EMG) and Auditory Evoked Potentials, among others. The amplitude of these signals ranges from $10\mu V_{PP}$ to $1mV_{PP}$ and its bandwidth ranges from $0.1Hz$ to $5kHz$. In addition, to correctly acquire these signals, high $CMRR$ (greater than $80dB$) and ultra-low-power operation must be guaranteed (the state-of-the-art supply current of neural front-ends is around $12\mu A$ at supply voltages ranging from $3.3V$ down to $1.0V$, see Table II).

The trade-offs and solutions when complying with the programmability, gain, noise and power consumption requirements, as well as accommodating the signal ranges along the processing chain, are addressed in this paper.

The low noise preamplifier was implemented using a novel architecture based on a differential-difference amplifier (DDA) [1] proposed in [2], which applies gm-C techniques for fixing the cut-off frequencies. In this work this architecture is also extended to be applied to the other filtering/gain stages of the front-end.

The performance achieved by relevant prior works that implement complete front-ends [3]–[8], which reach high gain (greater than 65 dB) and cover the desired bandwidth, are compared with our work in Table II. However, these works, unlike the present work, do not address the design process to define the architecture. [9] considers similar front-end specs, except for the ultra low power requirement.

II. Architecture

The proposed neural front-end consists of three stages (see Fig. 1). In the first place, a low-noise ultra-low-power preamplifier. In the second place, a programmable band-pass filter. Finally, a low-gain high-linear-range output filter. Why this is a suitable solution will come up once the main trade-offs in the processing chain design are presented in next subsections.

A DDA-based architecture originally proposed for neural preamplifiers [2] was used to implement the three stages (see Fig. 2). This low-noise ultra-low-power architecture presents high CMRR and offers a well-controlled low cut-off frequency (since this frequency is not determined by highly variable MOS-bipolar high valued pseudo-resistors [9]). The low cut-off frequency is fixed by means of a novel local feedback loop at the output [2].

Gm2 and Gmf are symmetrical OTAs (Operational Transconductance Amplifier) whose respective transconduc-

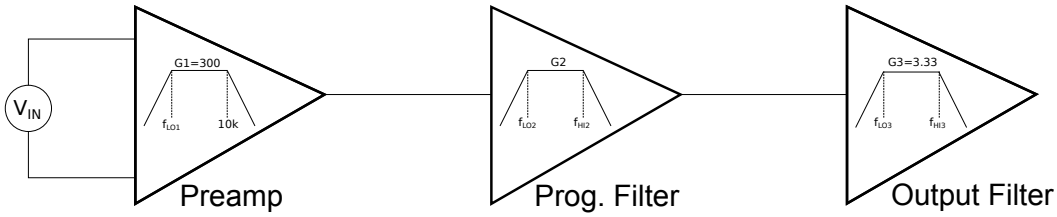

Fig. 1. Front-end block diagram.

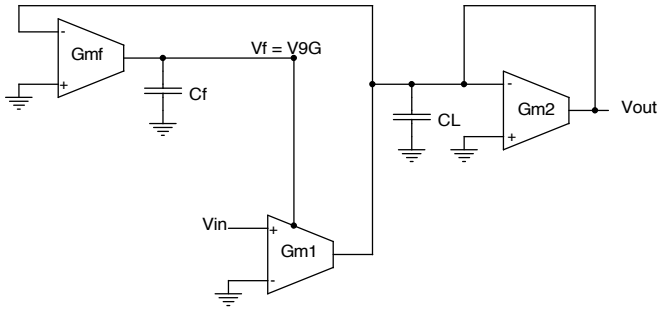

Fig. 2. Circuit architecture.

tance are G_{m2} and G_{mf}. Gm1 is a special 3-input OTA (the third input is for the local feedback loop at the output for DC control) with the following transfer function:

$$i_{Gm1,OUT} = G_{m1} v_{IN} + 2 g_{mC} v_f \tag{1}$$

where G_{m1} is the Gm1 transconductance and g_{mC} is an internal parameter.

It can be shown that the circuit depicted in Fig. 2 has a first-order band-pass transfer function where the high cut-off frequency f_{high}, the band-pass gain G and the low cut-off frequency f_{low} are given by:

$$f_{high} = \frac{G_{m2}}{2\pi C_L} \tag{2}$$

$$G = \frac{G_{m1}}{G_{m2}} \tag{3}$$

$$f_{low} = \frac{2 g_{mC}}{G_{m2}} \frac{G_{mf}}{2\pi C_f} \tag{4}$$

In [2] it is shown that the input-referred noise power spectral density S_{ni}^{total} is:

$$S_{ni}^{total} = \frac{2\gamma n k T}{G_{m1}} A \tag{5}$$

where n is the slope factor of the MOS transistor sub-threshold region, $\gamma = 2$ in weak inversion and $\gamma = 8/3$ in strong inversion, k is the Boltzmann constant, T is the absolute temperature and A is a factor that depends on the transconductance over drain current ratio (g_m/I_D) of transistors of Gm1 (the input differential pair and the current mirror transistors).

In order to evaluate the trade-off between power consumption and noise, the NEF (Noise Efficiency Factor) introduced by [10] is used:

$$NEF = v_{ni} \sqrt{\frac{I_{DD}}{2k\pi T U_T BW}} \tag{6}$$

where v_{ni} is the input-referred noise voltage, I_{DD} is the total supply current, BW is the bandwidth, $U_T = kT/q$ is the thermal voltage and q is the electron charge. An amplifier using a single bipolar transistor will present a $NEF = 1$, which is a lower bound for MOS amplifiers. We will use this figure of merit because it is a *de facto* standard for neural amplifiers, but it must be noticed that it takes into account only the thermal noise, therefore any effort focused in reducing low frequency noise (i.e. Flicker noise) will not be reflected in the NEF since the BW will remain constant.

In the next subsections we will discuss the main trade-offs that this architecture, the application's specifications and the technology present.

A. Noise Gain trade-off

In order to reduce the noise requirement of the second stage it is desirable to have a high gain in the first stage. Therefore, the noise requirement will define the preamplifier gain. If the preamplifier input-referred noise voltage has to be $v_{ni1} = 2\mu V_{rms}$, then its output-referred noise voltage will be $v_{no1} = G_1.2\mu V_{rms}$, where G_1 is the preamplifier gain (and in general G_i is the gain of the ith stage). The preamplifier is one of the main contributors to consumption due to its low noise requirement. Therefore, to reduce consumption, we should enable the second stage to have higher noise. If we choose that the input-referred noise voltage of the second stage has to be $v_{ni2} = 0.25mV_{rms}$, and we impose that the noise contribution of the second stage adds only a 10% to the noise given by the first stage in the total input-referred noise voltage v_{ni2}^{total}, then we have:

$$v_{ni2}^{total} = \sqrt{v_{no1}^2 + v_{ni2}^2} < 1,1 v_{no1} \tag{7}$$

Thus,

$$v_{ni2} < 0,92 G_1 \mu V_{rms} \Rightarrow G_1 > 1,09 v_{ni2} = 273 V/V \quad (8)$$

B. Linearity Gain trade-off

Our ultra-low-power architecture uses transconductors instead of operational amplifiers. This approach is very advantageous in terms of power consumption but faces linearity problems. A transconductor with a standard input differential pair will not be able to handle an input signal much higher than $300mV_{PP}$.

Therefore, if the input signal ranges from $10\mu V_{PP}$ to $1mV_{PP}$, the preamplifier gain G_1 should be less or equal to $300V/V$. This will ensure that the signal amplitude at the preamplifier output will be less or equal to $300mV_{PP}$ (observe in Fig. 2 that the inputs of Gm2 and Gmf are connected to the preamplifier ouput).

Moreover, the same restriction will apply to the second stage. If $G_1 = 300V/V$, the signals at the programmable filter input ranges from $3mV_{PP}$ to $300mV_{PP}$. In order to assure that the signal amplitude remains below $300mV_{PP}$, the programmable gain G_2 will have to vary between $1V/V$ (for the signals in the $300mV_{PP}$ range) and $100V/V$ (for the $3mV_{PP}$ signals).

C. Transconductance value and Programmability constraints

It can be seen from Eqs. 2, 3 and 4 that in order to program the gain we need to vary the transconductance values, and possibly also the capacitor values, to program the cut-off frequencies. In order to vary the transconductance value we may vary the bias current of the transconductor or we may modify the internal structure of the transconductor (e.g. vary a current mirror gain factor).

According to Eq. 2, given $C_L = 2pF$, in order to vary f_{high} between $100Hz$ and $5kHz$, Gm2 has to vary between $1,3nS$ and $63nS$. Thus, Gm2 has to vary by a factor of 50. This cannot be done by just modifying the Gm2 bias current because the Gm2 input differential needs to be biased in strong inversion to provide the required linearity and if we change the bias current by a factor of 50 either the differential pair will no longer be in strong inversion or the DC voltages (VGS, VDSAT) will vary too much. In the meantime, if G_2 has to vary between $1V/V$ and $100V/V$, according to Eq. 3, Gm1 must vary between $1,3nS$ and $6.3\mu S$. This means that Gm1 has to vary by a factor of 5000. Achieving these large factors can be a problem, in section III we present how these challenges were addressed.

D. Capacitor size constraints

According to Eq. 4, in order to achieve sub-1Hz low cut-off frequencies it is necessary to work with sub-nS OTA [11] as well as to use relatively large capacitors ($200 - 300pF$).

III. Implementation

The balance between the constraints and trade-offs presented in the previous section led lo the following design decisions. The programming is performed in the intermediate stage, where it is not necessary to filter very small signal amplitudes (and thus the noise is no longer a major problem) nor very large signal amplitudes (where the linearity starts to be a problem). The preamplifier has a $G_1 = 50dB$ fixed gain. The gain of the second stage (G_2) can be programmed between $0dB$ and $40dB$ and the high cut-off frequency between $100Hz$ and $5kHz$. The output filter has a $G_3 = 10dB$ fixed gain, so its linear range at the output should be $1V_{PP}$.

In order to program the gain and the upper cut-off frequency of the programmable filter we designed a *Base Filter* with the maximum gain ($G = 40dB$) and the maximum desired high cut-off frequency ($f_{high} = 5kHz$). The first and third stage were designed to have a cut-off frequency higher than $f_{high} = 5kHz$ in order to warrant that the whole processing chain can reach a $f_{high} = 5kHz$.

We implemented two mechanisms to program the gain of the Base Filter. First, a *rough tuning* was implemented by modifying the copy factor at the output current mirror of Gm1 (this allows to divide Gm1 by 10 or 100). Second, a *fine tuning* was achieved by varying the Gm1 Bias current (this permits to divide Gm1 continuously by up to 8 times). The high cut-off frequency was programmed varying the value of C_L. This was done by connecting in parallel (by means of switches) various integrated capacitors of different values in order to obtain 8 discrete values of C_L.

Table I presents the main parameters of the front-end transconductors.

TABLE I
FRONT-END MAIN PARAMETERS

	Preamp	Base Filter (Prog.)	Output filter
G_{m1}	$100\mu S$	$6.3\mu S$	$523nS$
G_{m2}	$320nS$	$63nS$	$157nS$
G_{mf}	$1.2nS$	$1.9nS$	$5.7nS$
g_{mC}	$360nS$	$158nS$	$53nS$
C_L	$5pF$	$2pF$	$2pF$
C_f	$47pF$	$300pF$	$300pF$

For the higher upper cut-off frequency f_{high} ($5kHz$) the Flicker noise effect is negligible compared to the contribution of thermal noise (the same behavior has been reported in [12]). For the lower f_{high} (around $100Hz$), the effect of the Flicker noise was taken into account adjusting the size of the transistors of Gm1 (for example by increasing the width W and the length L while keeping the ratio W/L constant in order not to modify the inversion level).

IV. Results

Montecarlo simulations (500 runs, process and mismatch) of the frequency response were performed on the four corners that arise from programming the gain and the high cut-off frequency f_{high}.

Fig. 3 depicts the transistor level Montecarlo simulations of the front-end frequency response for maximum G and minimum f_{high}.

Fig. 4 depicts the transistor level Montecarlo simulations of the front-end frequency response for maximum G and maximum f_{high}.

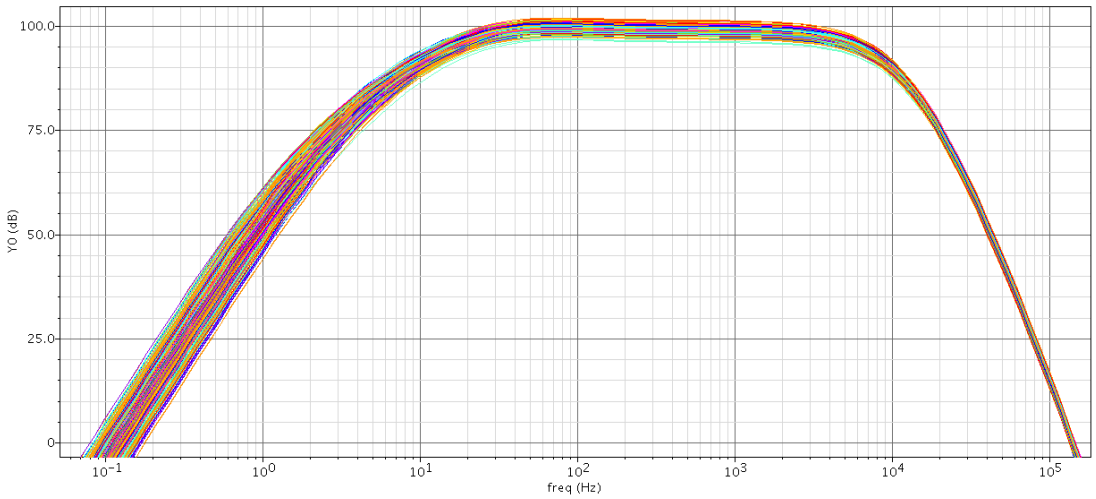

Fig. 4. Montecarlo simulations of the front-end frequency response for maximum G and maximum f_{high}.

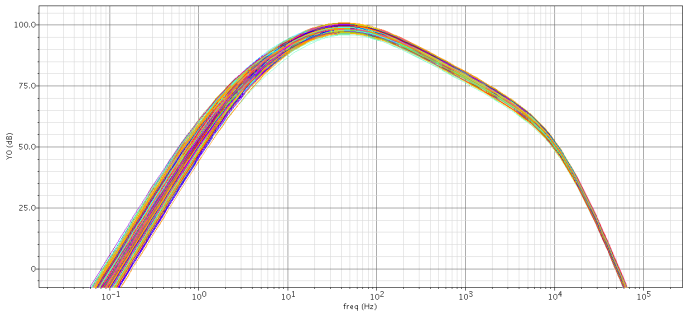

Fig. 3. Montecarlo simulations of the front-end frequency response for maximum G and minimum f_{high}.

Simulation results show that the front-end gain is programmable between $57dB$ and $99dB$, the upper cut-off frequency is programmable between $116Hz$ and $5.2kHz$. The maximum power consumption of the front-end is $11.2\mu A$ and its maximum equivalent input-referred noise voltage is $1.87\mu V_{rms}$. The front-end presents a good linearity achieving an output swing of $950mV_{pp}$ with a $THD = 4.8\%$. Moreover, the front-end configured for the maximum gain ($99dB$) and the maximum upper cut-off frequency ($5.2kHz$), has a consumption of $11.2\mu A$ and its equivalent input-referred noise voltage is $1.46\ muV_{rms}$, which corresponds to a $NEF = 2.61$. It also has a $CMRR_{typical} = 82dB$ and a low cut-off frequency of $20Hz$ (with fully integrated capacitors).

In Table II the performance of our design (at maximum f_{high}) is compared with some state of the art designs that provide high gain (greater than $65dB$) and cover the desired bandwidth. Except for the 2004 work of Nicolelis et al. [3] that uses discrete components, the rest of the references are implemented on IC, most of them in technologies with smaller minimum transistor length (therefore the effect of parasitic capacitors at high frequency will be more significant in our chip). Not all of them have the capability to program the high cut-off frequency.

The data shows that our front-end has the greater value of gain, equaling the best NEF reported and presenting an excellent performance in the other features required by the application.

V. Conclusions

The most important contribution of this work is to have applied a novel architecture to the design of a complete programmable front-end.

The main design trade-offs (noise-power, gain-power, noise-gain and linearity-gain) of the front-end architecture were discussed and their impacts in the design of the processing chain in terms of assignment of gain, noise, linearity and programmability to each stage were shown.

Noise is the most critical requirement of the first stage because ultra-low-amplitude signals must be amplified and filtered. Therefore, the noise-power trade-off, expressed in terms of the NEF, led us to assign most of the power budget to the first stage. Furthermore, the noise-gain trade-off and linearity-gain trade-off determined the gains of the first and second stage. Moreover, it was shown that programming wide ranges of gain and/or cut-off frequencies implies wide ranges of transconductance values and high capacitor values. Finally, we presented how these challenges can be addressed.

The integrated programmable analog front-end architecture presented is focused in acquiring a wide range of physiological signals (*all-terrain front-end*). This can be done because the gain is programmable between $57dB$ and $99dB$, and the upper cut-off frequency is programmable between $116Hz$ and $5.2kHz$, while the maximum power consumption of the front-end is $11.2\mu A$ and its maximum equivalent input-referred noise voltage is $1.87\mu V_{rms}$.

The comparison between our front-end and other works in the state-of-the-art shows that our front-end has greater value of gain, equaling the best NEF reported and presenting an

TABLE II
STATE OF THE ART COMPARISON.

	[3]	[4]	[5]	[6]	[7]	[8]	This work
Technology (μm)	Discrete	0.13	0.5	0.18	0.25	0.13	0.5
Max. Gain (dB)	93.4	77.6	78.0	66.0	79.8	65.5	99.3
Min. Gain (dB)	69.4	42.8	67.8	49.0	52.4	47.5	58.1
f_{high} (kHz)	6.5	10.0	8.0	11.7	8.9	6.9	5.2
$f_{low}(Hz)$	445	300	10	350	100	167	18
Supply current (μA)	3170	75	25	11.1	3.67	1.9	11.2
Input-referred noise (μV_{rms})	1.0	1.95	4.32	5.4	6.67	3.8	1.46
NEF	28.0	6.60	8.32	6.53	5.29	2.46	2.61
$CMRR_{worstcase}(dB)$	39	NR	NR	NR	NR	NR	66
$CMRR_{typical}(dB)$	42	63	-	66	62	83	82
f_{high} programmable (kHz)	No	No	No	No	$1-8.9$	$4.8-9.8$	$0.1-5.2$
f_{low} programmable (Hz)	No	No	$100-1000$	No	$4-1200$	$12-167$	No
THD 1% (mV_{pp})		1					483

excellent performance in the other features required by the application.

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