Power Estimations vs. Power Measurements in Spartan-6 Devices

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***Abstract*—Experimental measurements of power consumption for core logic of a 45-nm Spartan-6 FPGA and the comparison with the values predicted by the power estimation tool are presented. The measurement setup, benchmark suite, and EDA flows utilized to obtain power estimations are described. Several types of multipliers implemented in both LUTs and embedded blocks have been utilized as case-studies. They include versions with different levels of pipelining. In addition, a set of actual circuits obtained from OpenCores is analyzed. Main results of power estimations errors are presented and compared.**

Keywords—low-power; power measurements; power estimations

I. INTRODUCTION

Since first introduced in the mid-80s, the focus of research on FPGA architecture and CAD tools has been centered on improving area and speed. But, in recent years, with the growth of portable applications, there has been an increasing interest in power efficiency. The development of power consumption estimation tools and its integration to commercial and academic EDA packages is relatively recent: Xilinx announced Xpower in December 2000 [1], Altera introduced PowerPlay in 2004 [2], and in 2002 a power model was integrated to the VPR tool which is commonly employed by the research community [3].

Among the three main physical features that determine a circuit, area, speed and power consumption, the last one presents more difficulties for its estimation. There are mainly two reasons for that. First, power consumption depends on each circuit node's activity; so, its value depends on the input vectors. For example, a state-machine can receive thousands of data and remain in an idle state, while a particular sequence of a few bits can move it from one state to another. The second source of error in power estimation comes from the spurious transitions or glitches. Its propagation on a combinatorial circuit strongly increases the activity on most of the nodes of the circuit, and therefore the power consumption.

In this paper, we continue an analysis of the accuracy of power estimation tools for FPGAs. This work is the second part of the study. First experiments [4] were focused on a Cyclone_III chip and Altera tools. In the present paper, the analysis is extended to Xpower Power Analyzer and actual measurements in a 45-nm Spartan-6 Xilinx device.

The remainder of the paper is organized as follows: Section II describes previous works. The experimental part is detailed in Section III, including the measurement setup, the benchmark circuits and the EDA flows utilized to obtain estimations. In Section IV, results are presented and analyzed. Finally, main conclusions are summarized in Section V.

II. RELATED WORKS

Several works have reported direct on-board power measurements and compared them with low or high level estimation tools. For example, early measurements in Xilinx XC4000 families were reported in [5]. In [6], dynamic power consumption was analyzed for Virtex II devices, defining three factors that contribute to total power dissipation: capacitance, resource utilization, and switching activity. Comparisons of power measurements and power estimations with Xpower of different dynamically reconfigured applications in Virtex devices were shown in [7]. A similar study between Xpower and PowerPlay was done in [8].

A technique for early estimation of FPGA dynamic power consumption was presented in [9]. Applying this methodology in a Spartan-3 device, the tool error was 18% with respect to the measured value. Paper [10] presented several differences between measured and estimated power consumption, which varied from 15.52% to 208% for the Xilinx devices (Virtex II-Pro, and Spartan 3), and from 5.64% to 32.15% for the Altera device (Cyclone II), using security cores as benchmark circuits. Same authors in a more recent work [11] identified the effects of different synthesis settings on FPGA power consumption using security cores in a Virtex II-Pro. They stated that XPower Analyzer overestimates power consumption in a range from17.5% to more than 200%.

A different idea based on switched capacitor to get a cycle-by-cycle energy measurement in FPGAs was presented in [12]. Using this method it is possible to determine the static and dynamic energy per cycle. The authors reported that Xpower highly overestimates the predicted values when compared with the measured ones. The work [13] presented a dynamic power estimation methodology for the embedded multipliers in Xilinx Virtex-II PRO chips; and [14] proposed a procedure for power measurements in FPGA devices.

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On-board measurements of MicroBlaze power using ChipScope was performed in [15], and presented estimations with a 34% of error.

Finally, a more recent work [16] showed a new estimator with errors within 10% when compared with both on-board measurements and low-level XPower estimates for binary divider IP cores.

In this paper, we extended the measurements to a Xilinx Spartan-6 device using several circuits of different sizes, pipeline degree and with LUT and hardware embedded blocks implementations. The measured power values were compared with low-level estimations based on simulations.

III. EXPERIMENTAL WORK

The selected circuits used as benchmark were different types of multipliers, and a set of realistic circuits extracted from OpenCores. They were simulated to generate signal activity files, and this information was used to feed Xpower Analyzer.

The circuit shown in Fig. 1 was developed in order to make the experiments. Block 1 is the benchmark block or circuit under test (CUT), Block 2 includes an instance of Block 1 and an on-chip test vector generator, comprising a digital clock manager (DCM) and a linear feedback shift register (LFSR).

The LFSR output, a variable pseudo-random signal, was connected to the input of the CUT to generate all the possible input patterns. This experimental setup minimized the use of inputs and outputs and its influence on the design [16] [4].

The outer part of Block 2 (*i.e.* the LFSR, the DCM and the output parity generator), was common to all experiments while Block 1 was changed to include each different benchmark circuit.

The first series of experiments was done using a 32x32 unsigned integer multiplier as benchmark circuit. Different implementation alternatives were experimented for the multiplier:

- LUT pure combinatorial implementation.
- LUT implementation with different pipeline depths.
- Multiplier embedded block combinatorial implementation.
- Multiplier embedded block with different pipeline depths.

A second series of experiments was done using four different designs as benchmark circuits, obtained from the OpenCores site IP cores repository. The four cores employed as circuit under test were: "High throughput and low area AES core" [17], "Pipelined FFT/IFFT 256 points processor" [18], "IEEE 802.15.4 Core (physical layer)" [19][20] and "openMSP430" [21].

It is important to note that exactly the same configuration was used both for power estimation and measurement. They were performed on a testbench that instantiates the two blocks in Fig. 1, so that the only input that had to be generated was the external clock signal. The following sections provide a detailed description of the method.

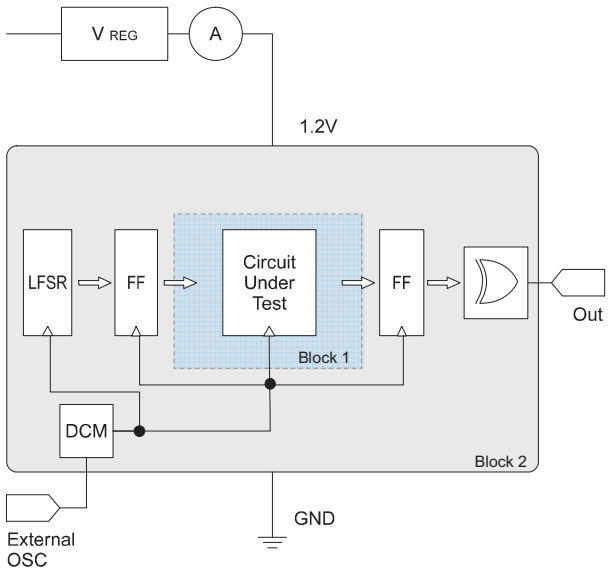

Fig. 1. Experimental setup

A. Estimation flow

The estimations were done as exactly as possible, using the XPower Analyzer tool. The node activity files were obtained from circuit simulations performed using the Isim simulator provided by the Xilinx ISE 13.1 tool.

Each simulation was run for a long interval in order to guarantee that the circuit reached a steady state from a power consumption point of view, obtaining as a result a SAIF format node activity file. These node activity files were provided as an input to the Xilinx XPower Analyzer tool to obtain the power consumption estimation. This tool gives a detailed power estimation report of the currents drained from the different power supplies.

B. Spartan-6 Measurement Setup

All the measurements were performed using an Avnet Xilinx Spartan 6 LX16 Evaluation Kit [22]. It includes some circuitry that simplifies the sensing of the input current. Each power supply circuit is equipped with a shunt, connected through a low pass filter to a differential input of a Cypress PSoC (CY8C38). Analog to digital conversion of the voltage on both terminals of each shunt was performed inside the PSoC, and the results were transmitted to a personal computer through a USB connection. Avnet provided a program (AvProg) to calculate mean values of the voltage and current of each of the power supplies of the board. The same program can be used to reconfigure the Spartan chip with a different design, downloading the bitstream.

The power consumption was determined by sensing the core power line voltage (1.2 V) and averaging 500 measurements for two identical boards. The system was

calibrated by connecting a Fluke 45 multimeter to the shunt terminals, that were accessible as test points.

A Matlab program was developed as a substitute of AvProg to automatize the measurement process of several different circuits. The program searches all the *.bit files inside a folder and, for each of them, it reconfigures the FPGA chip through the PsoC. After a delay to allow circuit stabilization, it measures the consumptions and stores them on disk. The communication protocol between the PSoC and the personal computer is proprietary from Avnet. To develop the Matlab implementation, the AvProg program and PSoC firmware source files were provided by Silica, an Avnet company.

IV. RESULTS

A. *Results for the 32x32 multipliers*

The results for different implementations of the 32x32 multiplier are listed in Table I. For each multiplier version, the measured current, the estimated current and the percentage error of the estimation with respect to its real measurement are shown.

The first remarkable observation is that the error introduced by the estimation tool is in some cases quite large, reaching a value of 149% in the worst case, which matches the results published in [10] and [11]. It can be observed that the worst cases are always for the combinatorial multiplier, followed by implementations with few pipeline stages. This suggests that the tool is overestimating the amount of glitches produced in a combinatorial circuit with long propagation paths. The Isim simulator does not allow for fine tuning when dealing with glitches. It only has an option *insert_pp_buffers* that avoids pulse swallowing during simulation, but it does not allow to control the width of the pulses to be filtered.

Different settings of Isim, simulation model and Xpower Analyzer configurations were experimented to minimize the error in power estimation. Among all the modifications tested, the best strategy was the modification of the "Simulation Model Target" variable. This variable specifies the HDL language used to represent the simulation model when performing the "Generate Post Place & Route Simulation Model" operation. The available options are: VHDL and Verilog. It was verified that when using Verilog instead of VHDL the estimation error was strongly reduced.

Table II lists the results for the different 32x32 multiplier alternatives. Fig. 2 and Fig. 3 show the same information graphically. As was explained above the use of Verilog greatly enhances the estimation, lowering the worst case error from 149% to 17%.

To obtain more insight, a simulation was run and the circuit output waveform was observed for both Verilog and VHDL netlists.

When comparing Fig. 4 with Fig. 5, it can be seen that in the simulated time interval the Verilog model filters out all the glitches. A zoom-in is shown in Fig. 6 and Fig. 7. In Fig. 6 glitches with different widths can be observed.

TABLE I. RESULTS FOR A SET OF 32X32 MULTIPLIERS

Type of circuit	Measured (mW)	Estimated (mW)	Error %
LUT	71.4	168.1	135
LUT 1 pipeline	71.3	173.2	143
LUT 2 pipeline	59.5	102.3	72
LUT 3 pipeline	47.0	66.2	41
LUT 4 pipeline	47.4	61.0	29
LUT 5 pipeline	46.1	58.8	28
LUT 6 pipeline	47.4	59.2	25
Embedded mult	22.0	54.8	149
Embedded mult 1 pipe	21.6	41.8	93
Embedded mult 2 pipe	18.5	25.5	38
Embedded mult 3 pipe	16.8	23.7	41
Embedded mult 4 pipe	16.2	22.6	40
Embedded mult 5 pipe	16.2	21.7	34
Embedded mult 6 pipe	17.1	23.3	36

TABLE II. RESULTS FOR A SET OF 32X32 MULTIPLIERS

Type of circuit	Measured (mA)	Estim. VHDL (mA)	Error VHDL %	Estim. Verilog (mA)	Error Verilog %
LUT	71.4	168.1	135	68.5	-4
LUT 1 pipeline	71.3	173.2	143	67.2	-6
LUT 2 pipeline	59.5	102.3	72	60.2	1
LUT 3 pipeline	47.0	66.2	41	54.9	17
LUT 4 pipeline	47.4	61.0	29	51.4	8
LUT 5 pipeline	46.1	58.8	28	50.9	10
LUT 6 pipeline	47.4	59.2	25	51.7	9
Embedded mult	22.0	54.8	149	20.2	-8
Embedded mult 1 pipe	21.6	41.8	93	20.1	-7
Embedded mult 2 pipe	18.5	25.5	38	19.2	4
Embedded mult 3 pipe	16.8	23.7	41	18.4	10
Embedded mult 4 pipe	16.2	22.6	40	18.9	17
Embedded mult 5 pipe	16.2	21.7	34	18.8	16
Embedded mult 6 pipe	17.1	23.3	36	19.1	12

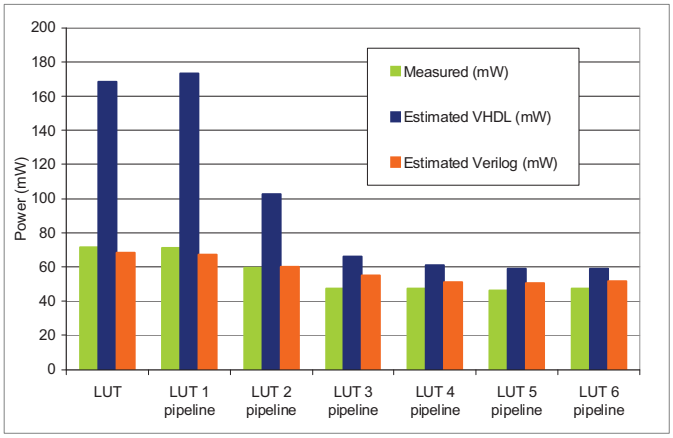

Fig. 2. Mult 32x32 LUT power consumption estimated and measured

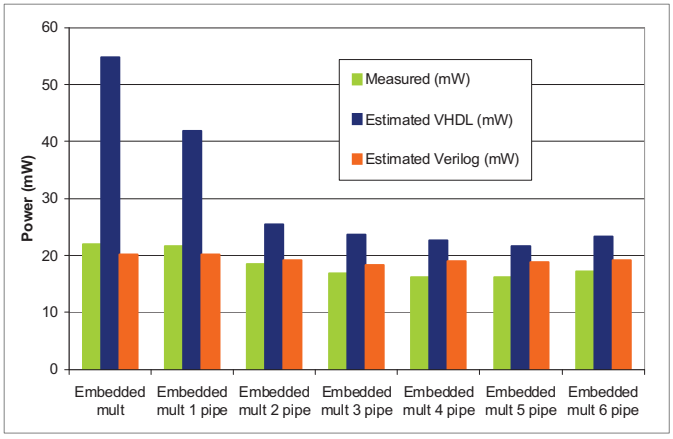

Fig. 3. Mult 32x32 DSP power consumption estimated and measured

B. Results for the OpenCore circuits

In order to analyze if the previous results are consistent throughout a wide type of circuits, the power consumption of several blocks obtained from the OpenCores IP core repository was simulated and measured. The power estimations and measurements were obtained using the same methodology explained above for the set of 32x32 multipliers.

The cores employed as benchmark circuits include an AES coder, an FFT calculator, an implementation of the physical layer of IEEE 802.15.4 and a 16 bit microcontroller openMSP430. In the last case the microcontroller is running an endless loop program previously loaded in memory performing a matrix multiplication. Note that in this case clock and reset are the only inputs to the CUT.

Table III shows a summary of the main block characteristics and the measured and estimated power consumption results are listed on Table IV. Very large estimation errors, as high as 377% in the worst case, are obtained when using VHDL. On the other hand, when Verilog is utilized, the estimations are consistently much closer to the measured values. The estimations are very good for the first two circuits, but the size of the estimation errors is still too high for the OpenMSP430 and the IEEE 802.15.4. blocks.

TABLE III. OPENCORE CIRCUITS CHARACTERISTICS

	LUT	FF	Embedded Mult	RAM Blocks	Clock Blocks	MHz
AES	2343	1419	0	0	1	66
FFT	5314	4278	4	3	1	100
IEEE802154	2048	440	0	0	1	16/2
openMSP430	1847	1006	1	4	2	20

TABLE IV. POWER CONSUMPTION OF OPENCORE CIRCUITS

Type of circuit	Measured (mW)	Estim. VHDL (mW)	Estim. Verilog (mW)	Error Estim. VHDL %	Error Estim. Verilog %
AES	90.7	206.4	86.1	128%	-5%
FFT	218.2	277.3	235.4	27%	8%
IEEE802.15.4	14.3	68.0	23.2	377%	63%
OpenMSP430	21.9	29.5	26.7	35%	22%

V. CONCLUSION

High differences were found between measured and estimated power for most of the circuits under study. When different implementations of the same function were experimented, the errors were consistently higher in the circuits with longer combinatorial paths. Even when special care was taken to provide a realistic estimation of node activity for all the circuit nodes, the resulting estimation was not good for several of the circuits under analysis.

The divergence between estimation and measurements can be attributed to the simulator tool rather than to the power consumption estimation one. To obtain a good estimation it is required that the simulation matches the real circuit behavior in the presence of glitches.

An important conclusion is that, at least with the versions of the tools employed in the present work, it is not possible to know *a priori* if the glitches are being correctly simulated, and consequently if the power estimation is close to reality. Therefore some measurements must be done, at least to calibrate the results provided by the tools.

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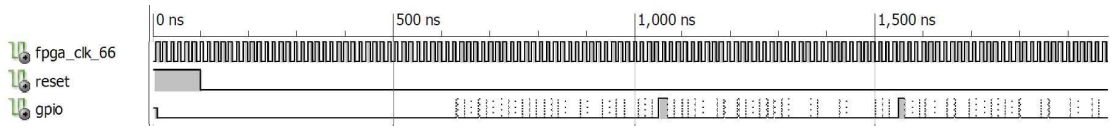

Fig. 4. Simulation with VHDL netlist

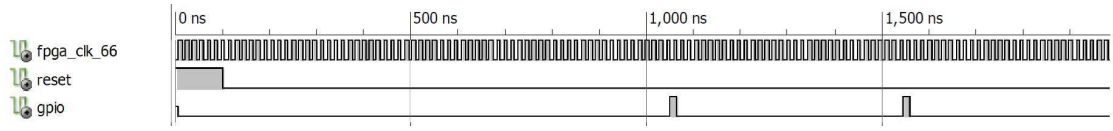

Fig. 5. Simulation with Verilog netlist

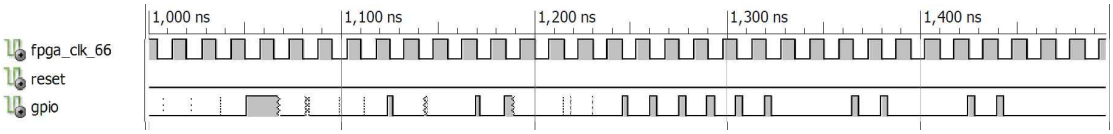

Fig. 6 Zoom of VHDL netlist simulation

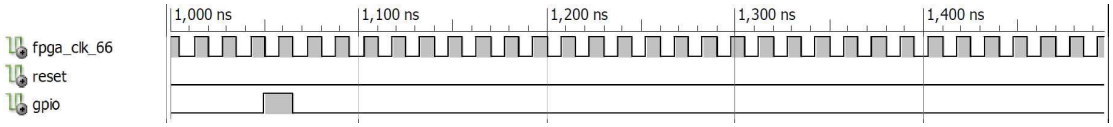

Fig. 7. Zoom of Verilog netlist simulation

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