Analysis and Implementation of Low-cost FPGA-Based Digital Pulse-width Modulators

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***Abstract*—This paper describes the architecture and operating principles of two digital pulse-width modulator (DPWM) implementations for low-cost field-programmable gate arrays (FPGAs). Both architectures are based on a counter-comparator block to process the most significant bits (MSB) portion of the reference input, enriched with additional elements to enhance duty-cycle resolution according to the less significant bits (LSB). The first architecture described has already been reported, it uses the on-chip PLL blocks to generate fixed delays and a selector to choose the one corresponding with the desired duty-cycle. Post-fitting adjustment of PLL delays are required to compensate delay differences between the diverse signal paths across the selector. In the second architecture described, a serializer-deserializer (SERDES) module is used to serialize a thermometer-coded representation of the LSB portion of the input. This serialization technique is commonly used for data transmission on high-speed serial I/O data transmission standards like LVDS and is extensively supported by FPGA providers. Experimental results are presented for both architectures synthesized on standard low-cost FPGA chips, showing very good linearity and resolutions up to 1ns. The first architecture provides a moderately better resolution. The second architecture, on the other hand, is a much more robust solution as it requires no post-fitting delay adjustments.**

Keywords—DPWM; FPGA; serdes; LVDS

I. INTRODUCTION

The trend toward digital control in high-frequency dc-dc converters has created a need for a new class of modulator: the digital pulse-width modulator (DPWM). This basic building block receives as an input a digital word and outputs a square wave of fixed period with the a duty-cycle proportional to the input value. It can therefore be used as a modulator for controlling the switches in dc-dc converter applications, substituting traditional analog implementations.

Many DPWM designs have been proposed in the literature, mostly consisting of custom ASIC implementations. These are suited for high-volume products but may not be practical for research, prototype design or low-volume products because of the high costs involved in ASIC design and fabrication. Therefore, there exists a need for low-cost FPGA-based DPWM blocks that can be incorporated early in a digital control loop design process.

Some FPGA-based DPWM implementations were reported in [1]-[5]. The implementations presented in [1],[2] use delay lines in combination with a counter-comparator architecture, emulating in some sense many of the ASIC implementations found in the literature. These implementations obtain excellent resolution results, but they require manual routing or post fitting adjustments, and they lack of flexibility as the obtained resolution must be a multiple of technology dependent delays. A recent work [7] uses Altera's synthesis tool features to avoid the need for manual routing but still suffer from the second drawback.

In [3]-[6] specific resources encountered in modern FPGAs are used, namely phase-locked loops (PLL), also complemented by a counter-comparator architecture. One aproach [3],[5] uses on-chip PLL blocks to generate fixed delays and a selector to choose the appropriate delay. Manual routing or post-fitting delay adjustments are needed to compensate delay differences between the different propagation paths. Other works [4], [6] use the fine phase shifting of the clock available in the on-chip PLL of most FPGA families obtaining resolution values similar to the delay lines solutions. However, the procedures to modify the phase on PLL outputs is usually slow, and this is undesirable when a fast response is needed.

This paper describes two DPWM architectures with emphasis on low-cost FPGA implementation. One implementation, presented in section II., is based in the architectures presented in [3], [5] and, as expected, post-fitting adjustment to PLL delays was needed to obtain a linear response. The second implementation is introduced in section III. and, as far as the authors know, is a novel one. It is based on a serializer block driving an LVDS high-speed serial I/O available in most of modern FPGA families and does not need manual routing nor post-fitting calibration. The device used for these designs belongs to the Cyclone II family by Altera. The target specification is a PWM period of 1us with a duty-cycle resolution of 1ns.

II. PLL-BASED DPWM

The system's main components are shown in Fig. 1. and described next. The key in this DPWM is the flexibility in the

management of clock signals provided by the PLLs. With these blocks it is possible to change the phase of clock signals, as well as to multiply and divide its frequency in a controlled manner. The PLL multiplies the system's clock frequency from 25MHz to 250MHz. Besides the main output P0, three additional outputs P90, P180 and P270 are generated with phase shifts of 90º, 180º, and 270º respectively. The use of these signals allow for an effective increase in the resolution of the DPWM, adding two more input bits providing a fine adjustment of the duty-cycle reaching 1ns resolution.

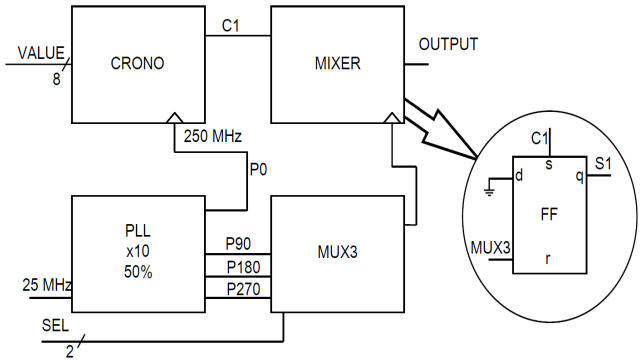

Fig. 1. Simplified diagram of the PLL-based DPWM architecture.

Delay differences due to different paths inside the multiplexor lead to non-monotonic and non-linear behavior. These undesired effects are eliminated by a calibrating procedure: a post-fitting simulation is run to estimate the delay differences and the phase shifts at the PLL outputs are adjusted accordingly. Special care must be taken to lock on-chip placement of the DPWM module resources after this calibration is completed. Otherwise the insertion of additional circuit elements (as the JTAG interface module used during the experiments to provide module inputs) can completely modify the placement of the circuit inside the chip and therefore also the timing and delays, leaving the previous calibration useless.

III. SERDES-BASED DPWM

The second implementation is based on the use of a serializer-deserializer (SERDES) module and the low voltage differential signal (LVDS) I/O standard. This serialization technique is commonly used for data transmission over high speed serial I/O lines and is extensively supported by FPGA providers. It can also be applied to enhance DPWM resolution as explained next.

The architecture is shown in Fig. 2. The SERIAL block receives a 4-bit parallel vector at the edges of the system's clock (200 MHz) serializing these bits at the output beginning with the most significant bit. In our case the output rate is 800 Mbps, which will have a resolution of 1,25 ns. During the relevant clock period at the end of the pulse on the counter-comparator output, a thermometer encoding of SEL is presented to the serializer module input, thus providing the fine adjustment resolution control.

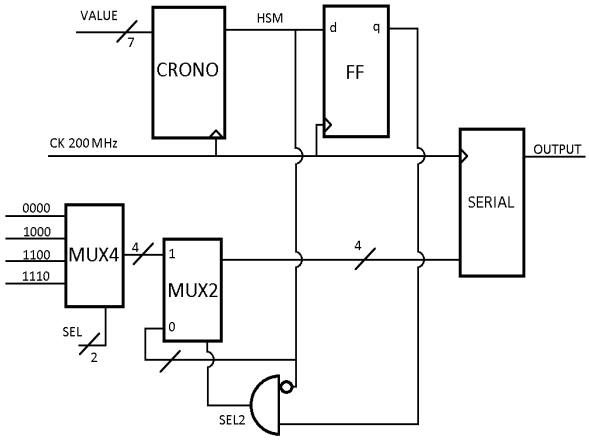

Fig. 2. Simplified diagram of SERDES-based DPWM.

The limitation to the resolution is imposed by the maximum data rate tolerated by the FPGA's high speed LVDS output pins. It was 805MHz on the Cyclone II chip used during measurements [8]. This limit has been increased up to 1080MHz on newer low-cost chips [9].

IV. RESULTS

Both implemented systems were experimentally evaluated on the IIE-Cylcone board, a general-purpose FPGA board developed by our group that is equipped with a IIE-Cyclone II FPGA.

Coarse adjustment is obtained in both architectures by the use of a counter-comparator module, providing a good behavior in terms of large-signal linearity and proportionality between the digital input and the duty cycle output. In this paper we focus on small-signal properties like monotonicity and accuracy of the increments in pulse duration with unity increments in the digital input word.

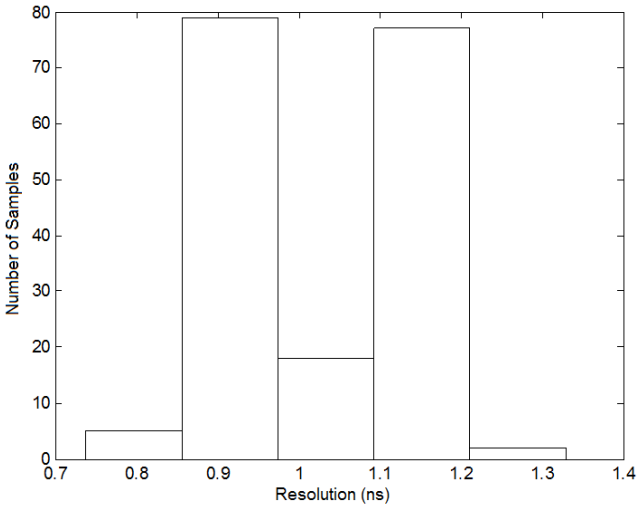

Fig. 3. PLL-based method histogram.

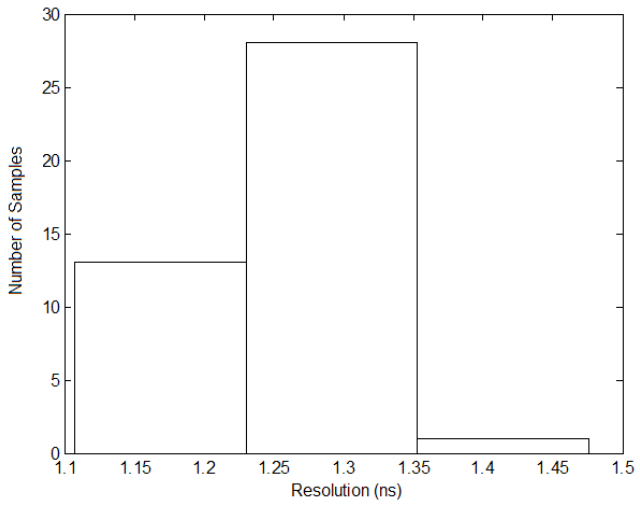

Fig. 4. SERDES-based method histogram.

Measurements of the output were taken for several intervals covering the whole duty cycle range. On each interval the duty cycle was measured for every input value and the step increment was evaluated. Histograms of the step values are presented in Fig. 3. and Fig. 4., and TABLE I. shows step average values and maximum error for both architectures.

TABLE I. SUMMARY OF STEP MEASUREMENTS

	PLL-based	**SERDES-based**
Step average (ns)	1,0226	1,2564
Maximum relative error (%)	30,5	18,1

V. CONCLUSIONS

Two possible solutions to build a digital pulse-width modulator (DPWM) were presented: the PLL-based method (already reported in the literature) and the SERDES-based method (a novel contribution of this paper). Both modulators are composed of two main blocks: a counter and comparator block for coarse resolution and a fine-tuning block comprising either a PLL or a serializer. The two solutions can be implemented in low-cost FPGAs.

The PLL-based method achieves a resolution of 1ns while the SERDES-based method achieves a resolution of 1.25ns in the low-cost EP2C20 Cyclone II FPGA. The measured average resolution in both cases is within 2% of the nominal value and the maximum error, relative to the nominal value, is within 30%. It is concluded that both solutions have good linearity and monotonicity properties.

While the PLL-based method achieves a finer resolution, it also requires a calibration procedure dependent on the final placing and routing in order to compensate for different path delays in the PLL signals. Once the calibration is made the system must remain unaltered to preserve linearity and monotonicity, which implies that a change in the circuit design may require a new calibration.

On the other hand, the SERDES-based solution design process is simple and straightforward, the resulting circuit is robust with respect to modifications in place and route and the response to a change in the required duty cycle is fast. The above characteristics make the proposed solution, based on a serializer attached to a standard high speed I/O pin, a very attractive alternative for the DPWM controller in a growing range of resolutions.

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