

Design Method for an Ultra Low Power, Low Offset, Symmetric OTA

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Abstract—A design method for ultra low power, low offset, symmetric OTAs is presented. The method is based on the g_m/I_D methodology and uses a model of MOS transistor valid in all the regions of operation which assures that the optimal operating point is chosen. The method was used to design a $2.5 \frac{\mu A}{V}$ cascoded OTA with minimum offset and current consumption in a $0.5 \mu m$ CMOS technology. Post layout Montecarlo simulations were performed to obtain an estimated offset of the circuit. The standard deviation obtained from the Montecarlo simulation was $3.94 mV$ while that expected from the design method was $3.86 mV$. The total current consumption of the OTA is only $400 nA$. Simulation results confirm the reliability of the presented design method.

I. INTRODUCTION

Analytical methods for the synthesis of analog circuits provide the designer with a fast insight to the trade-offs among specifications. Using a design method based on a model of the MOS transistor valid in all regions of operation [1], leads to an optimal design of the circuit. This method is based on the g_m/I_D methodology [2], [3] which allows the designer to choose the best operating point for each transistor and provides a tool for computing their dimensions.

Additionally, the growing demand for battery-powered devices has increased the efforts to optimize their consumption and thus increase battery life. It is well known that in CMOS analog circuits the minimum power consumption is achieved when MOS transistors operate in the weak inversion region [4] while the maximum speed is achieved in strong inversion. Because of this trade-off between speed and consumption, the best compromise is often achieved in moderate inversion. The g_m/I_D methodology considers all the operating regions of the MOS transistor allowing the designer to evaluate this trade-off.

Offset is an important issue regarding analog circuit design, specially in amplifiers and comparators. Variations in the parameters of two identical devices due to randomness in the fabrication process lead to offset voltages that reduce the performance of the circuit.

Offset is usually modelled [5] through the following equations

$$\sigma(\Delta V_T) = \frac{A_{VT}}{\sqrt{W \cdot L}}, \sigma\left(\frac{\Delta \beta}{\beta}\right) = \frac{A_\beta}{\sqrt{W \cdot L}}, \quad (1)$$

where A_T and A_β are technology-dependent constants.

The inaccuracy caused by offset can be reduced in two ways: improving matching of devices by increasing their

sizes and introducing offset compensation techniques such as autozeroing, correlated double sampling, chopper stabilization [6] and dynamic element matching [7], [8].

While the latter techniques are very effective, they usually increase circuit complexity and consumption. This work deals with the raw offset of a circuit. In turn, it can be further reduced by using the aforementioned techniques.

On the contrary to the simple differential OTA, a symmetric cascode OTA (Fig. 1) displays high output impedance, G_m multiplier capability and the output voltage swing does not depend on the input common mode voltage [9]. Thus, this architecture is used in a very wide range of applications.

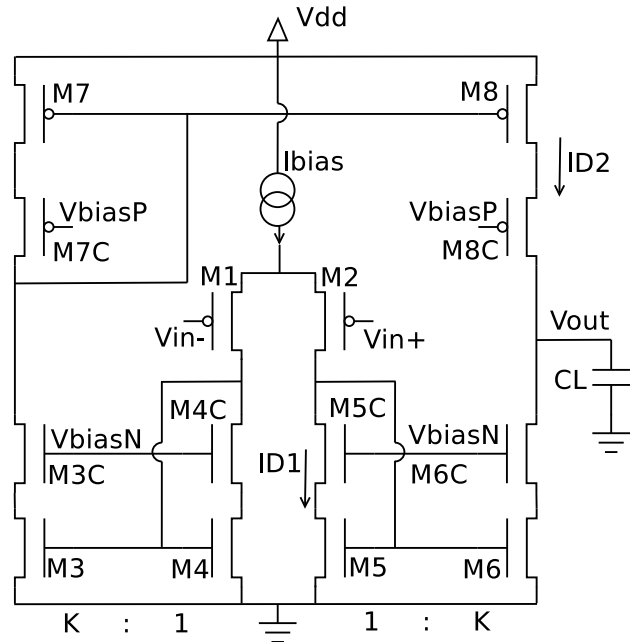


Fig. 1. Architecture of a Symmetric Cascode OTA

This paper is organized as follows. Section II presents the design method while Section III shows an application example. Simulation results can be found in Section IV. Finally, conclusions are drawn in Section V.

II. DESIGN METHOD

The design method proposed in this work takes into consideration the trade-offs among power consumption, offset and bandwidth of the circuit allowing the designer to obtain the optimal operating point for a given total transconductance.

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Figure 2 shows a flow chart of the proposed method. The following paragraphs describe each step of the method in detail.

Notation

- G_m : Total transconductance of the OTA
- K : copy ratio of the NMOS current mirror
- f_T : unit gain frequency
- PM : phase margin
- $f_{p_{MN(P)}}$: frequency of the parasitic pole introduced by the NMOS (PMOS) mirror
- $\alpha_{MN(P)} = f_{p_{MN(P)}}/f_T$
- $V_{off_{MN(P)}}$: offset voltage introduced by the NMOS (PMOS) current mirror
- $V_{off_{DP}}$: offset voltage introduced by the differential pair
- $V_{off_{TOT}}$: total offset voltage (quadratic sum of $V_{off_{MN}}$, $V_{off_{MP}}$ and $V_{off_{DP}}$)
- I_{D_1} and I_{D_2} : branch currents as shown in Fig. 1

All the offset voltages are expressed as one standard deviation (1σ). Cascode transistors $M_{3C,4C,5C,6C,7C,8C}$ shown in Fig. 1 are the same size as transistors $M_{3,4,5,6,7,8}$ respectively. This simplifies the implementation of good layout matching techniques essential to minimize the parameter variations due to the fabrication process. Additionally, the method that will be presented can be used whether the OTA is cascoded or not. For this very same reason, equal lengths were selected for transistors M_3 to M_6 and also for M_7 and M_8 .

In order to ensure that the bandwidth is not affected by the parasitic poles introduced by the circuit, the frequency of each of them will be kept α times over the f_T ($\alpha_{MN}, \alpha_{MP} > \alpha$).

Step 1: Select g_m/I_D of transistors M_1 and M_2

In order to select them, the influence of this parameter over power consumption and offset will be analyzed. The dependence on $(g_m/I_D)_{1,2}$ of the transconductance and offset voltage introduced by the differential pair are shown in

$$G_m = K \cdot \left(\frac{g_m}{I_D}\right)_{1,2} \times I_{D_1} \quad (2)$$

and

$$V_{off_{DP}} = \sqrt{\frac{2}{(WL)_{1,2}}} \sqrt{A_T^2 + \left(\frac{A_\beta}{(g_m/I_D)_{1,2}}\right)^2}, \quad (3)$$

respectively [10]. W and L are the width and length of transistors M_1 and M_2 while A_β and A_T are the technology-dependent constants used to model the random variation of the difference in threshold voltage V_T and current factor β .

Equation (2) shows that for a given G_m , if $(g_m/I_D)_{1,2} \uparrow$ then $I_D \downarrow$ and consequently power consumption decreases. Regarding offset, (3) shows that if $(g_m/I_D)_{1,2} \uparrow$ then offset will decrease. Additionally, transistors in weak inversion have a higher aspect ratio (W/L) which leads to bigger transistors decreasing even more $V_{off_{DP}}$. Because of these, the highest g_m/I_D allowed by the technology must be selected for transistor M_1 and M_2 .

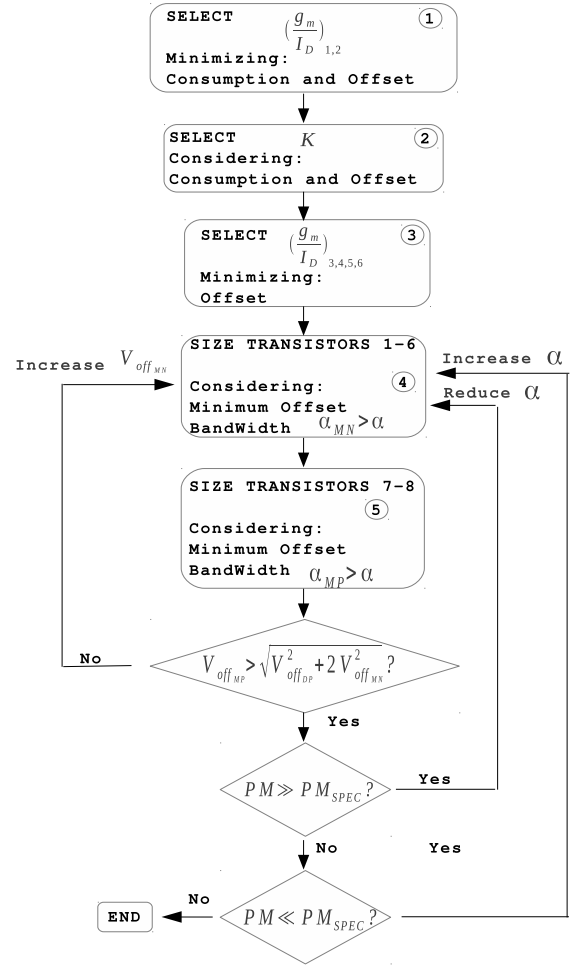


Fig. 2. Proposed design method

Step 2: Select the NMOS current mirror ratio (K)

Having selected $(g_m/I_D)_{1,2}$ (Step 1) and using the specified G_m , branch current I_{D_2} is defined by

$$\left. \begin{aligned} (g_m/I_D)_1 \\ G_m = K g_{m_1} \end{aligned} \right\} \Rightarrow I_{D_1} = \frac{G_m}{K \cdot (g_m/I_D)_1} \quad (4)$$

$$\Rightarrow I_{D_2} = K I_{D_1} = \frac{G_m}{(g_m/I_D)_1}$$

Thus, the total current of the circuit is determined by the NMOS current mirror ratio (K) as

$$I_{TOT} = 2I_{D_2} \left(1 + \frac{1}{K}\right). \quad (5)$$

Equation (5) shows that the total consumption decreases with K .

On the other hand, a larger value of K increases the gate capacitance of M_6 leading to a smaller α_{MN} . In order to keep $\alpha_{MN} > \alpha$, the area of both M_5 and M_6 would need to be decreased which in turn increases $V_{off_{MN}}$. Thus, there is a trade-off between power consumption and offset entailed by the choice of K . If $K \uparrow$ then $V_{off_{TOT}} \uparrow$ and Power \downarrow . Moreover, the dependence between consumption and K (5) shows that the power reduction decreases as a larger K is selected.

The selected K must be the minimum that assures the restriction of power consumption is guaranteed. A larger value of K would reduce the power consumption at the expense of a larger offset.

As $(g_m/I_D)_{1,2}$ and I_{D1} are now known, the aspect ratio $M_{1,2}$ is determined by the (g_m/I_D) characteristic curve for the technology [2], [3]. After choosing a value for $L_{1,2}$ $M_{1,2}$ are completely determined and V_{offDP} can be computed from (3).

However, in this method V_{offDP} will be considered as the design variable in place of $L_{1,2}$. Thus for a given V_{offDP} , (3) and $(W/L)_{1,2}$ determine $W_{1,2}$ and $L_{1,2}$.

Step 3: Select g_m/I_D of transistors $M_{3,4,5,6}$

The offset voltage contributed by the NMOS mirror is [10]

$$V_{offMN} = \frac{1}{K(g_m/I_D)_1} \sqrt{\frac{2}{W_3 L_3}} \sqrt{A_\beta^2 + \left[\left(\frac{g_m}{I_D} \right)_3 A_T \right]^2} \quad (6)$$

For a given $(g_m/I_D)_{3,4,5,6}$ a similar discussion can be made for $M_{3,4,5,6}$ as for $M_{1,2}$. Hence, the design variable will be V_{offMN} which determines $W_{3,4,5,6}$ and $L_{3,4,5,6}$.

Now, we have a design space defined by V_{offDP} and V_{offMN} where the dimensions of the transistors $M_{1,2,3,4,5,6}$ are determined. Therefore, the parasitic capacitance in the gates of $M_{3,4}$ and $M_{4,5}$ and in the drains of $M_{1,2}$ can be estimated and thus the parasitic pole f_{pMN} can be computed in each point of the design space for each value of $(g_m/I_D)_{3,4,5,6}$.

Design condition $\alpha_{MN} > \alpha$ must be imposed. Fig. 3 shows curves with constant $\alpha_{MN} = \alpha$, and $(g_m/I_D)_{3,4,5,6}$ as a parameter, as a function of design variables V_{offMN} and V_{offDP} . The thin elliptical curves represent constant total offset voltages considering the contribution of the differential pair and the NMOS mirror.

The figure is based on data from the example in section III. It provides the designer with a graphical tool to choose a constant $(g_m/I_D)_{3,4,5,6}$ curve which allows to achieve the minimum offset.

Step 4: Size transistors $M_{1,2,3,4,5,6}$

Figure 4 depicts the same diagram as Fig. 3, showing only the curve for the chosen $(g_m/I_D)_{3,4,5,6}$. The curve is a boundary between a forbidden (gray) area and the region where $\alpha_{MN} > \alpha$ as desired, so that the parasitics associated with the NMOS mirror do not significantly affect f_T .

In the first iteration at this step, the selected design point should be the one which minimizes the total offset introduced by both NMOS current mirrors and the differential pair (black circle in Fig. 4). As already shown, once V_{offDP} and V_{offMN} are chosen, the dimensions of $M_{1,2,3,4,5,6}$ are determined.

W_{3C} (in our case equal to W_3) might adversely affect the parasitic pole associated with the PMOS mirror (f_{pMP}). If that is the case (M_3 too wide), step 5 will result in relatively small $M_{7,8}$ transistors in order to keep $\alpha_{MP} > \alpha$ and V_{offMP} might dominate the total offset.

In that case, the designer must come back to this step and choose another design point with a larger V_{offMN} (for example the square one shown in Fig. 4). Increasing V_{offMN} decreases W_3 , allowing the designer to enlarge transistors $M_{7,8}$. Thus, V_{offMP} decreases at the expense of a larger V_{offMN} , while V_{offTOT} decreases.

Step 5: Size transistors $M_{7,8}$

Since the current of these transistors is defined, its size will be determined by $(g_m/I_D)_{7,8}$ and $L_{7,8}$ [2], [3]. A numerical analysis must be performed in order to evaluate the trade-off between bandwidth and V_{offMP} . An example of this analysis is shown in Fig. 5. It shows V_{offMP} and the bandwidth related boundary $\alpha_{MP} = \alpha$ as a function of $(g_m/I_D)_{7,8}$ and $L_{7,8}$.

The gray filled zone over the continuous black line does not fulfil the condition $\alpha_{MP} > \alpha$. The minimum transistor width allowed by the technology is represented by the continuous gray line and defines another forbidden region. Finally, the loci of constant V_{offMP} are depicted as thin black lines. This analysis allows the designer to choose the design point which adds the minimum offset to the circuit, thus defining $W_{7,8}$ and $L_{7,8}$.

As it was explained in step 4, in order to obtain minimum V_{offTOT} , V_{offMP} must not dominate over V_{offMN} . If these offset voltages are approximately the same, the designer must proceed to the next step. Otherwise, it is necessary to return to step 4 in order to increase V_{offMN} , which will result in a smaller V_{offMP} .

Step 6: Verify specifications

At this point the size of every transistor has been determined. Now, all the parameters of the circuit must be calculated to confirm that the specifications are fulfilled.

In particular, the DC gain is

$$A_0 = G_m R_o, \quad (7)$$

where

$$R_o = \frac{g_m s_{8c}}{g_{d8} g_{d8c}} // \frac{g_m s_{6c}}{g_{d6} g_{d6c}} \quad (8)$$

and

$$g_d \approx \frac{I_D}{V_A L} \quad (9)$$

where V_A is the normalized ‘‘Early voltage’’ of the transistor.

If the DC gain of the circuit, computed through (7), (8) and (9), is not large enough to satisfy the specifications, the design must be repeated, this time lifting the restriction $M_{iC} = M_i$ on the cascodes. After calculating f_T and the phase margin (PM), if they comply with the specifications, the design is finished. Otherwise, if the phase margin is too high and f_T is satisfied, the designer must reduce α and go back to step 4 which in consequence reduces the total offset at the expense of a lower phase margin. On the contrary, if either the phase margin is too low or the f_T requirement is not fulfilled, α should be increased before returning to step 4.

III. APPLICATION OF THE DESIGN METHOD

The design method described in section II will be used to design a low power, low offset, OTA as specified in Table I.

In this case, α is initially chosen as 5, but as explained in section II this might change during the design process.

In order to obtain the large gain required by the specifications, cascode transistors are needed. From specifications the output resistance can be calculated as

$$R_{out} = \frac{A_0}{G_m} = 4 \text{ G}\Omega \quad (10)$$

If we were achieve this output resistance without cascodes, the length of transistors $M_{6,8}$ would have been

$$L_{6,8} = \frac{R_{06,8} \cdot I_{D2}}{V_A} > 188 \mu\text{m} . \quad (11)$$

where V_A is the normalized ‘‘Early voltage’’ of the transistor and I_{D2} was chosen as the minimum current that fulfils the restriction imposed by (4).

Step 1: Select g_m/I_D of transistors M_1 and M_2

In order to obtain the minimum offset and power consumption, the maximum $(g_m/I_D) = 25 \text{ V}^{-1}$ allowed by the technology was chosen.

TABLE I
SPECIFICATIONS FOR THE EXAMPLE IN SECTION III

$V_{DD}(V)$	3.3
$A_0(dB)$	> 80
$G_m(\mu S)$	2.5
Offset	Minimum
Consumption	Minimum
$f_T(kHz)$	200
$C_L(pF)$	2

Step 2: Select the NMOS current mirror ratio (K)

Having selected $(g_m/I_D)_{1,2} = 25 \text{ V}^{-1}$ (Step 1) and $G_m = 2.5 \mu S$ (from specs), (4) defines $I_{D2} = 100 \text{ nA}$. By choosing K , the power consumption of the circuit is defined. In this application we prioritize offset over power consumption, thus $K = 1$ was selected obtaining a total consumption of 400 nA .

Step 3: Select g_m/I_D of transistors $M_{3,4,5,6}$

The numerical analysis explained in section II is shown in Fig. 3. It can be concluded that for this application the maximum $(g_m/I_D)_{3,4,5,6}$ allowed by the technology must be selected. Table II shows this choice.

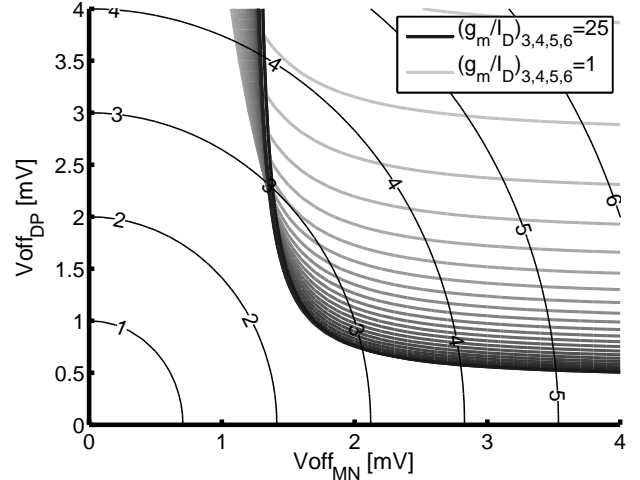


Fig. 3. Selecting $(g_m/I_D)_{3,4,5,6}$

Step 4: Size transistors $M_{1,2,3,4,5,6}$

The result of the numerical analysis presented in section II is shown in Fig. 4. The forbidden region (filled gray) does not fulfil the restriction $\alpha_{MN} > 5$ on the parasitic pole. Additionally, it shows that this restriction is enough to guarantee that the frequency of the parasitic pole introduced by the cascode is at least fifteen times f_T (vertical dashed line inside gray area). It also shows the total voltage offset introduced by the differential pair and NMOS current mirrors.

The selected design point is the black circle, obtaining the minimum total voltage offset introduced by both NMOS current mirrors and the differential pair. From $V_{off_{MN}}$, $V_{off_{DP}}$ and $(g_m/I_D)_{3,4,5,6}$, the sizes of transistors $M_{1,2,3,4,5,6}$ are obtained. This result is presented in table II.

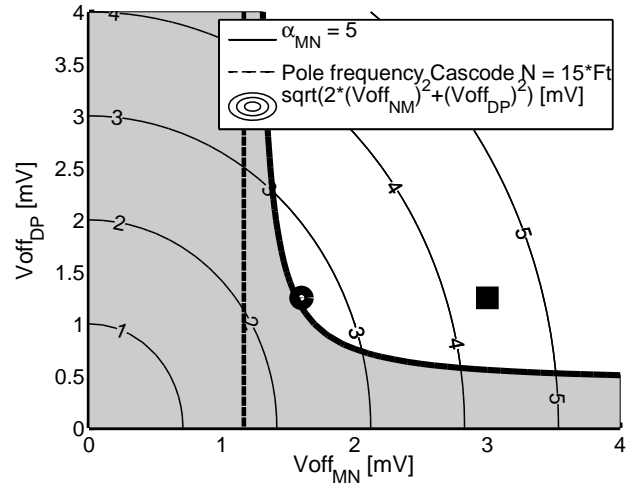


Fig. 4. Sizing of transistors $M_{1,2,3,4,5,6}$

Step 5: Size transistors $M_{7,8}$

The performed numerical analysis is shown in Fig. 5. The minimum achievable offset is obtained by choosing the point

marked as a square in this figure. However, by selecting the one marked as a circle, V_{offMP} is not significantly increased while the output voltage swing has a considerable improvement due to the decrease of V_{DSSat} of $M_{7,8}$, now in moderate inversion. An even larger value of $(g_m/I_D)_{7,8}$ worsens the offset voltage but does not considerably decrease V_{DSSat} .

From $(g_m/I_D)_{7,8}$ and $L_{7,8}$ the sizes of $M_{7,8}$ are determined as shown in Table II.

As V_{offMN} , V_{offDP} and V_{offMP} all have a similar value, it is not necessary to iterate back to step 4.

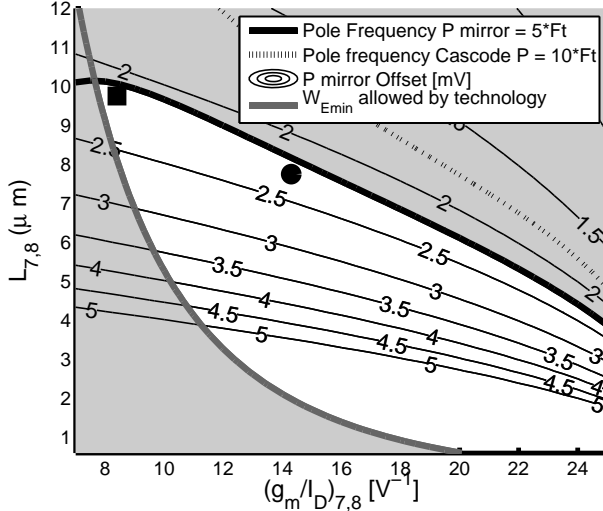


Fig. 5. Sizing of transistors $M_{7,8}$

Step 6: Verify specifications

Transistors sizes determined in steps 1 to 5 are shown in Table II which also presents the offset voltages introduced by each block. From these values, all the circuit parameters are computed and reported in Table III. No further iterations were needed.

TABLE II
TRANSISTOR SIZES, g_m/I_D AND PARTIAL OFFSET VOLTAGES.

	Sizes [μm]	g_m/I_D [V^{-1}]	V_{off} [mV]
$M_{1,2}$	$W = 79.8; L = 1.95$	25	1.29
$M_{3,4,5,6}$	$W = 34.5; L = 5.4$	25	2.39
$M_{7,8}$	$W = 6; L = 7.8$	14.3	2.24

IV. LAYOUT AND SIMULATIONS

The layout of the designed circuit was performed on a $0.5 \mu\text{m}$ CMOS technology while observing proper layout practices for minimum mismatch [11]. These are required for the A_T and A_β parameters in (3) and (6) to be valid. Fig. 6 shows the layout of the complete circuit. The total die area is $20.000 (\mu\text{m})^2$ while the gate to total area ratio of the circuit is 0.1.

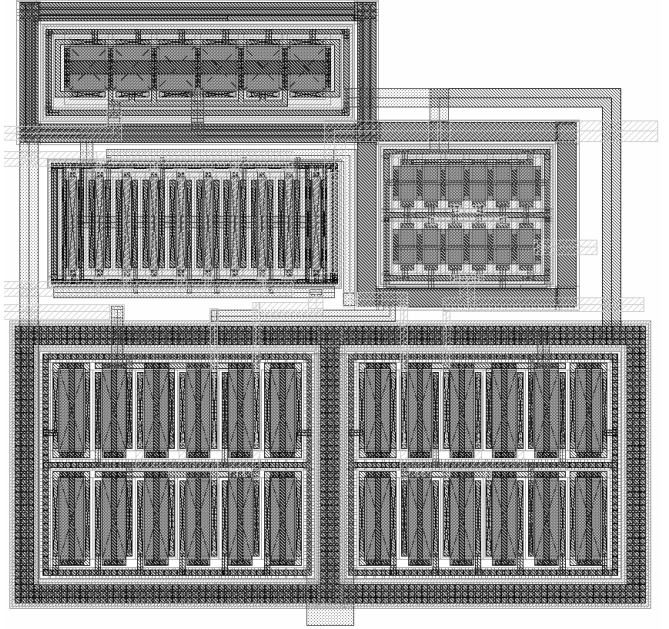


Fig. 6. Layout of the symmetric OTA

TABLE III
COMPARISON OF SPECS, DESIGN AND SIMULATIONS

	Specifications	Design	Simulation
G_m ($\frac{\mu\text{A}}{\text{V}}$)	2.5	2.5	2.5
f_T (kHz)	200	195.5	187.3
PM (Deg)	>60	68.1	64.4
A_0 (dB)	>80	105.7	112.0
Offset (mV) (1σ)	Min	3.86	3.94
Consumption (nA)	Min	400	400
OVSF (V)	-	[0.32, 2.92]	[0.27, 3.04]
ICMR (V)	-	[-0.88, 2.27]	[-0.85, 2.38]

Post-layout simulations were performed taking into account all parasitic capacitances, including those due to wiring. The result from these simulations are shown in Table III together with specified values and those computed by the design method. As expected, f_T and PM are somewhat degraded in post layout simulations. However, these difference are not significant. During the design a slightly larger PM than specified was used in order to compensate for the lower parasitic capacitance. V_{biasN} and V_{biasP} were computed to obtain the maximum output voltage swing.

The simulated circuit had a higher DC gain (A_0) than that estimated during the design. The latter one was calculated using (7), (8) and (9). As (9) is a first approximation of g_d it leads to a slight difference between computed and simulated DC gain.

Total offset voltage (V_{offTOT}) was simulated by 2000 MonteCarlo runs, as presented in Fig. 7. Table III shows the offset voltage (1σ) estimated during the design stage using (3) and (6), and that obtained from simulation. The analytical result is an excellent estimation of the simulated parameter.

V. CONCLUSION

A design method for ultra low power, low offset, symmetric operational transconductance amplifiers was introduced. The method was applied to an example implementing a specific OTA, comparing the post layout simulation results with parameters expected from design, proving the accuracy of the method. The estimated offset voltage (1σ) was $3.86mV$ while that simulated through 2000 Montecarlo runs was $3.94mV$.

The layout of the circuit was implemented on a $0.5\ \mu m$ CMOS process and is being fabricated.

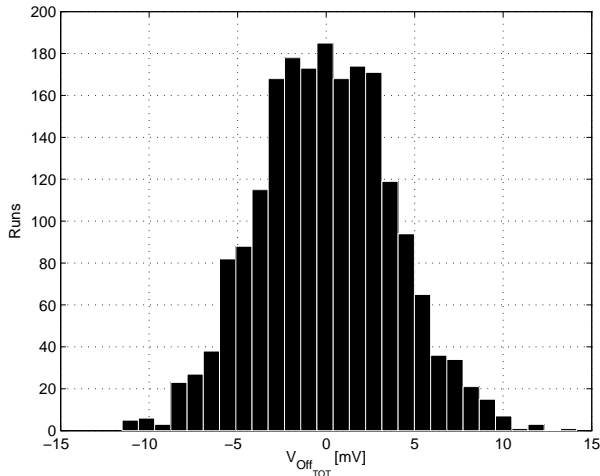


Fig. 7. Offset voltage distribution obtained for a 2000-run Montecarlo simulation

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