Modular Architecture For Ultra Low Power Switched-Capacitor DC-DC Converters

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***Abstract*— This work presents a novel modular architecture for a step-down Switched-Capacitor Converter for Ultra Low Power applications. The modularity of the architecture allows to generate any conversion ratio in the same way. Additionally a technique for increasing efficiency by recycling the charge stored in parasitic capacitances is presented, which reduced the losses due to this cause in 80%. An example of converter with four conversion ratios for a supply voltage of $2.8V$, load current up to $100\mu A$ in a $0.5\mu m$ CMOS process was designed and electrically simulated. The efficiency achieved for the 4/5 conversion ratio is above 77% for one order of magnitude of the load current.**

I. Introduction

The emergence of new ultra low power devices, such as nodes of wireless sensor networks, jointly with the growth of traditional ones, such as implantable devices, has increased the efforts to optimize the consumption of these devices and thus increase battery life.

Several techniques for energy reduction in digital circuits in these devices are related to voltage scaling, aimed at optimizing the supply voltage - energy consumption - speed trade off [1] and working as close to the minimum energy point as allowed by the required performance and tolerance to variability [2].

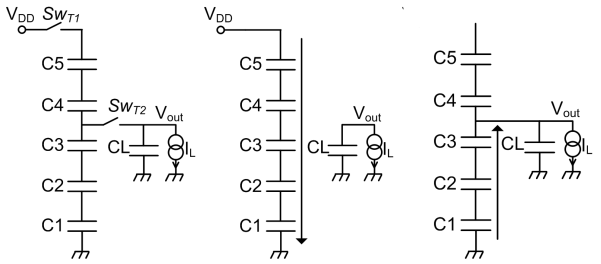
On the other hand, the scaling of CMOS process has decreased the maximum supply voltage tolerated by the Integrated Circuits, much below the voltage provided by different types of batteries, specially the different kinds of Lithium batteries applied in implantable devices, whose beginning of life voltage ranges from 2.8V to 3.7V [3]. Therefore, it becomes essential to be able to decrease the supply voltage from the battery voltage with high efficiency, even for μW consumption levels. The proposed integrated solutions to achieve these goals are based on switched-capacitor DC/DC converters (SC converters from now on) [4], [5]. One of the main energy loss mechanisms in SC converters are the conduction losses, associated to the energy loss when charge is transferred to a capacitor from a source (either the power supply or other capacitor) that is at a different voltage. The efficiency decreases as the voltage difference between the voltage in the capacitor to be charged and in the source of charge increases. In order to minimize this voltage difference, and hence the conduction losses, SC converters apply serial - parallel networks of capacitors for the capacitor charging phase and for the phase where the energy is delivered to the load. These networks need to be specially conceived for each of the phases and for each conversion ratio. This implies having a complex network of switches for assembling the required circuit topologies in each operating phase. An exception to this approach is the work of [6], where a reconfigurable architecture based on a standard unit cell for conversion ratios of 1/2, 1/3 and 2/3 is presented. This paper proposes a novel architecture for this type of converters with the advantage of being modular and capable of defining any conversion ratio in the same way.

Additionally, the present work proposes a novel technique to further increase efficiency. The efficiency is defined as the ratio between the energy delivered by the converter to the load and the energy taken by the converter from the supply voltage. The difference between these two energies is equal to the energy losses in the converter that can be classified as follows: E_{Cond} is the conduction loss previously defined, E_{CPar} is the energy lost due to charging and discharging to ground of parasitic capacitances (parasitic capacitance loss, also called bottom-plate loss), E_{Gates} is the energy expended in driving the gates of the switches, and in E_{logic} we will include the consumption of the digital circuit that manages the converter as well as the consumption of the analog circuit part of the control loop. Calling E_{Load} the energy delivered to the load, the efficiency is given by (1).

$$\eta = \frac{E_{Load}}{E_{Load} + E_{Cond} + E_{CPar} + E_{Gates} + E_{logic}}.100 \quad (1)$$

Losses due to parasitic capacitances (E_{CPar}) are usually the second loss factor in importance, after conduction losses [4], [5]. In our architecture we have incorporated a new feature to ”recycle” the parasitic capacitances charge instead of ”dumping” it to ground. Simple additions to our basic architecture allow to systematically use the charge available in parasitic capacitances that need to be discharged to charge those that need to be charged.

As a design case for assessing the proposed architecture we have considered the design of a converter with an input voltage of 2.8V, conversion ratios of ($\frac{1}{5}$, $\frac{2}{5}$, $\frac{3}{5}$ and $\frac{4}{5}$) and load current between $1\mu A$ and $100\mu A$ in a $0.5\mu m$ CMOS process. The capacitors applied are pMOS gate capacitors in parallel with poly1-poly2 capacitors in order to maximize the capacitance per area ratio.



(a) Basic Converter (b) Phase T1 (c) Phase T2

Fig. 1. Example of converter with n = 5 and conversion ratio of 3/5.

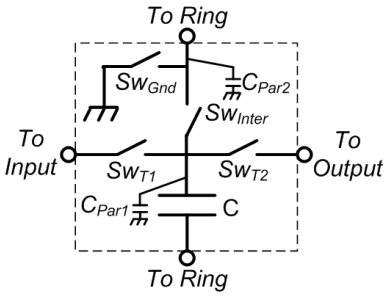
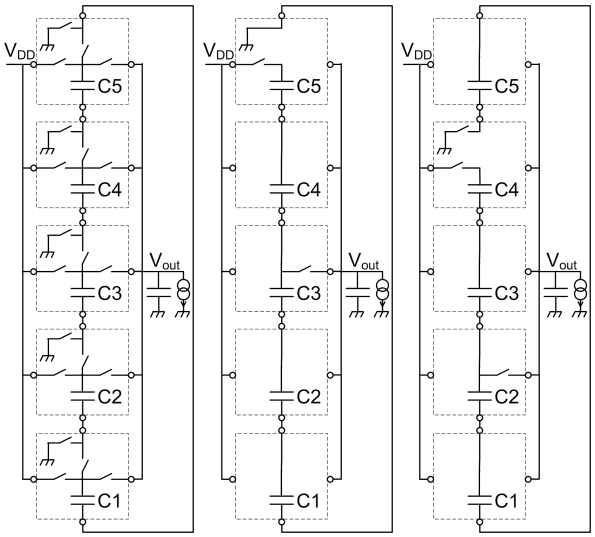


Fig. 2. Basic Capacitor Cell



(a) Ring with five Basic Capacitor Cells (b) Before rotation (c) After rotation

Fig. 3. Example of rotation in a five Basic Capacitor Cells ring

The paper is organized as follows. In Section II the proposed architecture is presented. In Section III the method for reducing parasitic capacitance losses is described. In Section IV and V the expected and simulated results are presented and the main conclusions of this work are summarized.

II. Proposed Architecture

The general idea of the architecture proposed in this work is to have n equal capacitors connected in series and step down the voltage through a capacitance divider. Additionally an output capacitor (C_L from now on) is always connected in parallel with the load. One end of the series of capacitors is always connected to ground. The circuit operates in two phases: $T1$ and $T2$ [1]. During $T1$, the other end of the series of capacitors is connected to the power supply voltage. During $T2$, the load and C_L are connected to an intermediate node of the series of capacitors. Therefore, the converter has $n-1$ conversion ratios (as many as intermediate nodes are in the series). Figure 1 shows a particular case with $n = 5$ and a conversion ratio of $\frac{3}{5}$.

In $T1$, since the power supply (V_{DD}) is connected to the capacitor series, the converter takes energy from it and all the capacitors in the series tend to a voltage $\frac{V_{DD}}{n}$, assuming equal capacitors. In this phase C_L gives charge to the load and maintains the output voltage V_{OUT}.

In $T2$, the converter gives charge to the load and returns to C_L the charge taken by the load during $T1$. The conversion ratio is defined by the node where the load is connected during this phase. As shown with an arrow in Figure 1(b), during phase $T1$ all the capacitors of the series take energy from the power supply. However, as shown with an arrow in Figure 1(c) during phase $T2$ only capacitors $C1..C3$ deliver energy to the load. The capacitors $C4$ and $C5$ are only receiving energy, so their voltages are increasing. This implies that the voltage in capacitors $C1..C3$ must decrease because during phase $T1$ the voltage of the series must be V_{DD}. So the output voltage will decrease too, cycle after cycle.

To solve this problem, capacitors are rotated of position in a ring. So instead of thinking about a series of capacitors it is better to imagine a ring which can be opened in every node as shown in Figure 3. All the capacitors of the ring are associated to a configuration of switches implementing a Basic Capacitor Cell shown in Figure 2.This cell is similar to the one proposed by [6], but used in a different way. The switches SW_{T1} y SW_{T2} connect the input and the output respectively, and the switches SW_{Inter} and SW_{Gnd} are used to open the ring and connect it to ground respectively. Two parasitic capacitances are associated to each Basic Capacitor Cell that are named C_{Par1} and C_{Par2} in the figure. Figure 3 shows an example where the ring is composed by five Basic Capacitor Cells. Figure 3(a) shows the ring with all the switches opened. Then in Fig. 3(b) and Fig. 3(c) the configuration of the ring before and after a rotation are shown. In the first one, the ring is opened in the Basic Capacitor Cell of capacitor $C5$ and the output is connected through the Basic Capacitor Cell of capacitor $C3$. After the rotation, the ring is opened in the Basic Capacitor Cell of capacitor $C4$ and the output is connected through the Basic Capacitor Cell of capacitor $C2$.

[1] $T1$ and $T2$ are used to represent both the phase and the duration of each phase.

III. Parasitic Capacitance Losses Reduction

As will be seen next, the parasitic capacitance losses in this architecture are the main source of loss if no actions are taken to reduce them. In the proposed architecture these losses occur

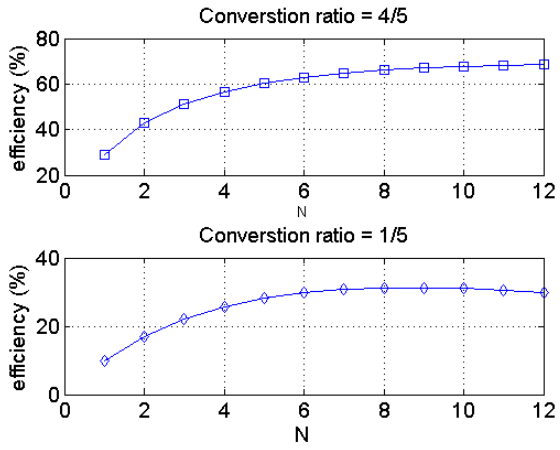


Fig. 4. Efficiency as a function of number of cycles between ring rotations (N), with @$I_L = 100\mu A$ and without the technique for parasitic capacitance losses reduction.

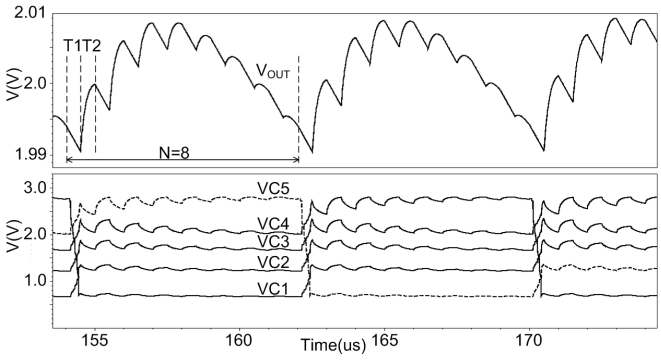


Fig. 5. Output and top plate waveforms.

when the ring is rotated because the voltages of the plates of the main capacitors respect to ground are changing.

A first measure for improving efficiency is to have N switching periods ($T1 + T2$), with $N > 1$, between rotations of the ring. N impacts mainly in two of the energies losses of the converter The larger the value of N is, the lower the output average voltage for a given conversion ratio and a given load current is. As the conduction loss depends on the difference between the output voltage and the no-load output voltage, the larger the value of N is, the larger the conduction losses are. So to minimize conduction losses we must minimize the value of N. On the other hand, the lower the value of N is, the larger the parasitic capacitances losses are, because there are more rotations of the ring. Therefore, there is a trade-off between conduction and parasitic capacitances losses that can be managed with the value of N.

To know which is the best value of N, a design space exploration was performed. This design space exploration was speeded up applying a numerical model of the converter operation. The developed model (which was checked against Spice simulations) allows to vary all the parameters of the design, such as the supply voltage, number and value of capacitors, size of switches, frequency and load current. The model returns the energy performance of the converter (efficiency, losses) and the output waveform. A very important feature of the developed model is that it allows the designer to perform a design space exploration of any technology with little effort. All the designer needs are some curves extracted from electrical simulation and some parameters of the technology. Figure 4 shows the efficiency as a function of N, for $100\mu A$ load current, the cases of conversion ratio of $4/5$ and $1/5$ (the largest and the smallest conversion ratios) and no other reduction technique applied for parasitic capacitance losses. From this analysis $N = 8$ was chosen, which being a power of 2 simplifies the design of the digital control circuitry.

An additional way of reducing losses due to parasitic capacitances arises from looking at the waveforms of the voltages in the circuit nodes. The waveforms resulting from the electrical simulation of the designed circuit for a $\frac{4}{5}$ conversion ratio and $100\mu A$ load current are shown in Figure 5. The upper graph shows the output voltage waveform (V_{OUT}). In the first $T1$ phase (marked in the figure) the ring is being rotated and the load is taking charge from C_L, so the output voltage is decreasing. In the next $T2$ phase the output voltage increases due to the charge supplied by the converter to C_L and the load. This process is repeated $N = 8$ times before the next rotation. It can be seen in the first three $T1 + T2$ periods that the output voltage is increasing, but due to the discharge of the capacitors that are delivering charge to the load, in the next five periods the output voltage decreases.

In the lower graph of the Figure 5 the top plate voltage of the five capacitors of the ring are shown. It can be seen how in the first rotation process the top plate voltage of the capacitor $C1$ goes from approximately V_{DD} to $V_{DD}/5$. The rest of the top plate voltages are increasing by $V_{DD}/5$ approximately. In the next rotation the same occurs with the top plate voltage of the capacitor $C5$, and so on.

The proposed method for reducing parasitic capacitance losses is based on the following principle. Consider for example the first transition where the parasitic capacitances connected to $C1$ top plate are discharged and the other parasitic capacitances must be charged. The idea is to use the charge stored in the parasitic capacitances connected to $C1$ top plate to charge the other parasitic capacitances. This can be achieved using a star of switches that connects the top plates of all capacitors to a common node. Then this switches are sequentially activated during the rotation process [7] so that the charge in the parasitic capacitances associated to $C1$ top plate is delivered to the rest of the parasitic capacitances. In the next section the improvement in efficiency achieved with this method is analyzed

IV. Results

This section presents the results of Spectre simulation of the designed converter. An output voltage control scheme based on controlling the switching frequency is considered. A switching frequency from 10kHz to 1MHz is applied. The analog blocks

TABLE I

COMPARISON WITH OTHER WORKS.

Design	[5]	[4]	This work
Technology (μm)	0.13	0.18	0.5
Chip Active area (mm^2)	0.52	0.57	10
Total On-Chip Cap (nF)	0.35	2.4	29
Conversion ratios *	2	4	4
V_{OUT} (V)	1.1-0.3	1.1-0.3	0.4-2
V_{DD} (V)	1.2	1.2	2.8
Minimum load current (μA)	1	10	1
Load power range (μW)	1-230	5-1000	0.4-200
Efficiency range (%)	80-30	80-50	78-35
Operating frequency (MHz)	0.1-6.5	15-3.75	0.01-1

* Unity conversion ratio is not considered

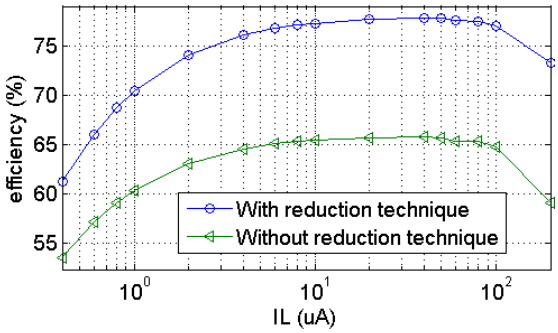


Fig. 6. 4/5 conversion ratio efficiency with and without parasitic capacitance losses reduction technique.

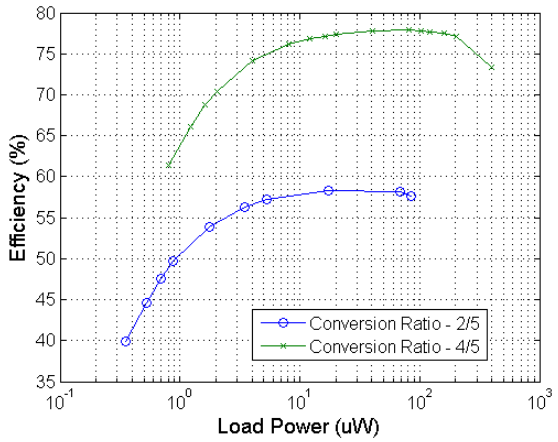


Fig. 7. Efficiency vs load power for the 2/5 and 4/5 conversion ratios.

of the control circuit are behaviorally modeled in the simulations and a constant consumption of $100nA$ is considered for efficiency calculations. Figure 6 shows the efficiency as a function of the load current for the $\frac{4}{5}$ conversion ratio, with and without the described charge recycling technique for parasitic capacitances losses reduction. This technique increased maximum efficiency from 66% to 78%, which corresponds to a reduction in parasitic capacitance losses of approximately 80%. Figure 7 displays the efficiency as a function of delivered power for $\frac{2}{5}$ and $\frac{4}{5}$ conversion ratios. Table I shows the general characteristics of the designed converter and makes a comparison with other works. From this comparison it can be seen that our architecture achieves similar performance, with increased flexibility due to its modular characteristic. The on-chip capacitor value used in this work is much bigger than the ones used by the two other works; this can be explained mainly in terms of the $0.5\mu m$ process applied, which was suitable for the 2.8V supply voltage considered. If this architecture were applied in a smaller feature process and with lower supply voltage, such as in [4], [5], the losses due to driving the gate of switches and due to the digital control circuit consumption will decrease, allowing to increase operation frequency and hence reduce the applied capacitors without jeopardizing the output resistance value. In fact [4] uses a switching frequency in the range $15 - 3.75MHz$. So if for example we can use a maximum switching frequency of $10MHz$ in a process with a smaller feature instead of $1MHz$, the total capacitance value can be reduced to $2.9nF$ keeping the same output resistance.

V. CONCLUSIONS

A novel architecture for Ultra Low Power Switched Capacitor DC/DC Converter was proposed. This architecture is modular and allows to easily add new conversion ratios. An example of Switched Capacitor Converter with five Basic Capacitor Cells was implemented. It was characterized in electrical simulation for the four conversion ratios and for load currents from $1\mu A$ to $100\mu A$. It was presented a technique based in "recycling" the charge stored in parasitic capacitances in order to decrease the energy lost due to this cause. The efficiency achieved is above 77% for one order of magnitude of the load current for the conversion ratio $4/5$.

VI. ACKNOWLEDGEMENTS

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