Variability-Speed-Consumption Trade-off in Near Threshold Operation

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Abstract. Sub-threshold operation is an efficient solution for ultra low power applications. However, it is very sensitive to process variability which can impact the robustness and effective performance of the circuit. On the other hand this sensitivity decreases as we move towards near-threshold operation.
In this paper, the impact of variability on sub-threshold and near-threshold circuit performance is investigated through analytical modeling and circuit simulation in a 65 nm industrial low power CMOS process. We show that variability moves the effective minimum energy point towards the near threshold region. Thus, we demonstrate that when variability is taken into account, a complete model that includes the near threshold (moderate inversion) region is necessary in order to correctly model circuit performance around the minimum energy point. Finally, we present the resulting speed-consumption trade-off in a variability-aware analysis of sub-threshold and near-threshold operation.

Keywords: Sub-threshold logic; Near-threshold operation; Variability; Modeling

1 Introduction

Over the last decade, sub-threshold logic has been used as an ideal option to achieve Ultra Low Energy consumption for applications with low demand in speed requirements. Here, sub-threshold term refers to the weak inversion (WI) region where the minimum energy can be achieved using a supply voltage V_{DD} well below the threshold voltage.

As the interest for ultra low energy has increased, research related to sub-threshold logic has attained considerable importance. Modeling and characterization of sub-threshold operation for standard CMOS cell designs have been investigated for energy and performance analysis[1][2].
However, several works have shown that variability in subthreshold logic, especially intrinsic one due to Random Dopant Fluctuations (RDF), is a critical limit

to achieve robust ultra low energy devices as it cannot be compensated through adaptive body biasing (ABB)[3][4][5]. As currents in weak inversion region exponentially depends on threshold voltage (V_t), random V_t variations significantly affect the on and off currents and gate delays and can affect the output swings and result in functional failures of some gates. Moreover, the minimum energy point can be strongly affected by variability. As reported in [6], device variability leads to 20% of minimum energy increase.

Models considering variability have been developed in previous works specifically for use in subthreshold, considering, therefore, just the weak inversion region. In this paper, we will show through 1K-point Monte Carlo Spice simulations in a Low Power (LP) technology from an industrial foundry that variability moves the effective minimum energy point towards the near-threshold region (Moderate Inversion). Thus, restrictive weak inversion models can no longer model circuit performance around the minimum energy point.
Therefore, we apply a complete and compact transistor model valid from weak to strong inversion in order to model the delay and energy performance over the weak and moderate inversion regions. This will allow us to correctly model the circuit performance in a variability aware analysis.

This paper is organized as follows. Section 2 presents the concept of subthreshold operation and investigates the impact of process variations on minimum energy point. In section 3, we propose a complete model that includes the near threshold region. We show through Monte Carlo Spice simulations that the new model is necessary to correctly model the circuit performance in a variability aware analysis.

2 Sub-threshold circuit design

In this section, the concept of sub-threshold operation is briefly explained. Variability impact on sub-threshold circuit performance through Monte Carlo Spice simulations of an inverter chain implemented in a Low Power technology from an industrial foundry is then presented.

2.1 Sub-threshold operation

Sub-threshold operation consist in reducing the power supply voltage V_{DD} below the threshold voltage V_T in order to achieve minimum energy consumption. The concept is simple: as P_{dyn} is proportional to the square of V_{DD}, a small reduction in supply voltage causes quadratic decrease in dynamic power consumption at the cost of a significant increase in delay. This results in an increase in leakage energy that leads to a minimum energy point achieved at an optimum supply voltage. In[7], authors provide an analytical solution for the optimum V_{DD} that minimize the energy for a given operating frequency.

However, lowering the power supply voltage will expose the circuit to the effect of process variations which can impact the functionality of the circuit and result in a functional failure of the gate. Thus, a process corners analysis

which determines the minimum operation voltage and the minimum transistor sizing which ensures a good functionality of the gate is the first step to do, as described in [2]. We have applied this analysis to an inverter from a 65nm Low Power industrial library. Figure 1 shows the limits for the ratio of the pMOS width to nMOS width, which must be between the minimum set by the Fast 0-Slow 1 (FS) corner and the maximum set by the Slow 0-Fast 1 (SF) corner in order to assure an output swing of 10%-90% of the supply voltage.

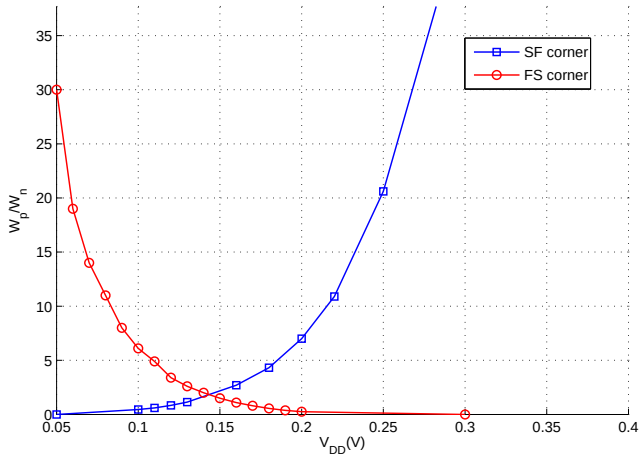

Fig. 1. Worst case corners analysis of the inverter for different supply voltage.

We observe that this restriction determines a minimum possible operating voltage, which for this technology occurs at 143mV by sizing the PMOS width to be 1.83 the NMOS one. We see that the inverter of the standard cell library is guaranteed to operate down to 160mV. Thus, if the minimum energy point is achieved by a supply voltage between 143mV and 160mV, a modified logic cell library should be created.

2.2 Variability effect on subthreshold circuit

Process variations is a critical limit of sub-threshold circuits. Intrinsic variations due to Random doping fluctuation (RDF) is considered to be the dominant source of variability in sub-threshold circuits [5].

To show the impact of variability on sub-threshold circuit performance, Monte Carlo Spice simulations with 1000 points have been performed for different values of V_{DD}. The considered benchmark circuit is a chain of inverters where the first inverters are not considered in order to correctly calculate the static current, increased due to the degeneration of stable states as mentioned in [1]. Since

delay variability depends on the logic depth of the circuit, an appropriate choice of the logic depth is essential. For our case study, we have choosen a logic depth of 23 like in [8] where the circuit is a standard 8-bit ripple-carry-array (RCA) multiplier.

Figure 2 shows the evolution of total energy consumption without and with variability effect, considering typical and 3σ worst case delay, respectively.

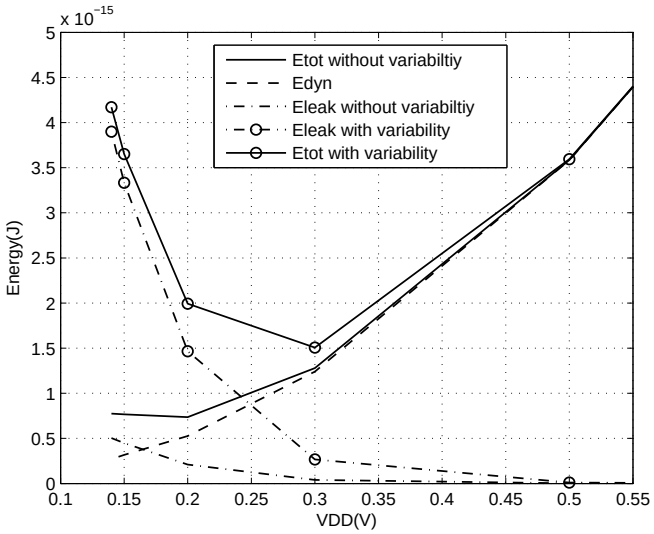

Fig. 2. Leakage and total energy evolution with and without variability.

We observe that variability leads to a considerable increase in leakage energy. This results in the increase of the minimum energy point by 50%, located now in the moderate inversion region.

3 Variability aware circuit model

In[1],[5] and [6], models in WI region are applied to describe sub-threshold operation. However, as we have seen in section 2, variability considerably affects the minimum energy point which moves in the moderate inversion region. In[1] the impact of operation in moderate inversion applying an all region transistor model is also considered, but the impact of variability is not analyzed in this case. [9] is another prior work where authors suggest to work in the near threshold voltage region in order to recover some of delay performance at the expense of a little energy increase. An energy-delay modeling framework that extends over all inversion regions is developed in this paper. But variability is still not considered in these models.

In this section, we present a variability aware model that extends over the weak and moderate inversion region. This model is based on the EKV model expressions [1]. The main contribution here is that we consider V_T and β variations in our analysis. We show through Spectre and Matlab simulations that the WI model in no longer sufficient to model the performance of a system exposed to process variations.

3.1 Current and delay model under variability analysis

In weak and moderate inversion region, the drain current can be expressed as[1]:

$$\begin{aligned} I_{DS} =& I_S(ln^2[1 + exp\frac{V_{GS} - V_T}{2nU_T}]- \\ & ln^2[1 + exp\frac{V_{GS} - V_T}{2nU_T}exp\frac{-V_{DS}}{2U_T}]) \end{aligned} \tag{1}$$

Where n is the subthreshold slope factor, V_{GS} and V_{DS} are respectively the gate to source and drain to source voltages and V_T is the threshold voltage. I_S is the specific current given by

$$I_S = 2n\mu C_{ox}U_T^2 W/L = 2n\beta U_T^2 \tag{2}$$

Where μ is the mobility, C_{ox} is the oxide capacitance, U_T is the thermal voltage and W/L denotes the channel width-length ratio of the transistor.
Equation 1 tends to the classical exponential WI model when $V_{GS} - V_T$ is negative.

The expression of delay can be derived from the current model as follows:

$$T_d = \frac{C_L V_{DD}}{I_{on}} \tag{3}$$

Where C_L is the load capacitance, V_{DD} is the supply voltage and I_{on} is the saturated on-current.

Leakage current is also determined from the I_{DS} expression when $V_{GS} = 0$. The model of Equation 1 is a long channel model that does not include effects such as mobility reduction, velocity saturation and drain induced barrier lowering (DIBL). The former two are mainly of impact in the strong inversion region and that is why, for simplicity sake, were not considered in this work. The last one (DIBL), has some impact on the performance in the WI and MI regions, as analyzed in [5]. In our case we considered the effect of DIBL when extracting the parameters for the model of Equation 1 by considering the drain current data of the 65nm Standard Threshold Voltage, Low Power (SVTLP) NMOS transistor with drain voltage equal to V_G. To extract model parameters, we have applied the method based on the gm/ID curve described in [10]. The following values were obtained:

- n = 1.22;
- V_T = 0.38(V);

– $\beta = 4.83e^{-4}(A/V^2)$.

Figure 3 shows the I_D versus V_{GS} for NMOS transistor determined with the weak inversion model, the complete model and spice simulations. As expected, the weak inversion model is not sufficient to model the current in near-threshold region. We observe that the complete model is not so accurate in strong inversion region due to the lack of modeling of mobility reduction and velocity saturation[10].

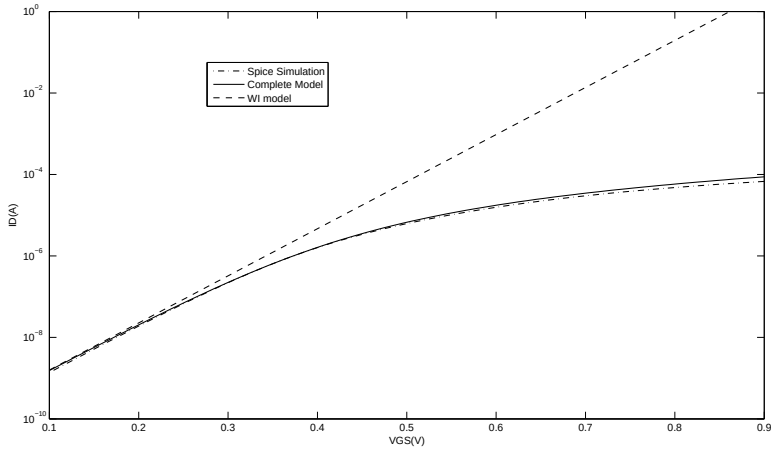

Fig. 3. I_D versus V_{GS} curves for NMOS transistor.

For variability analysis, we will consider just random V_T and β variations, modeled as a normal distributions ($\mu_{V_T}, \sigma_{V_T}, \mu_\beta, \sigma_\beta$), determined through Monte Carlo simulations or through analytical expressions given in [5]. Current model considering process variations is derived from Equation 1 by replacing β and V_T by values that follow the normal distribution described in the previous paragraph.

The evolution of typical and 3σ Worst Case(WC) delay is presented in Figure 4 (left). We observe that the complete model with and without variability consideration follow perfectly Monte-carlo Spice simulations whereas the delay of the WI model deviates from $0.3V$ of V_{dd}.

Figure 4 (right) plots delay variability versus the supply voltage. The simulated variability, obtained through Monte-Carlo simulations, shows that variability decreases as the supply voltage increases. We remark that delay variability, obtained with the WI model, remains constant at different supply voltage, while, the one obtained with the complete model presents the same shape as spectre simulations and has even close values.

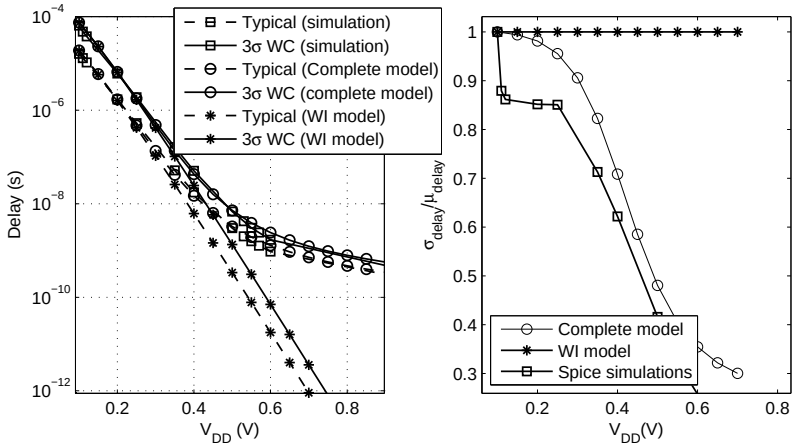

Fig. 4. Evolution of typical and WC delay (left), and normalized delay variability (right) for different V_{DD}.

We conclude that the WI model is a restrictive model that can not be used to model process variations and that the model developed, considering V_T and β variations, is a good model for variability analysis.

The delay model presented in Equation 3 is valid for a simple gate. For a circuit with a logic depth L_D, the delay will be $T_{circuit} = L_D.T_d$. If T_d is a normal distribution defined by (μ_{delay}, σ_{delay}), $T_{circuit}$ will be a normal distribution too defined by ($L_D.\mu_{delay}$, $\sqrt{(L_D)}.\sigma_{delay}$). Thus, the delay variability of the circuit can be obtained as follow:

$$var_{circuit-delay} = (1/\sqrt{(L_D)}).var_{gate-delay} \tag{4}$$

Table 1 lists delay variability for different Logic depth at $V_{DD} = 0.2V$.

Table 1. Delay variability for different logic depth at V_{dd}=0.2 V.

L_D	Delay variability ($\sigma_{delay}/\mu_{delay}$)	
	Spice simulation	**Analytical model**
1	0.86	0.99
7	0.28	0.36
15	0.25	0.26
23	0.205	0.209

As expected, the delay variability of a circuit decreases as its logic depth increases, and the decrease follows perfectly $1/\sqrt{(L_D)}$ law.

3.2 Energy model under variability analysis

The total energy consumed by the circuit is the sum of the dynamic energy E_{dyn}, required to charge and discharge parasitic capacitances during logic transitions, and static energy E_{stat} due to leakage currents I_{leak}. This can be summerized in the following expression :

$$E_{tot} = \alpha C_L V_{DD}^2 + V_{DD} I_{leak} T_{circuit} \tag{5}$$

Where α is the switching activity of the circuit and C_L is the load capacitance.

Here, we consider $Just - in - time$ operation [11], where the circuit works in its maximum frequency, i.e., the period is set to be the critical path delay of the circuit.

To consider variability in energy analysis, 3σ worst-case delay and mean I_{leak} are considered in the static energy calculation as follows

$$E_{stat} = V_{DD} \mu_{I_{leak}} \mu_{delay} (1 + 3 * \frac{\sigma_{delay}}{\mu_{delay}}) \tag{6}$$

Figure 5 shows the consumed energy under process variations consideration.

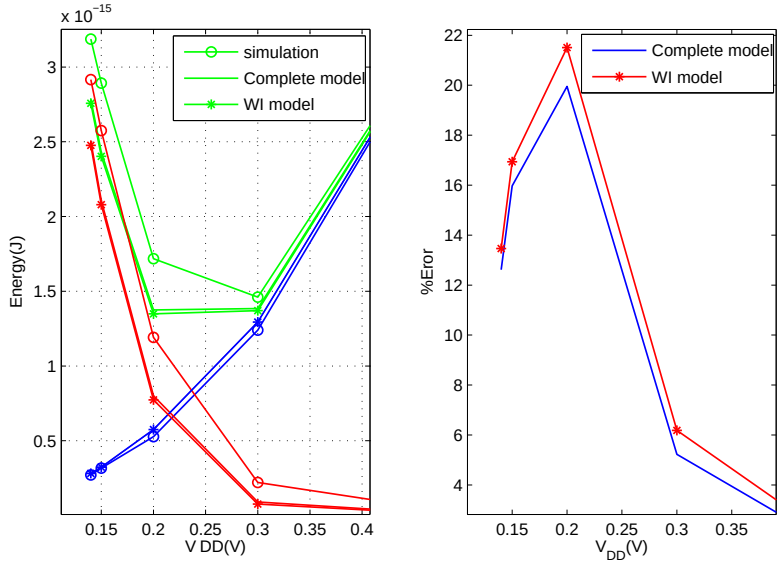

Fig. 5. Consumed energy under process variations (left), and % of complete and WI model error compared to Spice simulations (right).

We observe that the total energy consumed is slightly different from that determined by the models. The error of the energy on the minimum point is of

5% and 6%, when obtained by the complete and the WI model, respectively. Not what we expect, the error of the WI model is comparable to that of the complete model as shown in Figure 5 (right). This can be explained by the inverse tendency of variability and delay determined by the WI model. On the one hand, the variability of the WI model is constant whatever the value of the supply voltage. It is therefore overestimated in the moderate and strong inversion regions. On the other hand, the delay obtained by the WI model is underestimated with respect to the one obtained by Spice simulations as observed in Figure 4.
As the energy contains the product of variability and the delay, there is a compensation that let the WI model remain a good model of energy consumption even under variability analysis.

4 Conclusion

In this paper, modeling under variability analysis is investigated. We show that the Weak Inversion model, normally used to describe sub-threshold circuit, is a restrictive model that can no longer model circuit delay around the minimum energy point of circuit exposed to process variations.

We develop a complete model that extends over the weak and moderate inversion regions. Through Monte Carlo Spice simulations of a chain of inverters in a Low Power technology, we show that the new model is necessary to correctly model the variability of the circuit.

Nevertheless, instead of what may be expected, the Weak Inversion model remains a good model of energy consumption even under variability analysis. This is due to the compensation of delay and variability errors resulting when the WI model is applied.

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