A MOSFET-only Voltage Source with Arbitrary Sign Adjustable Temperature Coefficient

Conrado Rossi-Aicardi, Julián Oreggioni, Fernando Silveira
Instituto de Ingeniería Eléctrica
Universidad de la República
Montevideo, Uruguay
Email: {cra, juliano, silveira}@fing.edu.uy

Carlos Dualibe
Service d'Electronique et de Microelectronique
Université de Mons
Mons, Belgium
Email: fortunato.dualibe@umons.ac.be

***Abstract*— A MOS-diode biased by a constant inversion level current source is a simple MOSFET-only circuit that implements a voltage source with a linear temperature dependence. Through adjustment of the inversion level, the temperature slope may be changed from negative to positive, including the constant voltage condition. A test circuit, fabricated on a $0.35\,\mu\mathrm{m}$ CMOS technology, was measured from $300\,\mathrm{K}$ to $375\,\mathrm{K}$ while sweeping the inversion coefficient from 0.06 to 180. The theoretical model agrees with the measured data, accurately predicting the temperature slope. The presented all-region continuous model is especially useful at and near zero temperature slope operation.**

I. Introduction

Voltage sources, either constant-value or those exhibiting a linear temperature dependence, are ubiquitous in analog, mixed-signal and temperature sensor design [1], [2]. Common examples of linear temperature dependence circuits are PTAT (Proportional to Absolute Temperature) and CTAT (Contrary to Absolute Temperature) voltage generators.

Biasing of simple circuits with a constant inversion level current source (Section III-A) showed promising preliminary results [2]–[4]. This paper shows that biasing a saturated MOSFET with such a current leads to a simple, all-MOS circuit implementing a voltage source whose temperature slope can be chosen in a wide range from negative to positive values, including the case of constant voltage.

Compact models, such as ACM [5], [6], able to model the MOS transistor continuously through all inversion levels, have been widely applied to analog design at a constant temperature. The short number of main parameters in ACM lends the model very convenient to introduce temperature variations as already shown for the MOS divider in [4].

Next section reviews the ACM model for convenient reference. Section III applies ACM to modeling the temperature characteristics of the proposed circuit. Sections IV and V describe a test circuit and the measurements we performed. Section VI compares these results to the theoretical model while Section VII draws final conclusions.

II. ACM Model Review

This section presents the notation that we use throughout the paper and a brief review of the ACM model for the long channel MOS transistor [3], [4].

Absolute temperature T will often be expressed relative to a reference temperature (usually $\mathrm{T_R} = 300\,\mathrm{K}$) as:

$$\theta = \frac{T}{T_R}\,. \tag{1}$$

The R subscript will be applied to any variable taken at the reference temperature. The thermal voltage will be denoted as

$$U_{TR} = \frac{kT_R}{q}\,, \quad U_T = \frac{kT}{q} = \theta\, U_{TR} \tag{2}$$

where k is Boltzmann's constant and q is the electron charge.

ACM [6] expresses the drain current of a MOSFET as the difference between forward and reverse currents:

$$I_D = S\, I_{SQ}(i_f - i_r)\,, \quad S = W/L \tag{3}$$

where $\mathrm{i_f}$ and $\mathrm{i_r}$ are the forward and reverse inversion coefficients and W, L are the effective width and length of the MOS transistor. Usually, $\mathrm{i_f} = 1$ is considered an upper bound for the weak inversion (WI) region and $\mathrm{i_f} = 100$ a lower bound for strong inversion (SI) operation. The sheet normalization current is defined as

$$I_{SQ} \;=\; \frac{1}{2}\, n\, \mu C_{ox}\, {U_T}^2 \tag{4}$$

where n is the subthreshold slope factor, μ is the mobility of carriers in the MOS channel and $\mathrm{C_{ox}}$ is the gate capacitance per unit area.

The relationship between the terminal voltages $\mathrm{V_G}$, $\mathrm{V_S}$, $\mathrm{V_D}$ (all referred to the bulk) and the inversion coefficients is

$$\frac{V_P \,-\, V_{S(D)}}{U_T} \;=\; \mathcal{F}\left(i_{f(r)}\right) \;\equiv \\ \sqrt{1 + i_{f(r)}} \,-\, 2 \,+\, \ln\left(\sqrt{1 + i_{f(r)}} - 1\right). \tag{5}$$

The pinchoff voltage $\mathrm{V_P}$ depends on $\mathrm{V_G}$ through a rather complex expression [6], but is very well approximated by

$$V_P = \frac{(V_G - V_T)}{n} \tag{6}$$

where $\mathrm{V_T}$ is the threshold voltage.

The inverse function of $\mathcal{F}\,()$ is denoted as:

$$i_{f(r)} \;=\; \mathcal{F}^{-1}\left(\frac{V_P \,-\, V_{S(D)}}{U_T}\right). \tag{7}$$

III. Temperature model at constant inversion level

A. Constant inversion level current source

Some circuits, even simple ones, exhibit interesting temperature properties when biased by a current source that imposes a constant inversion coefficient in spite of varying temperature. This characteristic is easily obtained with the MOSFET-only circuit on Fig. 1 [2], [4], [7], [8] yielding a current $\mathrm{I_{bias}}$ proportional to the sheet normalization current $\mathrm{I_{SQ}}$.

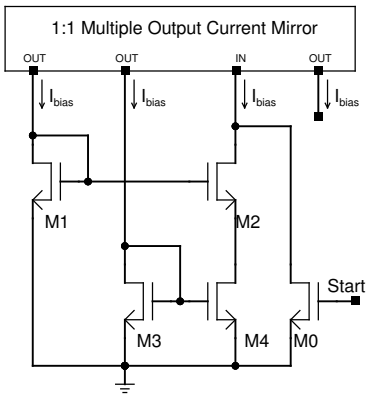

Fig. 1. MOSFET-only constant inversion level bias generator

As stated in [4], the following equations determine the inversion levels for every transistor in the circuit:

$$S_1 i_{f1} = S_2 i_{f2} = S_3 i_{f4} = S_4 (i_{f4} - i_{r4}) , \quad (8)$$

$$\mathcal{F}(i_{f1}) - \mathcal{F}(i_{f2}) = \mathcal{F}(i_{f4}) - \mathcal{F}(i_{r4}) . \quad (9)$$

These inversion levels depend neither on temperature nor on technology parameters but only on size ratios. Referring the output to the current through $\mathrm{M_2}$:

$$I_{bias} = S_2 \, i_{f2} \, I_{SQ} . \quad (10)$$

B. Constant inversion level saturated MOSFET

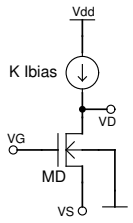

Fig. 2. MOSFET biased by a constant inversion level bias current

We will apply a current that is proportional to $\mathrm{I_{bias}}$ on Fig. 1 to a saturated MOS transistor $\mathrm{M_D}$ (Fig. 2). For the condition to hold, some kind of external feedback from the drain current to the gate voltage must be established. The most simple case, used in Section IV, is the direct connection of the gate and drain terminals as in a MOS-diode. Nevertheless, the following theory holds for a general case as long as the MOSFET is saturated.

With such current imposed to the drain of $\mathrm{M_D}$ (Fig. 2), considering Eq. 3 and that in saturation $\mathrm{i_r \ll i_f}$:

$$I_D = K \, I_{bias} = S_D \, I_{SQ} \, (i_{fD} - i_{rD}) \simeq S_D \, I_{SQ} i_{fD} . \quad (11)$$

Thus, using Eq. 10,

$$i_{fD}(K) = K \, \frac{I_{bias}}{S_D \, I_{SQ}} = K \, \frac{S_2 i_{f2}}{S_D} \equiv K \, i_{fD0} \quad (12)$$

is also temperature and technology independent as $\mathrm{i_{fD0}}$ is only determined by ratios among $\mathrm{S_1}$, $\mathrm{S_2}$, $\mathrm{S_3}$, $\mathrm{S_4}$ and $\mathrm{S_D}$.

From Eq. 5,

$$V_P - V_S = U_T \, \mathcal{F}(K \, i_{fD0}) . \quad (13)$$

If $\mathrm{V_S}$ is PTAT or $\mathrm{V_S = 0}$ ($\mathrm{V_S = \theta \, V_{SR}}$, $\mathrm{V_{SR} \geq 0}$), then $\mathrm{V_P}$ is PTAT. Using Eq. 6 we obtain:

$$V_G = V_T + n\theta \left[V_{SR} + U_{TR} \mathcal{F}(K \, i_{fD0}) \right] . \quad (14)$$

The main property of using the constant inversion level bias generator is the compensation of the $\mathrm{I_{SQ}}$ related temperature dependence in the biased circuit. In particular it eliminates the mobility related temperature dependence.

For a first order analysis, we consider a linear dependence of $\mathrm{V_T}$ with temperature [9]:

$$V_T = V_0 + k_{VT} \theta , \quad k_{VT} < 0 , \quad V_0 = V_{TR} - k_{VT} \quad (15)$$

where $\mathrm{V_0}$ is the extrapolation of $\mathrm{V_T(T)}$ to $\mathrm{0\,K}$. With this approximation, and neglecting the slight dependence of n with temperature :

$$V_G = V_0 + k_D \theta , \quad (16)$$

$$k_D = k_{VT} + n \left[V_{SR} + U_{TR} \mathcal{F}(K \, i_{fD0}) \right] , \quad (17)$$

that is, the gate voltage exhibits a linear temperature dependence which extrapolates to $\mathrm{0\,K}$ to the technology dependent parameter $\mathrm{V_0}$. Varying the inversion level (through K) and/or $\mathrm{V_{SR}}$ allows the designer to choose the slope $\mathrm{k_D}$ throughout a wide range of negative, null or positive values. This way, the circuit is suitable for constant voltage and adjustable temperature slope voltage generators.

In order to design a constant voltage source ($\mathrm{k_D = 0}$) it is enough to choose the inversion level of the saturated transistor as

$$i_{fD} = \mathcal{F}^{-1} \left(- \frac{k_{VT}}{n \, U_{TR}} - \frac{V_{SR}}{U_{TR}} \right) . \quad (18)$$

If necessary, the condition in Eq. 18 can be fulfilled by calibration.

A single bipolar diode cannot attain the constant voltage condition as our circuit does (with $\mathrm{V_S = 0}$). In that case, the constant value should have to be the bandgap voltage, much higher than practicable.

The preceding analysis is valid for all the MOSFET operating regions. This is particularly important as, in many circuits, transistors operate in moderate inversion (MI) for an optimum area-power tradeoff. Moreover, substituting usual values for the technology parameters in Eq. 18 (Table I) shows that (for $\mathrm{V_{SR} = 0}$) the condition $\mathrm{k_D = 0}$ is fulfilled in the MI region.

IV. Test Circuit

Following the theory presented in the precedent section, we designed a test circuit subsequently fabricated on a $0.35\,\mu\mathrm{m}$ CMOS technology (Fig. 3). Among other test structures,

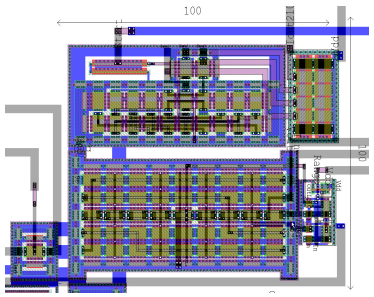

Fig. 3. Layout of test circuit

the circuit includes a constant inversion level bias current generator (Fig. 1) and a MOS transistor externally connected as an MOS-diode ($\mathrm{V_G = V_D}$), a simple way to ensure the saturation condition. For simplicity, the MOSFET source is grounded, making $\mathrm{V_{SR} = 0}$. In order to improve matching, transistors $\mathrm{M_1}$ to $\mathrm{M_4}$ in the bias generator are formed by series and parallel associations of a unit MOSFET sized $\frac{4\,\mu\mathrm{m}}{6\,\mu\mathrm{m}}$. The diode-connected MOS transistor is also the same size.

V. Experimental Measurements

The temperature characteristics of the fabricated circuit were measured inside a custom temperature-controlled oven stabilized to less than $\pm 25\,\mathrm{mK}$. A semiconductor parameter analyzer (HP 4155) was connected to the chip pins through suitable connectors available in the oven (Fig. 4). Measurements were taken at several temperatures ranging from 300 K to 375 K (approximately 27 °C to 102 °C), close to the commercial temperature range.

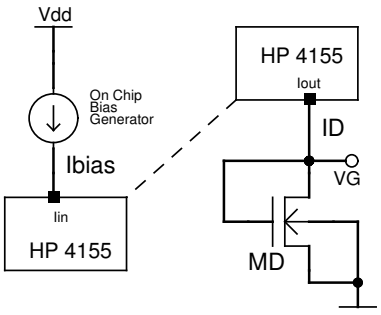

Fig. 4. Measurement Setup

Fig. 5 shows the measured temperature dependence of the constant inversion level bias generator for a typical chip. As expected, the current increases slightly with temperature which is a characteristic of its constant inversion level operation [2], [3].

At each temperature we also measured the $\mathrm{V_G(I_D)}$ curves for the diode-connected MOS transistor as shown on Fig. 6.

We then proceeded to evaluate the MOS-diode temperature behaviour at several constant inversion levels. For the sake of

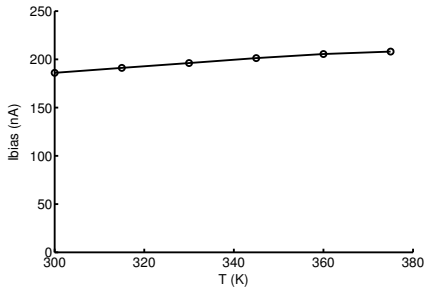

Fig. 5. Constant inversion level bias generator temperature dependence

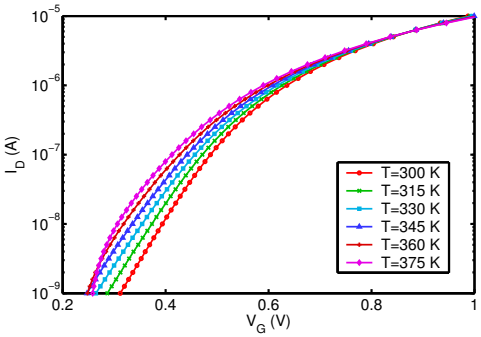

Fig. 6. MOS-diode at different temperatures

flexibility, this evaluation was performed numerically based on the aforementioned measurements.

For each temperature, we selected fixed multiples of $\mathrm{I_{bias}(T)}$:

$$I_D(K,T) = K I_{bias}(T) \tag{19}$$

with K taking on values ranging from 0.02 to 60 (Fig. 7). For each $\mathrm{I_D(K,T)}$, we searched through the measured $\mathrm{V_G(I_D,T)}$ curve to obtain the MOS-diode voltages corresponding to the chosen multiples (K) of $\mathrm{I_{bias}}$. The search was performed through b-spline interpolation for greater accuracy.

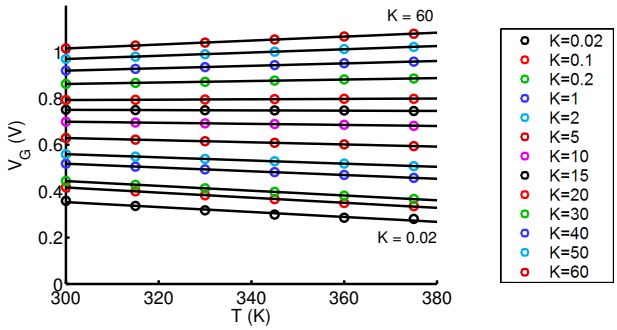

Fig. 7. Experimental data and fitted straight lines

This way we obtained points on the $\mathrm{V_G(K,T)}$ function which are plotted as circles on Fig. 7. The lines are best fits to the data showing that, as predicted by Eq. 16, $\mathrm{V_G(T)}$ are very close to straight lines. Their slopes depend on K, ranging from

TABLE I

FITTED TECHNOLOGY PARAMETERS AND INVERSION LEVEL

V_{TR}	519 mV
n_R	1.38
k_{VT}	-244 mV
V_0	763 mV
i_{fD0}	2.95

negative to positive as the inversion level increases from WI to SI. Considering $i_{fD0} \simeq 3$ as obtained on section VI (Table I), the inversion coefficients (Eq. 12) range approximately from 0.06 to 180.

VI. Analysis of Results

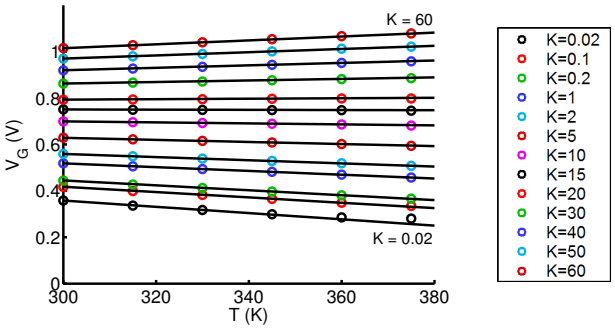

Fig. 8. Experimental data compared to Eqs. 16 and 17 using parameters from Table I

We compared the measured and predicted values of $V_G(T)$ for the set of factors K. Table I shows the parameters in Eqs. 16 and 17 which were found as follows. As the MOS was connected such that $V_S = 0$ then $V_{SR} = 0$. The parameters k_{VT}, $V_0 = V_{TR} - k_{VT}$, n are technology related while $i_{fD0} = \frac{S_2 i_{f2}}{S_D}$ depends only on ratios of transistor sizes. The values of V_{TR}, n and i_{fD0} were determined from data at $T = T_R$ ($\theta = 1$) by fitting Eq. 14 to the measured data through minimizing

$$\sum_K \left| V_{TR} + nU_{TR}\mathcal{F}\left(Ki_{fD0}\right) - V_G(K) \right|. \qquad (20)$$

The value for k_{VT} was obtained from fitting the slopes $k_D(K)$ of the lines on Fig. 7 to Eq. 17.

Fig. 8 shows the plot of Eq. 16 for each value of K as lines on top of the experimental data $V_G(K, T)$. The difference between theory and experiment is shown on Fig. 9, exhibiting a good agreement throughout all the inversion ranges. In WI, the increasing errors at high temperature are attributed to leakage currents.

VII. Conclusions

We proposed a simple MOSFET-only circuit that generates a voltage with linear temperature dependence. This can be adjusted from decreasing to increasing as the inversion level

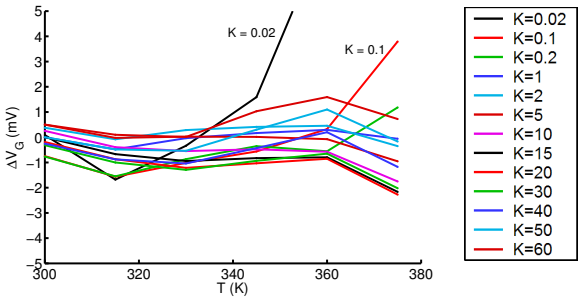

Fig. 9. Difference between theory and experiment

is varied from WI to SI. With proper calibration a constant voltage can also be obtained.

Based on ACM, we developed a model for the circuit which is continuous over the full inversion level range.

The model was experimentally verified.

Acknowledgments

This work was partially funded by PDT project 69/08 and by the Uruguayan Agency for Research and Innovation (ANII) under grant PR-POS-2008-003. The authors are grateful to Prof. Márcio Schneider at UFSC, Florianópolis, Brasil, for suggesting to design the test chip and fruitful discussions thereof, Marianela Rivero for her kind collaboration with layout and the MOSIS Educational Program for their support with chip fabrication. A stay of C. Rossi at UFSC leading to this work was financed by CSIC/UdelaR.

References

[1] P. Mok and K. N. Leung, "Design considerations of recent advanced low-voltage low-temperature-coefficient CMOS bandgap voltage reference," in *Proceedings of the IEEE Custom Integrated Circuits Conference 2004*, Orlando, FL, USA, Oct. 2004, pp. 635 – 642.

[2] P. Aguirre and C. Rossi, "Architecture and cells for micropower temperature sensors," in *Proceedings of the X Iberchip Workshop*, Cartagena de Indias, Colombia, Mar. 2004, pp. 1–10.

[3] C. Rossi and P. Aguirre, "Ultra−low power CMOS cells for temperature sensors," in *Proceedings of the 18th Annual Symposium on Integrated Circuits and System Design, SBCCI 05*. Florianópolis, Brasil: ACM Press, Sept. 2005, pp. 202–206.

[4] C. Rossi, C. Galup-Montoro, and M. C. Schneider, "PTAT voltage generator based on an MOS voltage divider," in *Technical Proceedings of the 2007 NSTI Nanotechnology Conference and Trade Show*, vol. 3, Santa Clara, CA, USA, May 2007, pp. 625–628.

[5] A. I. A. Cunha, M. C. Schneider, and C. Galup-Montoro, "An MOS transistor model for analog circuit design," *IEEE J. Solid-State Circuits*, vol. 33, no. 10, pp. 1510–1519, Oct. 1998.

[6] C. Galup-Montoro and M. C. Schneider, *Mosfet Modeling For Circuit Analysis And Design*. World Scientific Pub. Co., 2007.

[7] H. J. Oguey and D. Aebischer, "CMOS current reference without resistance," *IEEE J. Solid-State Circuits*, vol. 32, no. 7, pp. 1132–1135, July 1997.

[8] E. M. Camacho-Galeano, C. Galup-Montoro, and M. C. Schneider, "A 2-nW 1.1-V self-biased current reference in CMOS technology," *IEEE Trans. Circuits Syst. II*, vol. 52, no. 2, pp. 61–65, Feb. 2005.

[9] I. Filanovsky and A. Allam, "Mutual compensation of mobility and threshold voltage temperature effects with applications in CMOS circuits," *Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on*, vol. 48, no. 7, pp. 876 –884, Jul. 2001.