High CMRR Power Efficient Neural Recording Amplifier Architecture

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***Abstract*—This work presents an architecture of neural recording amplifier based on a modified differential difference amplifier (DDA). The proposed circuit improves the performance with respect to capacitive feedback neural amplifiers and standard DDA based amplifiers by taking advantage of the high CMRR achievable in a DDA without jeopardizing the power consumption. In addition a novel technique for rejecting the DC component at the output of the amplifier and fixing the low cut-off frequency is described. The expected performance of the circuit is checked by Monte Carlo simulation, achieving 48dB gain in a 250Hz-8kHz bandwidth, with higher than 107dB CMRR (@5kHZ), 2.4μVrms input noise and 4.2 noise efficiency factor at a total current consumption of 16.5μA from a 3.3V power supply in a 0.5μm CMOS technology.**

I. Introduction

The research on the application of microelectronic devices for interacting with the neural system and the brain has strongly intensified in the last two decades, oriented to, both, neuroscience research and medical application. One of the key elements for implementing these systems is the low noise, low power neural amplifier that handles acquired signals, which can be as small as a few μVs in amplitude. This signal is usually superposed to undesired signals of much higher amplitude. On one hand there is a differential mode DC component of tens of mVs or more related to polarization effects at the electrode - tissue interface. Therefore the input amplifier must be capable of rejecting this DC component. On the other hand, depending on the type of electrodes applied (e.g. cuff electrodes around nerves as in [1] or invasive neuron recordings [2]), and the positioning and design of these electrodes, in some cases (specially in cuff electrodes) high levels of common mode interfering signals from muscles and ambient electromagnetic noise are present. In addition, common mode interference may come from stimulation. So a high common mode rejection ratio (CMRR) is needed. One power efficient alternative is the one presented in [3]. This architecture, though simple, has two drawbacks. First, CMRR is limited by capacitor matching. In [3] the expected CMRR is higher than 42dB and the measured one higher than 80dB (though it is not stated on how many samples). In [4], where the same architecture is applied for the front-end amplifier, CMRR is 66dB. Second, in these architectures the high pass cut-off characteristic at low frequency is fixed by the use of an MOS-bipolar pseudoresistor element as a high-resistance element. The resistance of this component is difficult to accurately model and control, and may also suffer from drift.

This work aims at improving these two characteristics, without jeopardizing the power consumption, through the use of novel architecture based on a modified differential difference amplifier (DDA) [5]. DDAs are a known alternative for building an instrumentation amplifier [5], [6] taking advantage of one differential input for the signal to be amplified and the second differential input for the feedback that fixes the gain and bandpass characteristic. The DDA architecture, when the input signals are directly coupled to one of the differential inputs is intrinsically suitable for high CMRR because the CMRR is based on a differential pair common mode rejection. It has been applied to neural signal acquisition in [7] [8] [1] and [9], among other works. In [9] the DDA architecture has been applied combined with the architecture of [3], keeping the capacitor feedback network, and therefore keeping the CMRR limitation. The implementation in [7] consumes 900μW. [1] applies a standard DDA architecture. This work proposes a new approach of a neural recording amplifier architecture based on DDA that significantly decreases consumption with respect to a standard DDA architecture and improves the performance in terms of CMRR and design of the low cut-off frequency with respect to a capacitive feedback architecture ([3], [4]). This is achieved while maintaining the noise vs. power efficiency. This architecture is validated by simulation (including Monte Carlo simulation) of a circuit for a front-end neural recording amplifier in a 0.5μm CMOS technology with 48 dB of gain, 250Hz to 8 kHz bandwidth, 16.5 μA of consumption, a noise efficiency factor of 4.2 and more than 107 dB of CMRR.

The paper is organized as follows. Section II describes the proposed architecture. Section III presents the noise analysis and circuit design. Section IV show the simulation results and Section V summarizes the main conclusions

II. Proposed Architecture

The proposed architecture is shown in Fig.1 and it is based on a DDA composed of two OTAs (Operational Transconductance Amplifier) shown as $Gm1$ and $Gm2$ and a feedback gain β. The architecture shares with other

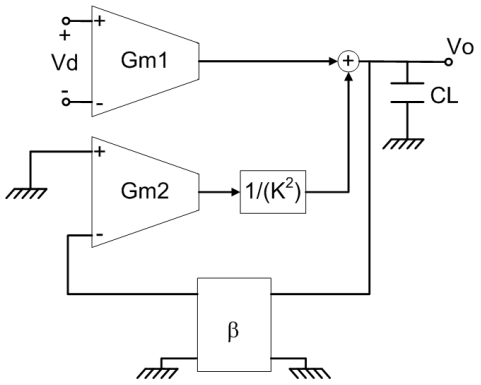

Figure 1. Proposed Architecture

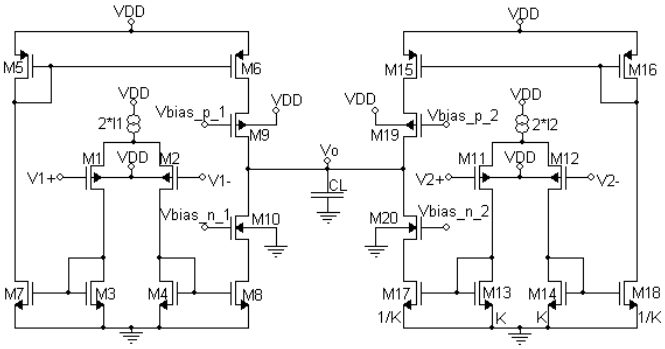

Figure 2. Implementation at transistor level of the open loop DDA

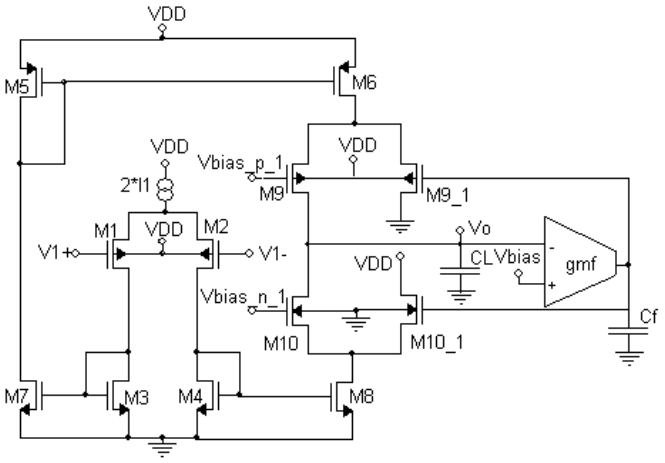

Figure 3. Offset Compensation.

DDA based architectures the characteristic of providing a differential input (the one of $Gm1$) for the signal to be amplified, with very good common mode rejection characteristics, due to the differential pair structure. On the other hand $Gm2$ provides a path for feedback. In Fig.1 a single feedback path to the Gm2 inverting input is shown. It could be applied one feedback path for the inverting input for fixing the gain and another one to the non-inverting input (for example with an inverting integrator) for setting the amplifier high pass characteristics as in [6] [7] [8]. The actual feedback structure applied in our case is discussed later.

One of the contributions of this work is to propose the use of an "assymetrical" DDA that improves the noise-consumption trade-off of the overall amplifier, which can be represented in the noise efficiency factor(NEF) [10]. The DDA is assymetrical in the sense that the transconductance Gm1 is different from Gm2 and the output current of $Gm2$ is further reduced by the $\frac{1}{K^2}$ factor. When a standard DDA is used to implement an instrumentation amplifier, with $Gm1 = Gm2$ and $K = 1$, the noise of $Gm2$ contributes to the input as much as the noise of Gm1, therefore degrading the NEF. By making $Gm2 < Gm1$ and $K > 1$, the noise contribution of $Gm2$ is made negligible, as will be shown in the next section, where the expression for the equivalent input noise is derived.

The implementation at transistor level of the two OTAs, $\frac{1}{K^2}$ factor and summing block is shown in Fig.2.

The summing block is obtained just joining the two OTAs outputs and thus adding their output currents. The $\frac{1}{K^2}$ factor is merged into $Gm2$, implementing it with the gain of the current mirrors inside Gm2. In this way the $\frac{1}{K^2}$ factor is implemented without additional circuitry and since the current at the output branch of $Gm2$ is reduced, the consumption is reduced with respect to an implementation with separate blocks for $Gm2$ and $\frac{1}{K^2}$. A cascoded current source is used for $2 * I1$ in $Gm1$ in order to enhance the CMRR.
A potential drawback of this asymmetrical architecture is that the reduction of the current provided by $Gm2$ to the summing node with respect to the current provided by $Gm1$, decreases the range of offset currents at the Gm1 output (associated with the offset and DC differences at $Gm1$ input) that the feedback through $Gm2$ can compensate. This is improved through a second novel approach of this work. The high pass cut-off frequency of the amplifier (and the aforementioned compensation of the DC component at the output of $Gm1$) is fixed through a local feedback at $Gm1$ output (not shown in Figs.1 and 2 for simplicity sake).

Fig.3 shows that implementation. For example, if V_o is higher than V_{bias}, the output of the local feedback transconductor (gmf) will decrease. Then $M9\_1$ will take more current (and $M9$ less) and $M10\_1$ will take less current (and $M10$ more). This will happen until the moment when V_o equals V_{bias} (except for the offset and finite gain error of gmf). gmf and Cf fix the low cut-off frequency.

In order to explain the selection of the feedback factor β, let us first analyze the expression of the close loop gain of the proposed architecture of Fig.1. We will call $A1(s)$ and $A2(s)$, the first order, dominant pole, approximation for the open loop gain from the input of respectively $Gm1$ and $Gm2$ to the V_o output. The dominant pole for $A1(s)$ and $A2(s)$ will

be given by the output node time constant (which is the node with the highest associated resistance), therefore it will be the same for $A1(s)$ and $A2(s)$. We will refer as ω_P to the angular frequency of this dominant pole Thus:

$$A1(s) = \frac{A1_0}{1 + \frac{s}{\omega_P}} \tag{1}$$

$$A2(s) = \frac{A2_0}{1 + \frac{s}{\omega_P}} \tag{2}$$

Where $A1_0$ and $A2_0$ are the corresponding low frequency gains. Calling R_o^{Total} the resistance at the output node V_o:

$$A1_0 = R_o^{Total}.Gm1 \tag{3}$$

$$A2_0 = \frac{R_o^{Total}.Gm2}{K^2} \tag{4}$$

$$f_P = \frac{1}{2.\pi.R_o^{Total}.C_L} = \frac{\omega_P}{2.\pi} \tag{5}$$

where $Gm1$ and $Gm2$ are the transconductances of the corresponding blocks and C_L the capacitance at the node V_o. Solving for the closed loop gain in Fig.1, we have:

$$\frac{V_o}{V_d} = \frac{A1(s)}{1 + A2(s).\beta} \tag{6}$$

and substituting Equations 1 and 2 we have that:

$$\frac{V_o}{V_d} = \frac{\frac{A1_0}{1+A2_0.\beta}}{1 + \frac{s}{(1+A2_0.\beta).\omega_P}} \tag{7}$$

So the in-band gain A_0 and dominant pole angular frequency ω_H of the closed loop transfer function are:

$$A_0 = \frac{A1_0}{1 + A2_0.\beta} \approx \frac{A1_0}{A2_0.\beta} = \frac{Gm1.K^2}{Gm2.\beta} \tag{8}$$

and:

$$\omega_H = (1 + A2_0.\beta).\omega_P \approx (A2_0.\beta).\omega_P = \frac{Gm2.\beta}{K^2.C_L} \tag{9}$$

where the approximations assume that $A2_0.\beta >> 1$ and the last equality in equation 8 stems from equations 3 and 4 and in equation 9 stems from equations 4 and 5.

If we express these two equations as a function of the parameters of the transistors, we have that:

$$A_0 = \frac{gm_{1in}.K^2}{gm_{2in}.\beta} \tag{10}$$

and

$$f_H = \frac{gm_{2in}.\beta}{2.\pi.K^2.C_L} \tag{11}$$

Where gm_{1in} and gm_{2in} are the transconductances of the transistors of the differential input pair of $Gm1$ and $Gm2$ respectively.

Therefore, provided $A2_0.\beta >> 1$, this architecture allows us to fix the closed loop gain A_0 as a function of well controlled parameters: the relationship between $Gm1$ and $Gm2$ and the K factor (which depend on matching), and the β factor, while remaining independent from the output conductance of the transistors. Furthermore, since the gain can be controlled with the $Gm1$ over $Gm2$ ratio and K, in our implementation, we choosed to set $\beta = 1$, which simplifies the circuit and avoids having resistive loading on the OTAs output, which occurs if a resistive feedback network is applied.

III. Noise Analysis and Circuit Design

This section presents the noise analysis and the transistor design that stems from it.

The input equivalent Power Spectral Density of the noise due to the transistors thermal noise, can be expressed as follows as a function of the $\frac{gm}{ID}$ ratio of each transistor.

$$S_{vin1}^{Total} = \frac{2.\gamma.n.k.T}{gm1_{in}}.[A + \frac{I2}{I1}.B] \tag{12}$$

With:

$$A = 1 + \frac{5}{2}.\frac{(\frac{gm}{ID})_{1n}}{(\frac{gm}{ID})_{1in}} + \frac{3}{2}.\frac{(\frac{gm}{ID})_{1p}}{(\frac{gm}{ID})_{1in}} \tag{13}$$

$$B = \frac{(\frac{gm}{ID})_{2in}}{(\frac{gm}{ID})_{1in}.K^4} + \frac{(\frac{gm}{ID})_{2K}}{(\frac{gm}{ID})_{1in}.K^4} + \tag{14}$$

$$\frac{1}{2.K^2}.(2.\frac{(\frac{gm}{ID})_{21/K}}{(\frac{gm}{ID})_{1in}} + 3.\frac{(\frac{gm}{ID})_{2p}}{(\frac{gm}{ID})_{1in}} + 3.\frac{(\frac{gm}{ID})_{2n}}{(\frac{gm}{ID})_{1in}})$$

For details about the correspondence between the transistors and subindex in these equations see Table II.

In Equation 12, $I1$ and $I2$ are the bias current of the input pair differential transistors of $Gm1$ and $Gm2$ respectively (See Fig.2).

A is the contribution of $Gm1$ to the noise and B is the contributions of $Gm2$. From Equation 12, it is clear that, the lower is I2 the better for the noise contribution. Additionally, in B, the presence of the terms $\frac{1}{K^2}$ and $\frac{1}{K^4}$ shows the effectiveness of the proposed architecture in decreasing the contribution of the $Gm2$ noise.

Second, $(\frac{gm}{ID})_{1in}$ appears in the denominator of A and B so the input pair differential transistors of Gm1 must be in weak inversion in order to maximize this term.

Third, the $\frac{gm}{ID}$ of the rest of the transistors appear in the numerator of A and B so the more in strong inversion they are the better.

The flicker noise component was handled as follows. The area of the transistors of $Gm1$ was increased in order to get a noise corner frequency of 250Hz. In the case of $Gm2$, the proposed architecture decreases the effect of $Gm2$ noise so that its flicker noise was not significant in the equivalent input noise. As an additional benefit of the proposed architecture, the contribution of $Gm2$ to the overall circuit area decreases.

In the Tables I and II we can see the final design values and a comparison with prior work.

	This Work Sim.	**[3]** Sim.	**[4]** Meas.	**[7]** Sim.	
A_0	48	40	40.85	80	dB
f_H	8	7.5	5.32	5.5	kHz
f_L	250	0.13	45	130	Hz
I_{Total}	16.5	16	2.7	180	μA
NEF	4.2	3.8	2.67	53.4	-
v_i^{noise}	2.4	2.1	3.06	7.6	μVrms
$CMRR$	> 107	> 42	> 66	90	dB
@freq	5	0.01 - 5	0.045 - 5.3	1	kHz

Table I
PERFORMANCE

Transistors	**L(μm)**	**W(μm)**	**ID(μA)**	$\frac{gm}{ID}(V^{-1})$	**Subindex**
$M1, M2$	2.6	1200	3.7	24.6	1in
$M3, M7$	84	40	3.7	5.1	1n
$M4, M8$	84	40	3.7	5.1	1n
$M5, M6$	40	55	3.7	4.6	1p
$M9$	1	240	3.5	24	1p
$M9\_1$	1	12	0.2	23.7	-
$M10$	1	180	3.5	26	1n
$M10\_1$	1	9	0.2	25.7	-
$M11, M12$	2	1	0.4	6.6	2in
$M13, M14$	20.9	1	0.4	3	2K
$M15, M16$	65	1	0.04	2.9	2p
$M17, M18$	188	1	0.04	2.8	21/K
$M19$	65	1	0.04	2.9	2p
$M20$	188	1	0.04	3	2n

Table II
TRANSISTORS SIZE, BIAS POINT AND SUBINDEX IN EQUATIONS

IV. SIMULATION RESULTS

Fig.4 shows a two hundred runs Monte Carlo simulation of the differential and common mode gains. In this we can see that we have a very good behavior in terms of the spread of the frequency response, as well as the effectiveness of the proposed local feedback for fixing the low cut-off frequency.

In order to show how the proposed amplifier takes advantage of the DDA architecture (differential input, high CMRR) while minimizing the cost of the additional transconductance ($Gm2$), we show in Table III the relative contribution of this block in terms of area, consumption and noise.

V. CONCLUSIONS

We have proposed a new alternative for neural recording amplifier implementation that improves the CMRR and the method for fixing the low cut-off frequency with power efficiency that is comparable with the best previous results. This is based on a modified DDA architecture and a novel technique, based on a local feedback at the amplifier output, for rejecting the DC component at the output and fixing the low cut-off frequency. The expected performance of the circuit was checked by Monte Carlo simulation in a 0.5μm CMOS technology.

Parameter	**Amplifier**	**Gm2**	**Gm2 (%)**
Area	30432 μm^2	804 μm^2	2.64%
Current	16.5 μA	0.8 μA	4.8%
Noise	2.4 μVrms	0.12 μVrms	5%

Table III
$Gm2$ CONTRIBUTIONS

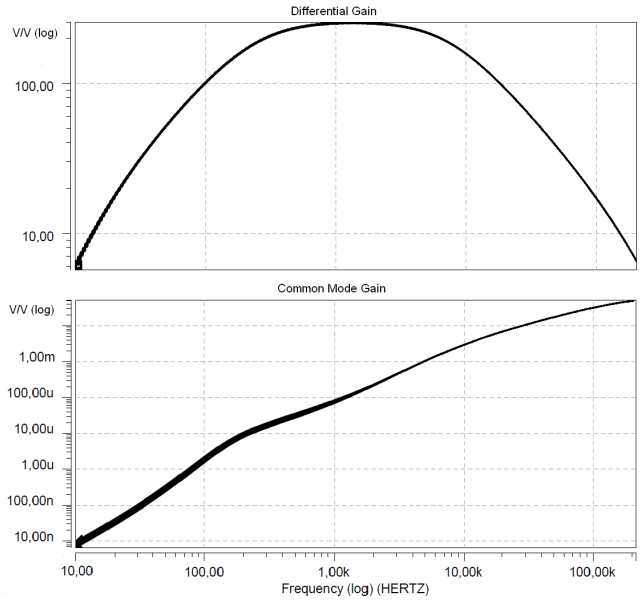

Figure 4. Monte Carlo Simulation of the Differential and the Common Mode Gain

VI. ACKNOWLEDGEMENTS

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