CMOS Op-Amp Power Optimization in All Regions of Inversion Using Geometric Programming

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ABSTRACT

In this paper Geometric Programming is successfully applied to the power optimization of CMOS operational amplifiers using a model valid in all regions of inversion (weak, moderate and strong), which assures a true globally optimal design. A complete transistor model presents some problems on the formulation of the Geometric Program. We will show in this paper that in the case of power optimization, a careful analysis of the physical meaning of the conflicting model equations, allow us to overcome these problems in a simple and efficient way. The proposed algorithm is tested in several cases for a Miller amplifier, showing how the optimum inversion level spans all the inversion regions as the target bandwidth changes.

Categories and Subject Descriptors

B.7.2 [**Hardware**]: Integrated Circuits—*Design Aids*

General Terms

Algorithms, design

Keywords

Analog, Automatic Design, CMOS, Geometric Programming, Optimization

1. INTRODUCTION

Automatic analog circuit synthesis has been the subject of active research since the late 1980s as a mechanism to increase designers productivity [1]. One central idea in this area is to apply optimization techniques to solve the circuit sizing problem while minimizing a cost function (power, area, etc.) under a set of specification constraints.

According to how the circuit performance and constraints are evaluated during optimization, the tools can be broadly classified in *simulation-based* optimization and *equation-based* optimization [1–4].

We will focus here in equation based optimization, where the circuit sizing problem is described through a set of equations that model the behavior of the amplifier and its building blocks (e.g. transistors). This results in a faster method, at the expense of the additional burden of establishing the equations. The result would be as accurate and general as the applied equations are.

Until recently, equation based optimization tools considered only the strong inversion model for the MOS transistor, hence neglecting part of the design space: weak inversion region and particularly the moderate inversion region where the optimum trade-off between power and bandwidth usually lies [5].

Prior art regarding the optimization method applied include general-purpose methods as steepest descent, sequential quadratic programming and Lagrange multiplier methods. The main disadvantage of these methods is that they only find locally optimal designs [2].

There are three main optimization methods that have been used to search for a global optimal design: Branch and bound, simulated annealing and convex optimization. The Branch and bound method is extremely slow with computational effort growing exponentially with problem size. Simulated annealing is also very slow and does not guarantee in practice (only in theory) a globally optimal solution [2].

On the other hand, convex optimization methods can compute a globally optimal solution in a extremely efficient way, reducing optimization time literally to seconds. Also, they can cope with hundreds of variables and thousands of constraints. The disadvantage is that design equations must be formulated in a posynomial form (see Section 2), which is not always the case in analog design. These methods have been used quite recently applied to the problem of CMOS opamp design [2–4].

The first two works [2, 3] used a transistor model valid only in the strong inversion region of operation. Therefore, in spite of using a global optimization method, their algorithms failed to obtain a true optimal design since they didn't include the whole design space available. That is, including the weak inversion region and, specially, the moderate inversion region where optimal designs usually are. This was also observed in the third work [4], where a complete model valid in all regions of inversion was used [6].

Nevertheless, when we use a complete model, there are some problems in the formulation of the equations in a posynomial form. To overcome these problems, [4] incorporates a branch and bound algorithm to its convex optimization method, and thus, looses part of its advantages.

We will show in this paper that in the case of power optimization, a careful analysis of the physical meaning of the design equations that can not be posed in posynomial form, allow us to overcome these problems in a simple and efficient way.

2. GEOMETRIC PROGRAMMING

2.1 Introduction

A Geometric Program (GP) is a type of mathematical optimization problem of the form:

$$\begin{aligned}
\text{minimize} \quad & f_0(x) \\
\text{subject to} \quad & f_i(x) \leq 1, \quad i = 1, \ldots, m \\
& g_j(x) = 1, \quad j = 1, \ldots, p
\end{aligned} \quad (1)$$

where $x \, \epsilon \, \mathbf{R_n^+}$ is a vector of n real positive variables and

$$f_i(x) = \sum_{k=1}^{K} c_k x_1^{a_{1k}} x_2^{a_{2k}} \ldots x_n^{a_{nk}} \quad (2)$$

$$g_j(x) = c x_1^{a_1} x_2^{a_2} \ldots x_n^{a_n} \quad (3)$$

are real valued functions of x where $c_k \geq 0$ are non-negative real numbers and a_{ik} are any real number. $f_i(x)$ is called a *posynomial* function and $g_j(x)$ is called a *monomial* function.

It is well known that geometric programs like (1) can be cast into convex form and thus, a global solution can be found using recently developed interior-point methods. These methods can solve GPs extremely efficiently and reliably, even with hundreds of variables and thousands of constraints. Also, these methods guaranty a global solution or will unambiguously detect that the problem is unfeasible [7].

2.2 Relaxed Problem

When all regions of inversion of the transistor are considered, some design equations are posynomial *equality* constraints (refered to as h_i in the formulation below (4)). However, in a GP, contrary to what happens with *inequality* constraints, posynomials are not allowed in *equality* constraints, only being allowed monomials. A posynomial equality constraints cannot be included in a GP since the equality sign on them implies both a convex and a non-convex constraint. However this can be partially overcome by a simple technique refered to dealing with the *relaxed* problem [7], as explained hereafter.

Consider the following optimization problem, non treatable by GP:

$$\begin{aligned}
\text{minimize} \quad & f_0(x) \\
\text{subject to} \quad & f_i(x) \leq 1, \quad i = 1, \ldots, m \\
& h_i(x) = 1, \quad i = m+1, \ldots, l \\
& g_j(x) = 1, \quad j = 1, \ldots, p
\end{aligned} \quad (4)$$

where f_i and h_i are posynomials and g_j are monomials.

We form the GP *relaxation* of the problem (4):

$$\begin{aligned}
\text{minimize} \quad & f_0(x) \\
\text{subject to} \quad & f_i(x) \leq 1, \quad i = 1, \ldots, m \\
& h_i(x) \leq 1, \quad i = m+1, \ldots, l \\
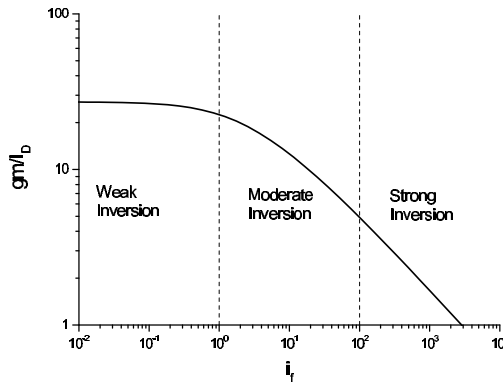& g_j(x) = 1, \quad j = 1, \ldots, p
\end{aligned} \quad (5)$$

Figure 1: (g_m/I_D) **curve (nMOS in** $0.35 \mu m$**).**

by replacing the posynomial equalities with inequalities. This problem is called relaxation since we have increased the set of feasible points. Problem (5) is a GP, and thus can be easily solved. Now, let $\bar{x}$ be the optimal solution of (5). If $h_i(\bar{x}) = 1 \; \forall i$, then $\bar{x}$ is also an optimal solution of the original problem (4). Of course, we might have $k \, \epsilon \, [m+1, l]$ such that $h_k(\bar{x}) < 1$, in which case $\bar{x}$ is not feasible for the original problem. There are ways of dealing with these special cases, however, they sometimes loose some of the advantages of GP [7].

We will see next, that a key equation for analog design in all regions of inversion is the one that links the (g_m/I_D) ratio with the normalized current [5]. However, this equation imposes a posynomial equality constraint on any active transistor in an CMOS analog design. This paper proposes that on power optimization problems, we can work out the problem relaxing the (g_m/I_D) ratio constraint and that the relaxed problem, due to the physical meaning of the (g_m/I_D) ratio will lead to a feasible solution for the original problem.

3. THE (g_m/I_D) RATIO AND POWER OPTIMIZATION USING GP

The (g_m/I_D) ratio is probably the most important characteristic in analog design, since it gives the designer the trade-off between performance and power-consumption [5]. It is present on almost any measure of analog performance: gain, speed, noise, offset, etc. [8]. The larger the (g_m/I_D) ratio, the more power efficient the transistor is. Using a compact MOS model [6], it can be expressed as:

$$\frac{gm}{I_D} = \frac{1}{n\phi_T} \frac{2}{\sqrt{1 + i_f} + 1} \quad (6)$$

where n is the sub-threshold slope factor, ϕ_T is the thermal voltage and i_f is the inversion coefficient, expressed in terms of the normalized current in forward saturation:

$$i_f = \frac{I_D}{\frac{1}{2} n \phi_T^2 \mu C_{ox} \frac{W}{L}} \quad (7)$$

$i_f < 1$ indicates weak inversion operation and $i_f > 100$ indicates strong inversion operation [6]. μC_{ox}, W and L have their usual meanings. Figure 1 shows the (g_m/I_D) ratio of NMOS transistors in a $0.35 \mu m$ technology and the inversion regions.
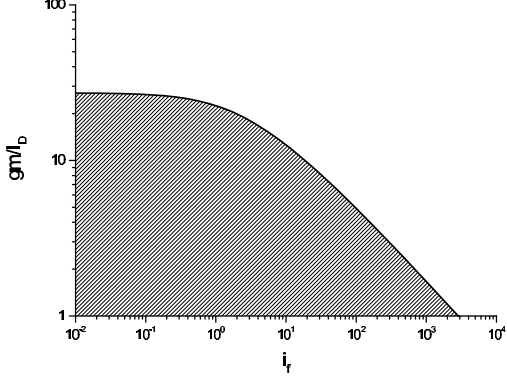
Figure 2: (g_m/I_D) **curve. Shaded area: convex set from constraint** (9).

Equation (6) can be posed as a posynomial of (g_m/I_D) and i_f as:

$$\left(\frac{n\phi_T}{2}\right)^2 (g_m/I_D)^2 i_f + (n\phi_T)(g_m/I_D) = 1 \qquad (8)$$

The problem with expression (8) is that it imposes a posynomial equality constraint for each active transistor on any optimization problem for analog design. Also, it is worth noting that this problem does not depend on the model of the transistor used, but it is intrinsic to the physics of the transistor.

As we commented in Section 1, ways of dealing with this problem have been presented in literature [4] by means of a branch and bound algorithms. However, this algorithm is extremely heavy in the computational effort involved, mainly due to their "blind" nature that ignores the physical meaning of the variables involved.

We propose to analyze the physical meaning of the (g_m/I_D) ratio, in order to provide some insight on the problem and obtain a more efficient algorithm in the particular case of power optimization.

As we said above, the larger the (g_m/I_D) ratio, the more power efficient the transistor is. Therefore, we propose the following idea for power optimization in analog design. If we substitute equality constraint (8) for the following inequality

$$\left(\frac{n\phi_T}{2}\right)^2 (g_m/I_D)^2 i_f + (n\phi_T)(g_m/I_D) \le 1 \qquad (9)$$

we obtain a *relaxed* GP as in Section 2.2. On the optimization side, this relaxation allows us to apply GP to the analog design problem. On the circuit side, this relaxation means that we have artificially increased the set of feasible transistors (shaded area on Figure 2). If the algorithm selects a set of (g_m/I_D) and i_f that doesn't comply with equality (8), it means that it has selected a transistor that doesn't really exist.

Nevertheless, we *know* that, the larger the (g_m/I_D) ratio, the more efficient, in a power consumption sense, our transistor will be. Thus, if we solve the *relaxed* geometric program with only constraint (9) in it, it is reasonable to assume that the optimization problem will always find its solution with the largest (g_m/I_D) ratio posible, since those
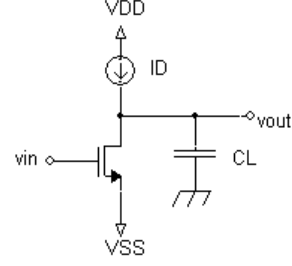

Figure 3: Common-source amplifier circuit.

are the most efficient transistors for a given inversion index i_f. In other words, the optimal solution for the relaxed GP should *also* satisfy the equality constraint (8), and thus, will also be the optimal solution for the original *nonrelaxed* geometric program.

4. PROOF OF CONCEPT: THE INTRINSIC AMPLIFIER

4.1 Design Problem

To test our idea, we will begin with the most simple amplifier: the common-source amplifier (also known as intrinsic amplifier), shown in Figure 3. Although this design problem is quite simple, and certainly we could do without GP to solve it, its simplicity also gives a clear picture on how the idea works.

Therefore, the objective will be to synthesize a common-source amplifier with optimal power consumption that complies with a gain-bandwidth product constraint for a given capacitive load C_L:

$$\omega_T = \frac{gm}{(C_L + C_d)} \ge \omega_{Tmin} \qquad (10)$$

This constraint can be posed as a posynomial of the design variables $I_D, W, L, i_f, (g_m/I_D)$:

$$\frac{(C_L + C_{pd})\omega_{Tmin}}{(g_m/I_D)I_D} + \frac{C_{wd}W\omega_{Tmin}}{(g_m/I_D)I_D} \le 1 \qquad (11)$$

where the bias dependent extrinsic drain capacitance is taken in its worst case (zero bias) as $C_d = C_{wd}W + C_{pd}$ (the intrinsic drain capacitance of the forward saturated transistor is neglected).

Also, we must include the constraint that links current, size and inversion level on any transistor,

$$\frac{I_D}{\frac{1}{2}n\phi_T^2 \mu C_{ox}\frac{W}{L}i_f} = 1 \qquad (12)$$

and equation (8), the posynomial equality constraint that links (g_m/I_D) and i_f, which we will substitute by the inequality constraint (9) to form the relaxed GP.

Finally, we must also impose the technology bounds for the transistor size: $W_{min}/W \le 1$ and $L_{min}/L \le 1$.

These are just an example of the basic constraints that can be included in the design of a common-source amplifier. Many others could also be included to take into consideration other performance parameters (i.e. gain, noise, output swing, etc.). Nevertheless, to clarify the proposed idea, we will not include any of them at this time.
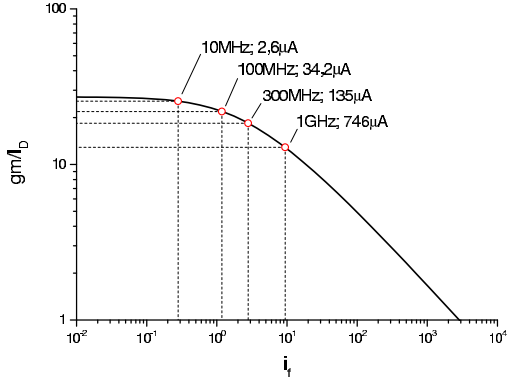
Figure 4: Synthesis of four common-source amplifiers ($0.35\mu m$, **1pF load**). **Text labels show the gain-bandwidth product and current consumption of each amplifier.**

4.2 Results

We used the relaxed GP from previous section to synthesize four common source amplifiers in a $0.35\mu m$ CMOS technology loaded by $1pF$. Figure 4 shows the result of the synthesis in a (g_m/I_D) - i_f plot. Text labels show the gain-bandwidth product and the obtained current consumption in each amplifier. GP assures that these solutions are the *global optimal solutions* to the *relaxed* design problem. Also, as we can see, all of them comply with the original posynomial *equality* constraint (8), although only the posynomial *inequality* constraint (9) was used in the synthesis. Therefore these solutions are also the *global optimal solutions* to the *original non-relaxed* design problem, as explained in section 3.

These examples are no coincidence nor particular cases. The fact that the optimal solution to the design problem will comply with equality constraint (8) can be demonstrated as follows:

Hypothesis: Let **A** be the optimal solution to the relaxed design problem described in Section 4.1.

Thesis: **A** must be valid in the original, *non-relaxed*, design problem (i.e. complies with equality constraint (8)).

Proof: By absurd let's assume that **A**, the optimal solution to the relaxed design problem, is not valid in the original problem.

Then, we will build **B**, a solution to the relaxed problem, such that is valid in the original, *non-relaxed*, design problem. We will build it in the following way: We will take the same transistor ($W_B = W_A$, $L_B = L_A$) and the same gain-bandwidth product ($\omega_{TB} = \omega_{TA}$) from solution **A**. Therefore solution **B** complies with all constraints. From eq. (11) we can write ω_T as:

$$\omega_T = \frac{(g_m/I_D)I_D}{C_L + C_{pd} + C_{wd}W} \qquad (13)$$

Both solutions share the same denominator since it only depends on load capacitance, technology parameters and width of the transistor. Therefore we can write the following relation between (g_m/I_D) ratio and drain current of each solu-

tion:

$$(g_m/I_D)_A I_{DA} = (g_m/I_D)_B I_{DB} \qquad (14)$$

Since solution **B** complies with equality constraint (8), we can substitute $(g_m/I_D)_B$ by the expression given in eq. (6):

$$(g_m/I_D)_A I_{DA} = \frac{2}{n\phi_T} \frac{I_{DB}}{\sqrt{1 + \frac{I_{DB}}{I_S}} + 1} \qquad (15)$$

where I_S is the normalization current (see eq. (7)) which is constant since we built our transistors with the same size. Since solution **A** doesn't comply with the equality constraint (8) we can write $(g_m/I_D)_A$ as:

$$(g_m/I_D)_A = k\frac{2}{n\phi_T} \frac{1}{\sqrt{1 + \frac{I_{DA}}{I_S}} + 1} \qquad (16)$$

where k is such that $0 < k < 1$. Using (16) in (15) and doing some algebra we can express I_{DB} as

$$I_{DB} = kI_{DA} \left[1 - \frac{(1-k)\frac{I_{DA}}{I_S}}{\left(\sqrt{1 + \frac{I_{DA}}{I_S}} + 1\right)^2} \right] \qquad (17)$$

It can be shown that the term between square brackets is between 0 and 1, and since k is also less than 1, we have found a solution **B** to both problems (the *non-relaxed* and the *relaxed* problems) such that

$$I_{DB} < I_{DA} \qquad (18)$$

which is absurd since **A** is the optimal solution to the relaxed design problem. Therefore, solution **A**, must be valid in the original, *non-relaxed*, design problem. ∎

This demonstration is based on the fact that the gain-bandwidth constraint is active (e.g. the solution has a gain-bandwidth equal to the minimum imposed by the inequality constraint). However, should exist another constraint that causes the gain-bandwidth constraint to be *in-active*, the solution might fail to be valid in the original, *non-relaxed*, problem. For example, if we add a slew-rate (SR) constraint that implies $\omega_T > \omega_{Tmin}$, then the solution would not be valid in the original problem.

Nevertheless, this "failure" of the optimization method can be noticed immediately and thus, there is no risk of taking for good the "false" transistor's design. As mentioned above there are ways of dealing with this, for instance, to adjust the ω_T constraint in order to turn it active. Also, the literature on GP proposes more elaborate methods, such as "Tightening" [7], to obtain a valid solution on the original problem from the relaxed solution. However, this methods sometimes loose some of the advantages of GP.

Therefore the method proposed in this paper is able to deal with a significant portion of power optimization problems where bandwidth is a limiting factor.

5. DESIGN EXAMPLE: THE MILLER AMPLIFIER

The Miller amplifier is one of the most common analog building blocks and has been thoroughly analyzed in the literature (e.g. [9]). In Figure 5 we show the circuit implementation of the Miller amplifier. It is well known that this amplifier has a right-half-plane zero (due to Cm), a low-frequency dominant pole and a high frequency pole due to
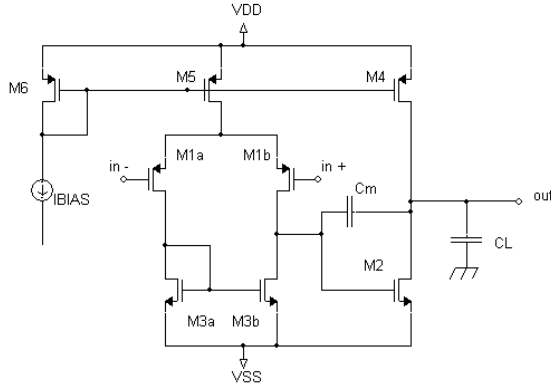
Figure 5: Miller amplifier circuit.

(a)

(b)

Figure 6: Synthesis of five Miller amplifiers. (g_m/I_D) - i_f plot for (a) Differential pair M1a-M1b transistors and (b) Output M2 transistor. Text labels show the gain-bandwidth product, load capacitance and total current consumption of each amplifier.

the output node. Also, the pole-zero doublet from the input stage current mirror (M3a-M3b) must be taken into account to avoid a degraded transient response [10].
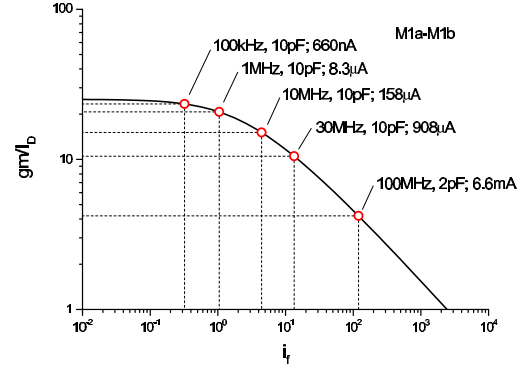
We built a GP to synthesize a Miller amplifier with optimal power consumption for a given gain-bandwidth product and phase margin. Constraints on minimum dc gain, output swing and maximum area were also included. Hershenson *et al.* [2], deeply analyze these and some other Miller amplifier's design equations and ways to pose them in posynomial/monomial form in order to include them as constraints in the optimization problem. In our case, though, we used expressions for the intrinsic capacitances valid in all regions of operation [6].

In order to take into consideration all regions of operation of the transistor, we included for each transistor a constraint that links current, size and inversion level such as (12). Also we included the constraint that links (g_m/I_D) and i_f for each *active* transistor. The gm of other transistors does not affect the circuit characteristics, hence consideration of their (g_m/I_D) ratio is not required. In the Miller amplifier, the only active transistors are M1a-M1b, M3a-M3b and M2. In order to minimize systematic offset we used $(g_m/I_D)_3 = (g_m/I_D)_2$ (which implies $V_{GB2} = V_{GB3}$), and therefore we only had to include two (g_m/I_D) ratio constraints (one for transistors M1a-M1b and the other for transistors M2 and M3a-M3b). Both constraints were relaxed and we will see that the solution to the relaxed GP complies with the (g_m/I_D) ratio equality constraints, i.e. the solution found provides the global optimum of the original, non-relaxed, design problem.
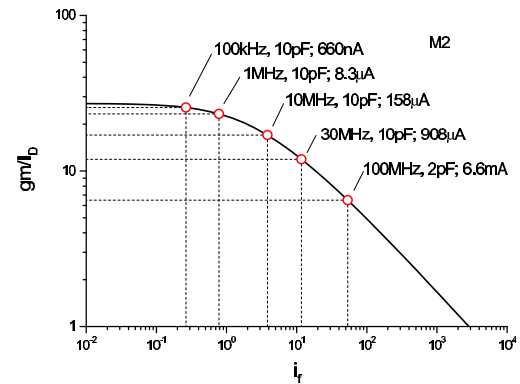
6. RESULTS

The GP from previous section was used to synthesize five Miller Amplifiers with different gain-bandwidth product specifications. Figure 6 shows the (g_m/I_D) - i_f plots for the two active transistors (M1a-M1b and M2). In all cases the solution for both transistors comply with the original non-relaxed problem, as we predicted. Table 1 shows the detailed results for the particular case of the $1MHz$ amplifier.

It is interesting to note that all optimal solutions lie on the moderate inversion region of operation for both active transistors. Only the slowest and fastest designs lie on the near-weak inversion and near-strong inversion regions re-

	Specs.		Result	
f_T	$\geq 1MHz$		$1MHz$	
PM	$\geq 65^o$		66°	
$(g_m/I_D)_1$	$2 \leq (g_m/I_D)_1 \leq 27$		20.7	
$(g_m/I_D)_2$	$2 \leq (g_m/I_D)_2 \leq 25$		23.3	
$V_{DSsat2,4}$	$\leq 300mV$		$130mV, 300mV$	
Cm	$\geq 0.1pF$		$0.45pF$	
IDD	minimize		$8.3\mu A$	
ID1	-		$0.15\mu A$	
ID2	-		$8.0\mu A$	
	W (μm)	**L** (μm)	**W** (μm)	**L** (μm)
M1	≥ 0.4	≥ 0.35	2.5	0.35
M2	≥ 0.4	≥ 0.35	57.7	0.35
M3	≥ 0.4	≥ 1	2.9	1
M4	≥ 0.4	≥ 2	26x0.4	2
M5	≥ 0.4	≥ 2	0.4	2

Table 1: Detailed results for the optimized 1MHz Miller amplifier.

spectively. This is not unexpected and shows the need of a model valid in all regions of inversion for analog design. Also, this is particularly important when using optimization tools as in our case. If a model not valid in all regions of inversion is used, as in the case of reference [2], a suboptimal solution will be found in spite of using a global optimization method.

7. CONCLUSION

Geometric programming was successfully applied to the power optimization of CMOS operational amplifiers, using a model valid in all regions of inversion, which assures a true globally optimal design.

The (g_m/I_D) ratio is a key parameter in analog design. However, when using it in a GP, it imposes a posynomial equality constraint for each active transistor, which is not acceptable. Previous solutions to this problem used more complex mathematical tools, such as branch and bound algorithms [4], which are extremely slow and the computational effort involved grows exponentially with problem size.

We showed how when we analyzed the physical meaning of the (g_m/I_D) ratio, we founded a much simpler solution. The *relaxed* GP enlarges the set of feasible points of the problem in order to transform the posynomial equality constraints in posynomial *inequality* constraints. Our analysis of the (g_m/I_D) ratio allowed us to foresee that usually the solution would be in the original set of feasible points, i.e. would comply with the posynomial equality constraint. This was explained and demonstrated by means of a simple example: the common-source amplifier. Then we showed how to apply the idea to a more "classical" example: the Miller amplifier. In all cases, the solution from the *relaxed* GP was a feasible solution of the original GP.

In both examples, most solutions lied on the moderate inversion region. This is particularly important since it showed the need of a model valid in all regions of inversion in order to avoid suboptimal solutions, even when using global optimization methods.

It is worth noting that not every performance constraint in any possible opamp architecture can be posed as a valid GP constraint (e.g. settling time constraint with a second order model, as shown in [4]). However, there is one constraint that can not be posed as a valid GP constraint which is always unavoidably present in CMOS analog design problems: the relation between the (g_m/I_D) ratio and the bias current of the transistor. In this paper we presented a simple and efficient way to overcome this problem for power optimization.

Acknowledgment

8. REFERENCES

[1] G. Gielen and R. Rutenbar, "Computer-aided design of analog and mixed-signal integrated circuits," *Proc. IEEE*, vol. 88, no. 12, pp. 1825–1854, Dec. 2000.

[2] M. Hershenson, S. Boyd, and T. Lee, "Optimal design of a cmos op-amp via geometric programming," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 20, no. 1, pp. 1–21, Jan. 2001.

[3] P. Mandal and V. Visvanathan, "Cmos op-amp sizing using a geometric programming formulation," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 20, no. 1, pp. 22–38, Jan. 2001.

[4] J. Vanderhaegen and R. Brodersen, "Automated design of operational transconductance amplifiers using reversed geometric programming," in *Proceedings on 41st Design Automation Conference*, vol. I, Jun. 2004, pp. 133–138.

[5] F. Silveira, D. Flandre, and P. G. Jespers, "A (g_m/I_D) based methodology for the design of cmos analog circuits and its application to the synthesis of a silicon-on-insulator micropower OTA," *IEEE J. Solid-State Circuits*, vol. 31, no. 9, pp. 1314–1319, Sep. 1996.

[6] A. Cunha, M. Schneider, and C. Galup-Montoro, "An MOS transisotr model for analog circuit design," *IEEE J. Solid-State Circuits*, vol. 33, no. 10, pp. 1510–1519, Oct. 1998.

[7] S. Boyd, S. J. Kim, L. Vandenberghe, and A. Hassibi, "A tutorial on geometric programming," Stanford University and University of California Los Angeles, Tech. Rep., 2005. [Online]. Available: http://www.stanford.edu/~boyd/gptutorial.html

[8] F. Silveira and D. Flandre, *Low Power Analog CMOS for Cardiac Pacemakers Design and Optimization in Bulk and SOI Technologies*, ser. The Kluwer International Series In Engineering And Computer Science. Boston: Kluwer Academic Publishers, Jan. 2004, vol. 758, ISBN 1-4020-7719-X.

[9] W. M. Sansen and K. R. Laker, *Design of Analog Integrated Circuits and Systems*. McGraw-Hill, 1994, ISBN 0-07-036060-X.

[10] B. Kamath, R. Meyer, and P. Gray, "Relationship between frequency response and settling time of operational amplifiers," *IEEE J. Solid-State Circuits*, vol. 9, no. 6, pp. 332–340, Dec. 1974.