A TOOL FOR DESIGN EXPLORATION AND POWER OPTIMIZATION OF CMOS RF CIRCUITS BLOCKS

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ABSTRACT - A tool that explores the design space of basic RF circuit blocks is presented. The tool takes advantage of the application of an MOS transistor model continuous in all inversion levels (weak to strong inversion). The performance of the circuit is analyzed in the I_D-g_m/I_D plane. The tool shows the existence of a inversion level that provides an optimum in the power consumption for a given gain and frequency. Examples are presented showing how comparison of the performance of different technologies or evaluation of the effect of parasitic elements can be easily done. The tool is applied to the design of a power amplifier and a VCO at 910 MHz in 0.35µm CMOS technology. The tools estimations are checked against simulations using BSIM3v3, showing very good agreement. Additionally, preliminary experimental results are presented.

I. INTRODUCTION

Nowadays, the development of low-cost, low-power radiofrequency (RF) devices grows up rapidly, and those systems are characterized by short range links (usually below 100m) and reduced power consumption (since the devices are powered with batteries).It is known that optimum power consumption of analog circuits can be reached in the moderate inversion region [1], where is obtained a good trade-off between a high g_m/I_D and a not too large transistor size and hence reduced parasitic capacitances values. Traditionally the operation at this optimum was restricted to low frequency applications, since the transconductance values required for operation at RF implied currents that, in order to operate in moderate inversion, lead to enormous transistor sizes. However, the scaling of devices changes this scenario as it is shown in this work. This idea, the possibility of exploiting operation in weak and moderate inversion for RF in scaled technologies, has also been advanced in [2,3,4].

However, as far as we know, there is no published work where a tool for analyzing the trade-offs and possible optimum solution has been presented. In this work this improvement is applied to design power amplifiers and voltage controlled oscillators (VCO). It will be presented a software tool which can be used either to design amplifiers, obtaining an optimum design and showing the trade off between amplifier's gain and power consumption, or to evaluate the performance of a particular technology at a desired frequency. With this tool it has been checked the good performance of a 0.35µm technology at 910MHz and it has been designed a VCO and a power amplifier of 40V/V gain and 5.5mA current consumption.

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II. MODEL AND ALGORITHM

A. Modeling approach

Firstly, the approach applied for modeling the MOS transistor in small signal operation and the amplifier building blocks is presented. A physical, compact MOS transistor model, continuous from weak to strong inversion (ACM [5]) was selected. As discussed later, a five intrinsic capacitances, quasi-static model was deemed sufficient for analyzing the circuits in the desired regions and frequencies.

The basic amplifier structures considered are modeled by quadripoles, as it is shown in Fig.1, in order to represent different configurations and loads.

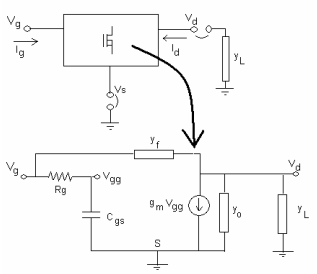

Figure 1: Transistor modeled as a quadripole and basic internal small signal model

The two port relations of the quadripole in Fig.1 can be written as:

$$\begin{aligned} i_d &= y_{dd} v_{ds} + y_{dg} v_{gs} \\ i_g &= y_{gd} v_{ds} + y_{gg} v_{gs} \end{aligned} \quad (1)$$

Assuming that the MOS transistor operates in saturation and in the quasi-static regime, the transadmittances shown in Eq.2 are automatically computed.

This transadmittances include intrinsic capacitances (C_{db}, C_{gs}, C_{gb}, C_{sb}, C_{dg}) and extrinsic capacitances (overlap and junction capacitances). Assuming the transistor in saturation, C_{db} and C_{dg} are equal to zero. The gain of the stage A is given by:

$$A = \frac{v_{ds}}{v_{gs}} = \frac{- y_{dg}}{y_{dd} + y_L} \quad (2)$$

The model that has been presented is a quasi-static model (QS). However, the limitation of the QS model is known at high frequency where the non-quasi-static (NQS) effects have influence. That is why it is important to have an estimation of the frequency which limits the zones of QS and NQS operation. This limit has been fixed at $0.1 \cdot f_T$ (where f_T is the unitary gain frequency of the transistor) as it is proposed in [6][7]:

$$f_{QS\max} \approx \frac{f_T}{10} = \frac{0.1\,g_m}{2\pi\left(C_{gs}+C_{gb}+C_{gd}\right)} \qquad (3)$$

Working below this limit also assures that is not necessary to use the complete model of the nine intrinsic capacitances and transcapacitances of the device [6].

Another effect that can limit the performance of the transistor MOS at high frequency is the carrier velocity saturation; an effect that is noticeable in very strong inversion. But, as in this work it is shown that it is possible and convenient to work in moderate inversion, in the following this effect is not considered. In case of working in very strong inversion (g_m/I_D less than 3…4 1/V), velocity saturation can modify the results shown.

B. Design Space Exploration Algorithm

The proposed algorithm for designing RF amplifier blocks considers the design space defined by the DC bias current I_D of the active transistor and its g_m/I_D ratio; parameters that define the transistor aspect ratio (W/L) [1]. The transistor length is always the minimum allowed by the technology in order to maximize the high frequency performance by decreasing parasitic capacitances. In this design space the current consumption was considered for a given voltage gain at a given frequency.

The algorithm is summarized as follows: the design space is covered by a grid of couples (I_D, g_m/I_D). For each of these couples the gain A =A (I_D, g_m/I_D), width W =W (I_D, g_m/I_D) and quasi-static boundary B = B(I_D, g_m/I_D) are obtained.

Having explored this design space, as it is shown in the example of the following section, for a given gain, there is a g_m/I_D value that results in an optimum of consumption. This optimum lies in moderate inversion for usual gain values.

This algorithm adds the evaluation of the harmonic distortion of the stage, so that the design space can be limited to those areas that comply with a given distortion target.

III. RESULTS AND DISCUSSIONS

In this example, a one-stage amplifier with load capacitance C_L and a feedback resistance R_F is presented, as it is shown in Fig.2.

The a priori design values are: C_L=0.5pF, R_F =5kΩ, f_0 = 910MHz W_{MP} =20µm, , $L_{MP,M1}$=0.35µm. In the first part of the example the gate resistance R_g is neglected. Later, it is studied the degradation of the previous results if the R_g corresponding to a non-interdigitized layout is considered.

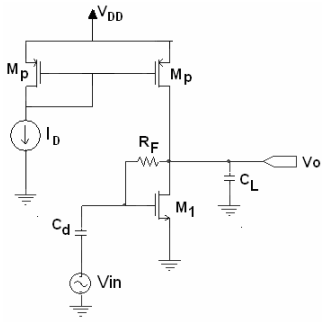

Figure 2: Example circuit.

Neglecting R_g and considering that the desired gain is 2V/V, the algorithm generates the gain curve of Fig.3 (circle markers), where the optimum is marked with an arrow. It is also shown the curve of optima (points of minimum consumption for a given gain, square markers); thus if it is desired to work optimally for a chosen gain, the current I_D and the g_m/I_D ratio (and therefore the transistor width) are fixed.

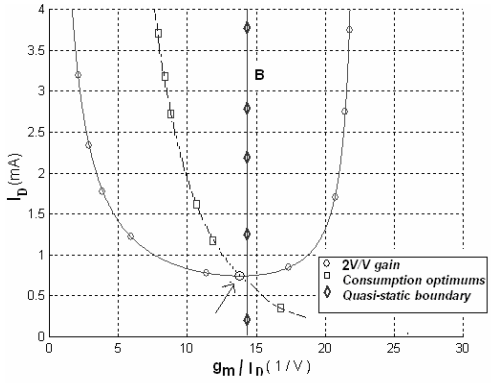

Figure 3: Result of example. Marked with circular markers is the 2V/V gain curve, with square markers is the optima of consumption and with rhomboid markers (B curve) is the quasi-static boundary @ 910MHz.

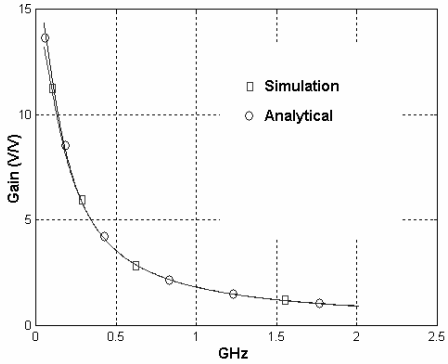

Figure 4: Frequency response calculated and simulated, neglecting Rg.

Fig.3 also shows the quasi static boundary limit B for this technology (rhomboid markers), where, given a working frequency f_0, the maximum g_m/I_D is fixed independent of I_D. In the optimal point the width of M_1 is 223µm, I_D is 0.75mA, and g_m/I_D is almost 14. The algorithm results have been contrasted with simulation results using BSIM3v3, and, as it is shown in Fig.4, a good correlation has been found.

To show the potential of the proposed tool is terms of evaluating design trade-offs, it is studied how the gate resistance degrades the performance of the amplifier designed previously, if proper care is not taken at the layout.

The algorithm adds R_{geff}=R_g/3, considering a non interdigitized layout for the transistor M_1[6], with a resistance per square of the gate material of 8.6k Ω/sq. From Fig.5 it is clear than the new optimum occurs at a higher current consumption that the previous one (marked by an arrow in the figure). Despite the gate resistance effect is extensively known, it is interesting to see the effect on the consumption at a given gain.

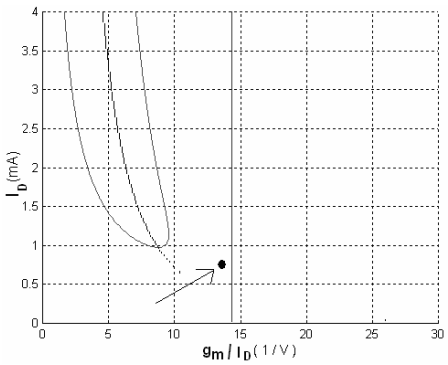

Figure 5: Gain curve of 2V/V of example when the effect of R_g of a non interdigitized layout is considered. The point marked by the arrow shows the location of the minimum consumption point determined in Fig. 3 for a negligible R_g.

Figure 6 shows the tool user interface which is a fully interactive plot. The designer can move a cursor on the I_D-g_m/I_D plane and each time the designer selects a point, several characteristics such as bias point, level of inversion, gain, power gain, HD_2, IM_3 and other circuit parameters are automatically computed as a function of the selected I_D-g_m/I_D couple and shown in the left part of the screen.

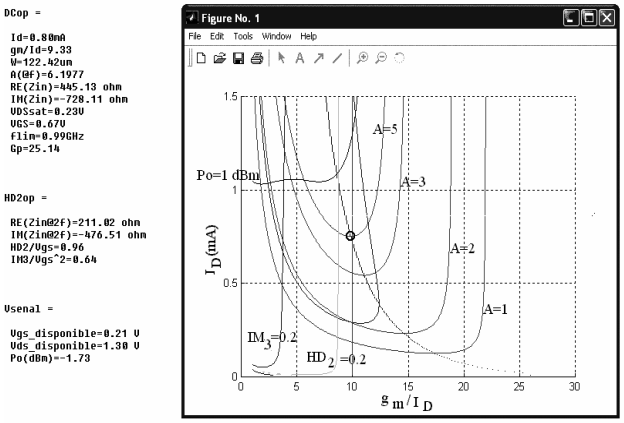

Figure 6: Tool user interface

IV. IMPLEMENTATION

Using the described methodology, the amplifier shown in Fig.7 has been designed. The final design parameters are:

Table I: Data of the designed amplifier.

	M_1	M_2	M_3	M_P
W (µm)	60	60	80	200
I_D (mA)	0.5	0.5	1.5	2.54

Current mirrors: Me_0, Me_1, Me_2: W=20µm Me_3: W=60µm

Feedback DC bias: R1=R2=15 kΩ , C2=1pF

Power given to the load R_L: 2dBm

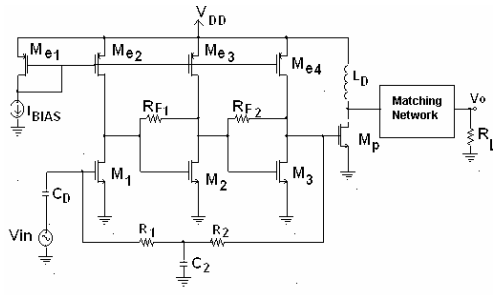

Figure 7: Amplifier implemented in 0.35µm technology with 40V/V gain at 910MHz.

V. MEASUREMENT RESULTS

A chip including this amplifier was fabricated. Unfortunately, a layout error was introduced during the final adjustments in the overall chip layout. This error made that the DC feedback, that sets the overall amplifier bias point, was non functional. Anyhow, in order to test the amplifier, the bias was set in open loop, which made it much more inaccurate and unstable.

Nevertheless, by testing several bias points and performing extensive simulations, it has been possible to select a bias point where it was possible to measure the performance of the circuit. In Table II are shown the results of the measurements, when V_{DD} is 2.3V, V_{bias} is 0.83V and I_D is 0.5mA

Table II: Measured and simulated characteristics.

Characteristics	Measured	Simulation
I_{DD}(at 0 power delivered)	3.21 mA	3.22mA
P_{out} (*)	-8.9 dBm	-5.7 dBm
Harmonic Distortion:HD_2	-26.5 dB	-22.0 dB
Voltage gain	8.9 V/V	12.7 V/V

(*) P_{in} = -16.4 dBm (V_{in} =13.1mV) @ 910MHz, R_L=50Ω through a matching network.

These results confirm the operation of the preamplifier stages (M_1, M_2 and M_3 in Fig. 6) at 910MHz while biased in moderate inversion as calculated. New designs have been fabricated and will be tested soon.

VI. DESIGN OF A –G_M LC CROSS-COUPLED VCO IN 0.35µM CMOS TECHNOLOGY

In this section the methodology and design of a 910MHz cross-coupled -G_m LC VCO [8] in 0.35µm CMOS standard technology with on-chip inductors [9] is presented (see Fig.8) Also it is shown how the tool previously presented is used to validate the use of a quasi-static model to design this VCO.

Being G_m the equivalent transconductance of the nMOS cross-coupled transisor block (with $G_m \cong g_{m,i}$, $g_{m,i}$ the transconductances of transistors M_i i=1,2), g_{tank} the equivalent tank conductance (assumed to be approximately $2 \cdot g_{inductor}$) and α the oscillation factor (a design criterion usually equal to 3), then the VCO oscillation condition is $Gm=\alpha \cdot g_{tank}$. If g_m/I_D of M_i is increased while α and the inductance electrical characteristics are known, then $g_{m,MOS}$ is fixed and I_D decreases (with

$I_D=I_{bias}/2$). However, the minimum possible value of I_D is limited by the maximum oscillator phase noise value specified [10][11], as it increases when I_D drops. It is also limited by the parasitic capacitances of M_i, i=1,2, since an increment in g_m/I_D produces an increment in the transistor's width. The last also restricts the oscillation frequency and diminish the tuning range.

Considering the previous discussion, the VCO design methodology proposed is presented in the scheme of Fig.9. Given an inductor value L and a oscillation frequency f_0, the inductor dimensions and its parameters are calculated ($g_{inductor}$ and quality factor among others). With them, g_m/I_D and α, it is found I_D. Using the transistor's characteristic curves (g_m/I_D vs. $I_D/(W/L)$), the width W of M_i and the varactor capacitance C_{var} are obtained.

In this work the emphasis has been laid on decreasing power consumption without a great detriment on phase noise. The transistors were dimensioned to work in moderate inversion ($g_m/I_D \cong 11$, W=450µm) with a bias current of 2.8mA and the power consumption is 8.4mW and a phase noise of -107dBc/Hz $_{@600kHz}$. In this design it has been assumed the quasi-static operation of the circuit because the quasi-static boundary of this transistor at 910MHz has been checked with the tool previously described (the boundary is around $g_m/I_D=14$).

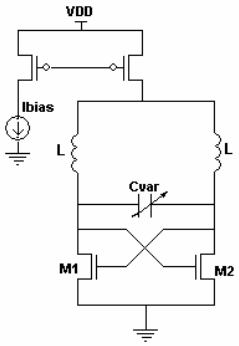

Figure 8: Cross-coupled –Gm LC VCO.

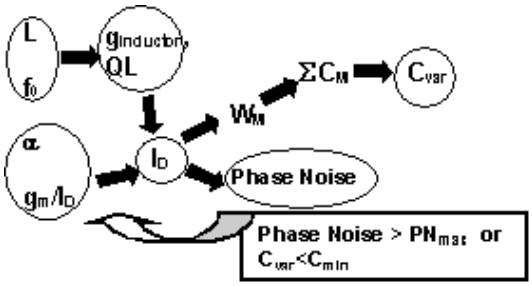

Figure 9: Proposed VCO design methodology considering the phase noise and power consumption specifications.

VII-CONCLUSION

In this work it has been presented a flexible tool to help in the design of low power RF blocks. It has also been shown the existence of an optimum inversion level which gives the minimum power consumption for a given gain, or equivalently, the maximum gain for a given consumption. This optimum inversion level appears in different types of amplifiers and in varied technologies. Finally it has been shown the feasibility of working, with 0.35µm technologies at 910MHz, in moderate inversion, which gives a better compromise between speed and consumption.

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