

Adaptive Output Current Feedforward Control in VR Applications

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Abstract—A method for adapting the gain of an output current feedforward path in VR applications is presented. For regulators using *adaptive voltage positioning* (AVP), output current feedforward can improve the dynamic response to fast load transients. However, the feedforward path depends on parameters of the power train that are not known with precision. By analyzing the error voltage and finding its correlation with the parameter error, a gradient algorithm is derived that makes the parameter error vanish and minimizes the voltage error.

I. INTRODUCTION

In voltage regulation (VR) applications for modern microprocessors, *adaptive voltage positioning* (AVP) was adopted as an effective way of reducing the output capacitance [1]. Instead of regulating to a fixed voltage, independent of the output current, AVP mandates that the regulator should have a small resistive output impedance. This means that the output voltage has to track the variations in the output current. The specification is valid both for static (DC) operation as well as transients (AC).

In control systems terminology, AVP imposes a tracking problem in which the reference signal becomes $V_r - R_{LL}I_o$, where V_r is the nominal reference voltage, R_{LL} is the reference output resistance (load-line), and I_o is the output current. Since the high-frequency output impedance of the buck converter is always equal to the ESR of the output capacitors, traditional designs select the ESR equal to R_{LL} . Some design considerations for this control strategy were presented in [2], [3]

This approach works well for electrolytic capacitors. However, this is not feasible for ceramic capacitors, which have a much lower ESR. For this reason, the concept of generalized load-line was introduced [4]. The generalized load-line acknowledges the physical limitations of the system, creating a dynamic output impedance reference Z_{ref} that is equal to R_{LL} at low frequencies, and the ESR of the output capacitor at high frequencies.

In tracking control problems it is usually convenient to include a feedforward path from the reference signal to the input of the plant, in order to improve the dynamic performance without pushing the bandwidth of the feedback loop too high. This approach is particularly useful in VR applications, in

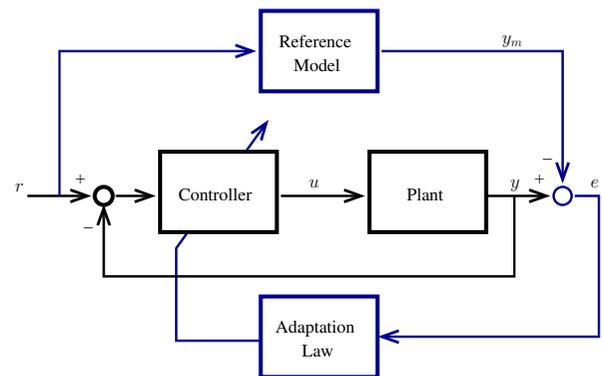


Fig. 1. Traditional *model reference adaptive control* (MRAC).

which the output current has large and fast transients that need to be tracked, while the bandwidth of the feedback loop is limited by the switching frequency of the converter through a stability constraint [4]. Output current feedforward had been reported earlier as a way of improving the output impedance of a DC-DC converter [5], [6].

The feedforward path is effective as long as its parameters correspond to the actual values of the plant. Unfortunately, the value of many components in the power train of a VRM converter have a wide uncertainty. For this reason, in this paper, an adaptive mechanism is presented in order to tune the feedforward path with the objective of minimizing the voltage error.

A traditional *model reference adaptive control* (MRAC) scheme is shown in Fig. 1 [7]. The desired behavior of the system is specified with a Reference Model. The difference e between the output y_m of the model and the output y of the Plant is used to tune the parameters of the Controller according to some Adaptation Law. This law is defined such that the behavior of the closed-loop system converges to that of the reference model. In the figure, a typical MRAC scheme for a feedback controller is shown.

In the case of a VRM application with AVP, since the objective is regulation of the output voltage, the output of the reference model is simply the reference voltage v_r minus the reference impedance times the output current i_o . Therefore,

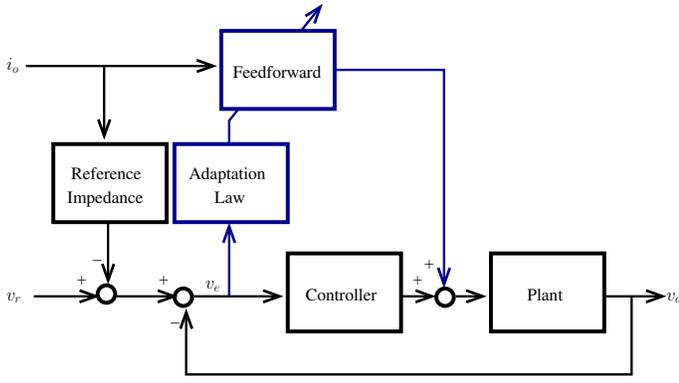


Fig. 2. MRAC in a VRM application.

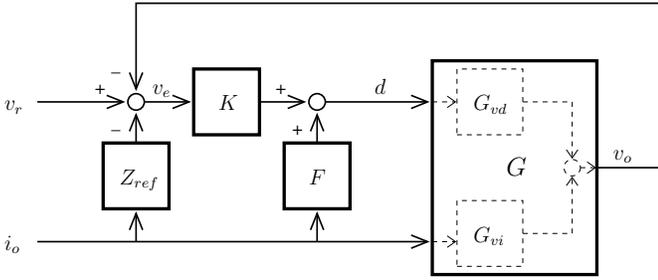


Fig. 3. DC/DC converter model using voltage mode control and output current feedforward.

the error signal to be observed for adaptation purposes is the same error signal v_e that is sent to the input of the feedback controller. This is illustrated in Fig. 2. In the adaptive control scheme developed in this paper, a gradient algorithm is used as an adaptation law to tune the parameters of the feedforward path.

II. FEEDFORWARD GAIN ADAPTATION

A. Ideal feedforward

The ideal feedforward transfer function can be computed from the block diagram shown in Fig. 3. Block G is the small-signal model of a buck converter, with two inputs corresponding to the duty cycle command d and the output current i_o , and one output corresponding to the output voltage v_o . This two-input-one-output block can be represented by two transfer functions, $G = [G_{vd} \ G_{vi}]^T$ such that

$$v_o = G_{vd} \cdot d + G_{vi} \cdot i_o. \quad (1)$$

The feedback controller is represented by block K and the output current feedforward by block F . Adaptive Voltage Positioning is achieved by subtracting the reference impedance Z_{ref} times the output current from the reference voltage v_r .

The closed-loop transfer function from the output current i_o to the output voltage v_o (i.e., the output impedance) in this system is equal to

$$Z_o^{CL} = T_{i_o \rightarrow v_o} = \frac{-G_{vd}KZ_{ref} + G_{vd}F + G_{vi}}{1 + G_{vd}K} \quad (2)$$

By equating the closed-loop output impedance to the desired output impedance $-Z_{ref}$, the ideal value of F can be found to be

$$F = -\frac{Z_{ref} + G_{vi}}{G_{vd}}. \quad (3)$$

This expression was reported in [4] for voltage mode control and including the circuit parameters is approximately equal to

$$F \approx \frac{Ls}{V_{in}(R_{LL}Cs + 1)}. \quad (4)$$

It can be seen that the feedforward path consists of a derivative term with a high-frequency pole. The most critical parameter is the gain or multiplying factor of the derivative term. This is the single parameter that is to be adjusted with the adaptation scheme outlined below.

B. Adaptation algorithm

In order to derive the adaptation law, a gain stage is added to the feedforward path noted as parameter θ , that ideally would be unity. Since the actual values of the parameters in the circuit (most notably the inductance L) may be different from the values used to compute F , the parameter θ will be allowed to change in order to compensate this difference. Then, the feedforward path will be

$$\hat{F} = -\theta \cdot \frac{Z_{ref} + G_{vi}}{G_{vd}}. \quad (5)$$

From Fig. 3, the error voltage v_e can be computed, with \hat{F} replacing F , as

$$v_e = \frac{Z_{ref} + G_{vi}}{1 + G_{vd}K} (\theta - 1) \cdot i_o. \quad (6)$$

Define the parameter error $\phi = \theta - 1$ and a new signal

$$h = \frac{Z_{ref} + G_{vi}}{1 + G_{vd}K} \cdot i_o, \quad (7)$$

then

$$v_e = h \cdot \phi. \quad (8)$$

A gradient algorithm [7] is implemented by defining the following estimation law:

$$\dot{\theta} = -g \cdot h \cdot v_e, \quad (9)$$

where $g > 0$ is a “small” value that will define the bandwidth of the adaptation algorithm.

It is simple to prove the convergence of this algorithm. Substituting (8) into (9) yields

$$\dot{\phi} = \dot{\theta} = -g \cdot h^2 \cdot \phi. \quad (10)$$

This equation shows that the adaptation algorithm will always change the value of the parameter θ in the direction that makes the parameter error ϕ go to zero, provided $h \neq 0$. The rate of convergence depends on the magnitude of the signal h as well as the gain g . In order to achieve an effective convergence to zero, h has to contain enough information to drive the equation (“persistence of excitation” [7]). In practice this is always achieved in VRM applications because the output current does

not remain constant. Moreover, with a digital implementation of the algorithm, once the parameter error converges to zero the persistence of excitation requirement is not necessary anymore and the correct value of θ can be stored in a register.

In order to obtain the signal h , the output current i_o needs to be filtered according to (7) by the transfer function

$$D(s) = \frac{Z_{ref} + G_{vi}}{1 + G_{vd}K}. \quad (11)$$

By using (3), this equation can also be written as

$$D(s) = -F \cdot \frac{G_{vd}}{1 + G_{vd}K}. \quad (12)$$

The feedforward path with the gain adaptation algorithm is shown in Fig. 4. This implementation requires a filter consisting of a replica of the plant transfer function G_{vd} and the feedback controller K , one integrator, and two multipliers. The output d_{ff} is the duty-cycle command that is added to the output of the feedback controller as in Fig. 3.

The adaptation algorithm was simulated using representative values for the power train and controller. The simulations of the output current step down response are shown in Fig. 5 and compared to the case of fixed-gain feedforward and no feedforward. It can be seen that, while output current feedforward improves the transient response, it is not a good response due to the uncertainty in the value of the inductor. With adaptive-gain feedforward, the transient response improves considerably and remains unaffected by the uncertainty in the inductor value.

III. DIGITAL IMPLEMENTATION

In Fig. 4 it can be seen that the transfer function $D(s)$ of (12) is implemented in two parts. The output current i_o is filtered with F , and then processed with the feedback connection of G_{vd} with K . The first part is shared with the actual feedforward path, so it will already be implemented. The second part has a total transfer function equal to

$$\tilde{D}(s) = \frac{G_{vd}}{1 + G_{vd}K}. \quad (13)$$

(Notice that the minus sign is carried to the output and into the gradient search (9).) The algebraic expression for this transfer function is of fourth order, but it will be shown that it can be simplified to a second-order expression.

The bode plots of $D(s)$ and $\tilde{D}(s)$ are shown in Fig. 6 for a representative set of parameters. In the figure it can be seen that the range of frequencies where the magnitude of the filter $D(s)$ is significant is around $[10^4, 10^7]$. In this frequency range, the filter can be approximated as a second order filter with a zero at the origin. Therefore, since F has a zero at the origin, $\tilde{D}(s)$ can be approximated as

$$\tilde{D}(s) \approx \frac{k}{\frac{s^2}{\omega_n^2} + \frac{2\xi}{\omega_n}s + 1}, \quad (14)$$

where k , ω_n and ξ are to be determined empirically. With this approximation, and after suitable choice of parameters, the transfer functions are the ones shown in Fig. 6.

TABLE I
FPGA BOARD CHARACTERISTICS.

FPGA board	
FPGA	Xilinx XCV2P40-7FG676
ADC for v_e	ADC10030CIVT LSB = 2mV
ADC for i_{ff}	ADC10030CIVT LSB = 71mA/ μ s
f_{sw}	372kHz
f_{samp}	$4 \times f_{sw} = 1.49MHz$
sampling delay	210ns
computation delay	84ns
DPWM resolution	11 bits = 13ns

An equivalent digital filter in the z -domain can be extracted from (14) using a bilinear transformation. The general form of such a digital filter is

$$\tilde{D}(z) = \alpha \cdot \frac{z + a_0}{z^2 + b_1z + b_0}. \quad (15)$$

The filter coefficients can be approximated by sums or subtractions of powers of two, so the filter can be implemented efficiently using only adders and shift operations. The effect of these approximations, as well quantization effects, can be analyzed by simulation to reach a reasonable trade-off between accuracy and cost of implementation.

In the experimental setup used, filter F is implemented analogically using an operational amplifier to perform the derivative of the output current signal with an extra high-frequency pole. The output of this filter is digitized and used as the feedforward command i_{ff} . This same signal is used as an input to filter $\tilde{D}(z)$ in order to perform the gain adaptation. The value of v_e , on the other hand, is already available in digital form at the digital feedback controller. The overall circuit of the implementation is shown in Fig. 7.

IV. EXPERIMENTAL RESULTS

The adaptive feedforward control is implemented digitally with an FPGA board and connected to a prototype four-phase VRM power train. The FPGA board contains a Xilinx VirtexII-Pro chip and two A/D converters for sampling the error voltage and the derivative of the output current. PWM is implemented digitally in the FPGA using a combination of a counter with an external delay line and dither [8]. The feedback controller is a PID implemented in the FPGA. The output current is measured using a sense resistor. The characteristics of the two boards are presented in Tables I and II.

A high-level block diagram of the FPGA implementation is shown in Fig. 8. The output voltage is sensed using resistive averaging of the voltages across the output capacitors of each phase. Twisted pairs are used to connect the differential signals to the input of the differential amplifiers. There is a differential stage for each signal, followed by a conversion to a ground-referenced voltage with an adequate common-mode voltage for the ADCs.

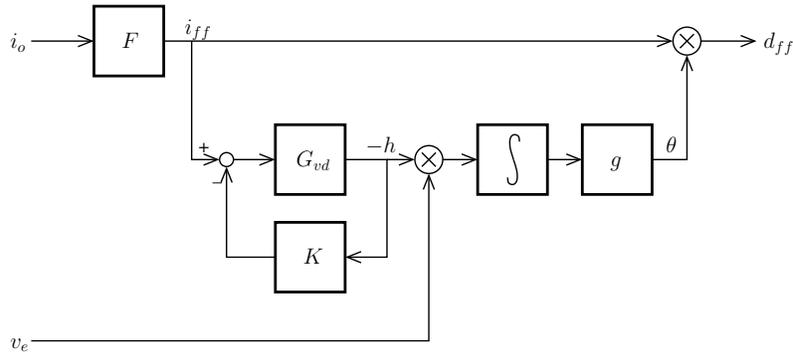


Fig. 4. Feedforward path with gain adaptation algorithm.

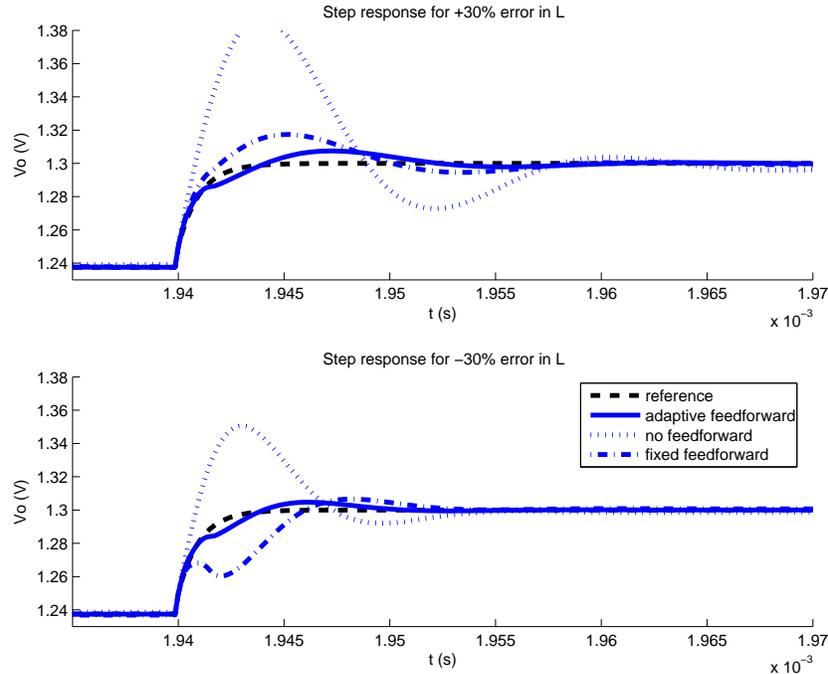


Fig. 5. Simulation of an output current step down response under three different conditions: without feedforward (dotted), with fixed-gain feedforward (dash-dotted), and with adaptive-gain feedforward (solid). The top figure corresponds to an initial feedforward gain error of +30%, and the bottom one to an error of -30%.

TABLE II
POWER TRAIN BOARD CHARACTERISTICS.

Power train board	
# phases	4
V_{in}	12V
V_{ref}	1.2V
R_{LL}	1.5m Ω
R_{sense}	1.5m Ω
L	300nH per phase
C	1.2mF
R_{esr}	1.2m Ω
top switch	2 \times Si4892DY
bottom switch	2 \times Si4362DY
drivers	LM27222

The experimental results are shown in Figs. 9, 10, 11, and 12. A 30A step (from 5A to 35A) is generated with a resistive load fired by a fast MOSFET. In Fig. 9 only the feedback controller is operating and an undershoot of about 50mV with respect to the new steady-state value is observed in the transient response. In Fig. 10, the feedforward path is enabled with a fixed gain that is less than the optimal value, a situation that may occur in practice due to the uncertainty in the power train components. The transient response improves and the undershoot is reduced to around 30mV. In Fig. 11 a similar situation is presented, but this time the fixed gain is greater than the optimal, resulting in an overshoot of around 10mV followed by an undershoot of around 25mV. Finally, in Fig. 12 the adaptive feedforward method is enabled, and

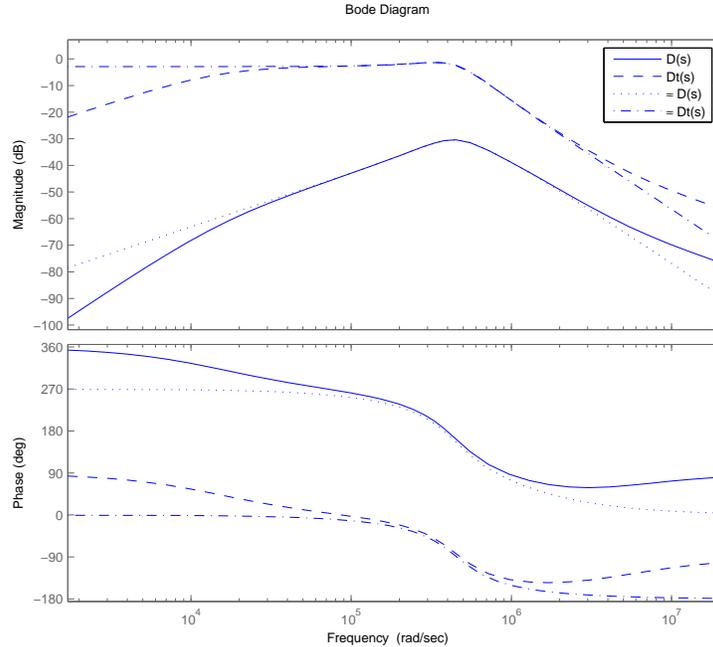


Fig. 6. Bode plot of $D(s)$ (solid), $\tilde{D}(s)$ (dashed), and their approximations (dotted and dash-dotted respectively).

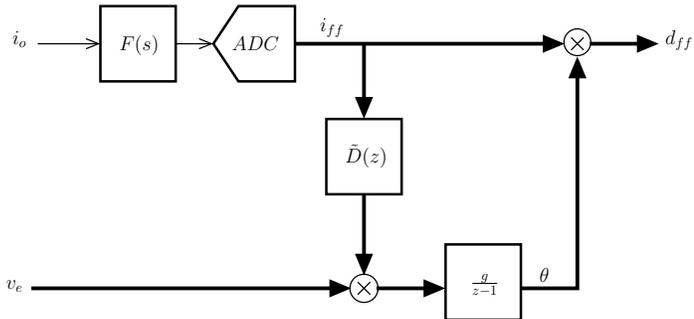


Fig. 7. Adaptive feedforward implementation. Digital signals are shown with bold lines.

the gain converges to a value that provides the best transient response achievable in this setup with an undershoot of around $20mV$.

V. CONCLUSIONS

In this paper, an adaptive control method was presented that tunes the gain of an output current feedforward path in VRM applications. The adaptation method is based on a gradient search that uses the correlation between the voltage error and the feedforward signal to minimize the parameter error. Convergence of the method is guaranteed as long as the output current changes sufficiently to excite the adaptation system. Once the parameter error converges to zero the feedforward path is tuned and no additional excitation is necessary.

The method was implemented digitally in an FPGA. Experimental results show a substantial improvement in the

transient response of a VRM prototype board with respect to control systems with only feedback and with fixed but detuned feedforward.

ACKNOWLEDGMENTS

The authors want to thank Kenny Zhang for his help with the experimental setup. This work was supported by the UC Micro program, National Semiconductor, and Fairchild Semiconductor.

REFERENCES

- [1] R. Redl, B. Erisman, and Z. Zansky, "Optimizing the load transient response of the buck converter," in *Proc. IEEE Applied Power Electronics Conference*, vol. 1, 1998, pp. 170–176.
- [2] K. Yao, M. Xu, Y. Meng, and F. C. Lee, "Design considerations for VRM transient response based on the output impedance," *IEEE Tran. on Power Electronics*, vol. 18, no. 6, pp. 1270–1277, Nov. 2003.
- [3] K. Yao, Y. Ren, J. Sun, K. Lee, M. Xu, J. Zhou, and F. C. Lee, "Adaptive voltage position design for voltage regulators," in *Proc. Applied Power Electronics Conference*, 2004.
- [4] A. Peterchev and S. Sanders, "Load-line regulation with estimated load current feedforward: Application to Voltage Regulation Modules," in *Proc. IEEE Power Electronics Specialists Conference*, 2004.
- [5] R. Redl and N. Sokal, "Near-optimum dynamic regulation of dc-dc converters using feedforward of output current and input voltage with current mode control," *IEEE Tran. on Power Electronics*, vol. 4, no. 1, pp. 181–191, July 1986.
- [6] G. K. Schoneman and D. M. Mitchell, "Output impedance considerations for switching regulators with current-injected control," *IEEE Tran. on Power Electronics*, vol. 4, no. 1, pp. 25–35, Jan. 1989.
- [7] K. J. Åström and B. Wittenmark, *Adaptive Control*. Addison-Wesley, 1989.
- [8] J. Zhang and S. Sanders, "A digital multi-mode 4-phase IC controller for VR applications," in *Proc. Applied Power Electronics Conference*, 2007.

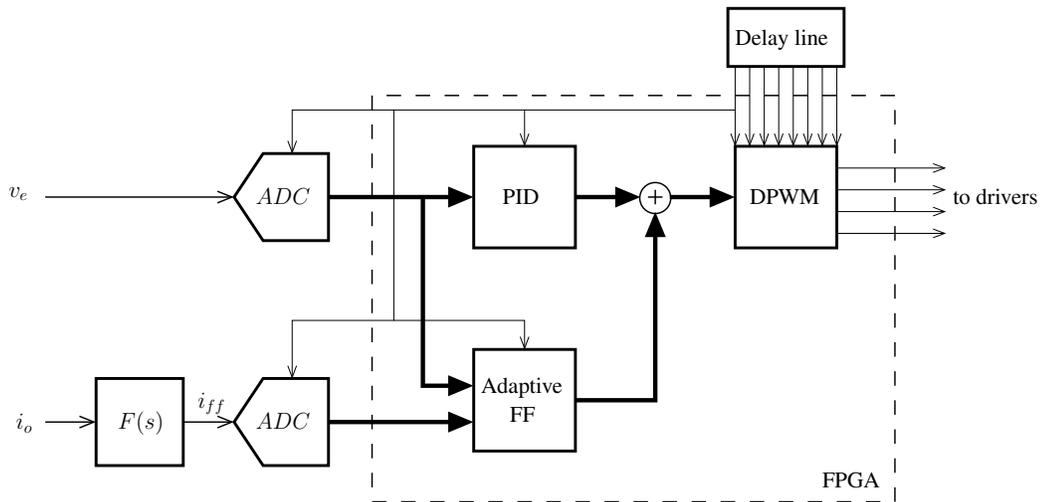


Fig. 8. FPGA implementation block diagram.

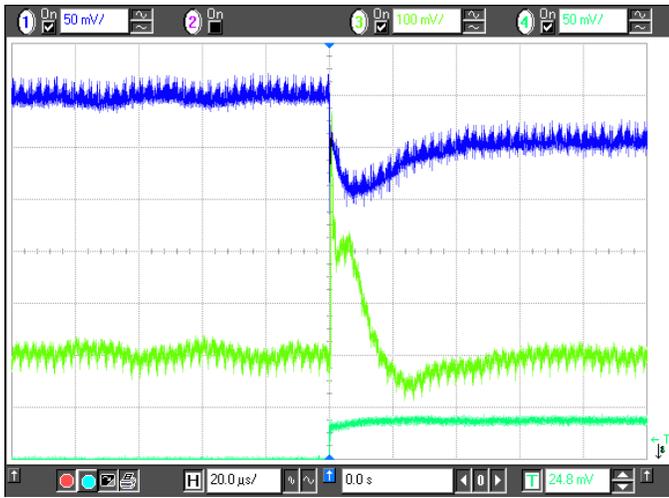


Fig. 9. Step response with feedback only. Top v_o (50mV/div), middle i_{ff} (100mV/div), bottom i_o (40A/div). Time axis 20μs/div.

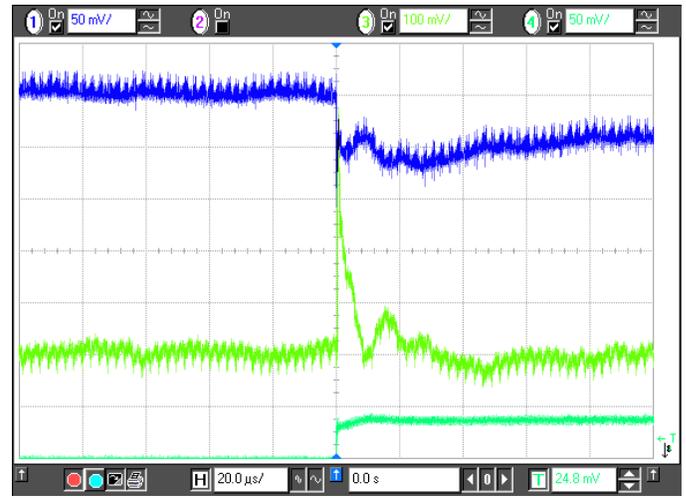


Fig. 11. Step response with large fixed-gain feedforward. Top v_o (50mV/div), middle i_{ff} (100mV/div), bottom i_o (40A/div). Time axis 20μs/div.

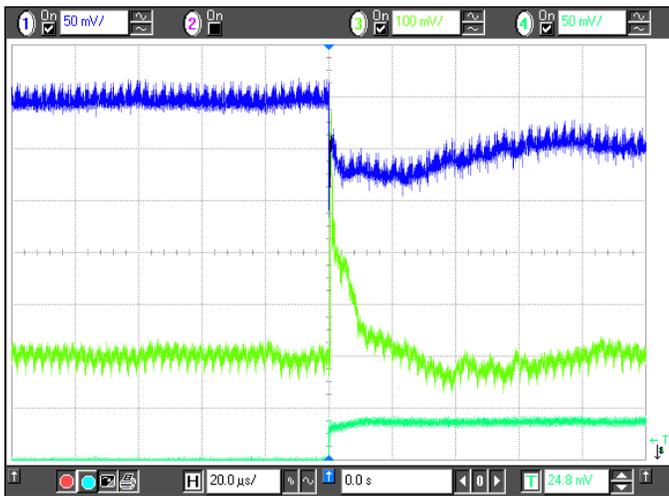


Fig. 10. Step response with small fixed-gain feedforward. Top v_o (50mV/div), middle i_{ff} (100mV/div), bottom i_o (40A/div). Time axis 20μs/div.

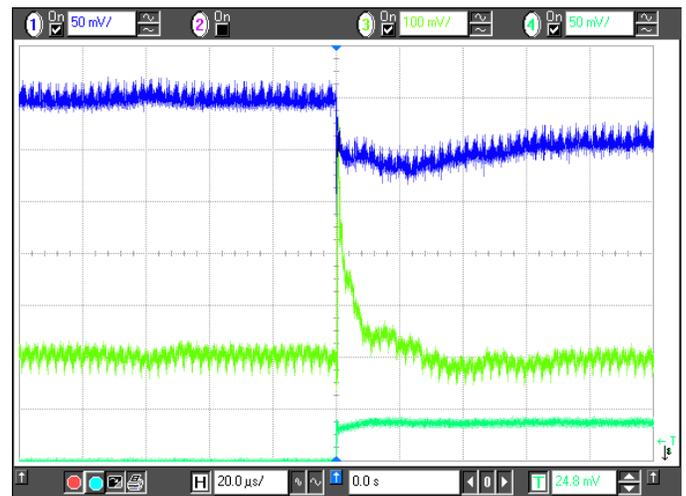


Fig. 12. Step response with adaptive feedforward. Top v_o (50mV/div), middle i_{ff} (100mV/div), bottom i_o (40A/div). Time axis 20μs/div.