Very Low Power Microprocessor Cell: Design, Fabrication and Test

[1]Pablo Castro, [1]Andrés Merello, [1]Sebastián Sayas, [1]Conrado Rossi
{pcastro,amerello,ssayas,cra}@fing.edu.uy

[1] Instituto de Ingeniería Eléctrica, Facultad de Ingeniería, Universidad de la República, Montevideo, Uruguay.

Abstract

We describe the development and test of a microprocessor cell intended for very low power applications. A novel design methodology using a VHDL simulation based consumption estimation tool was followed. The microprocessor cell was successfully tested exhibiting a low power consumption as intended. The strong correlation between measurements and simulation validates the chosen design methodology.

1. Introduction

The growing demand for application-specific low-power SOCs for several embedded applications has prompted our research on RISC microprocessor core architectures in order to achieve a reduction in power consumption. The mainstream commercial and academic research efforts focus mainly on performance [AGE 05]. However, we believe there is room for improvement in terms of consumption, particularly for low speed applications [FLY 05].

This IC complements other projects within our Microelectronics Research Group which, as a whole, are headed to developing very low power, short range, radiofrequency communication systems. These systems need very limited processing capabilities which must be fulfilled with the minimum possible consumption in order to extend battery life.

2. Project Description

This project addresses the above problem through the development of a microprocessor cell with the following features: 8-bit Industry Standard RISC architecture, very low power consumption [PIG 95a][PIG 95b], capable of working down to a clock frequency of 0Hz, low voltage supply [PIG 95a][PIG 95b], standard-cell based design, portability to different fabrication technologies

2.1 Design Flow

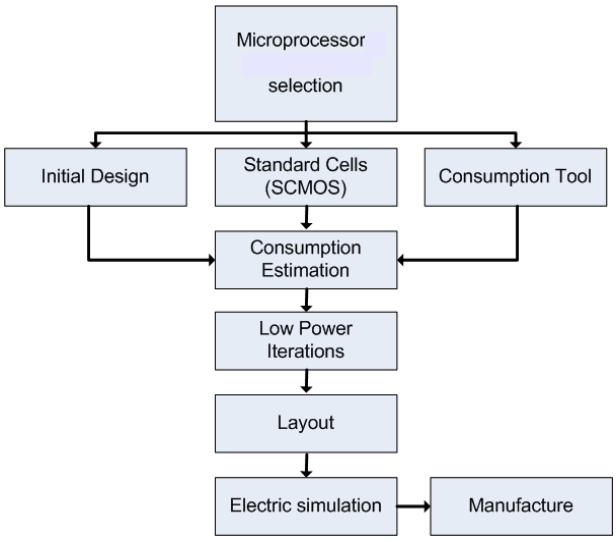

Fig 1. – Design Flow

A research of present microcontroller market was performed in order to select the architecture for the microprocessor. The selected architecture implements a well known industry programming model, providing an easy path for application development.

The design was carried out using the VHDL language, followed by a *low power consumption oriented methodology* [CAR 01]. We began by drafting an 'initial design' which complies with functional specifications regardless of the power consumption objective. This 'initial design' was synthesized to a structural VHDL description based on a standard cell library. Then, power consumption simulations were performed with a new VHDL based research tool [AMA 04], which performs a simulation while recording consumption based on the structural description of each block and a characterization of the standard cells. Simulations were performed using, as *benchmarks, some* test assembler programs. We then focused on those blocks of higher power consumption to tweak the internal architecture for optimal power consumption.

The final design was synthesized block by block obtaining structural descriptions in turn used as inputs for an automatic place and route layout tool. In order to improve total area expenditure, a semi full custom layout design style was adopted on repetitive blocks such as the internal STACK. A circuit extraction was performed on the microprocessor final layout. This circuit was simulated on a SPICE environment while running specific instructions and small applications.

2.2 Internal Architecture

The internal architecture of the microprocessor cell is divided in two blocks as shown in Fig. 2:

- *Operation Block:* It is composed by the internal registers of the µP (accumulator register: W, Status register: STATUS, the Instruction Register: IR, the Program Counter: PC and other specific registers such as: FSR and PCLatH), the Arithmetic Logic Unit (ALU), the internal STACK and the Data Memory Decoder Block: DMDB.
- *Control Block:* It is composed basically by a state machine specially designed to improve the low-power consumption feature. A 'Sleep' block that puts the µP in an extra low-power consumption state until awakened by an external interrupt is implemented using *Clock Gating* techniques.The *Control Block* performs the opcode reading, decoding, and then controls the data flow in the *Operation Block* in order to complete the operation.

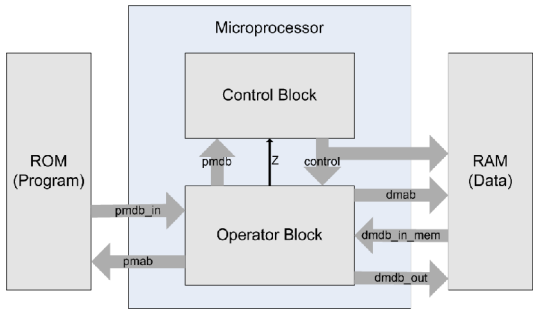

Fig. 2 - Internal Architecture

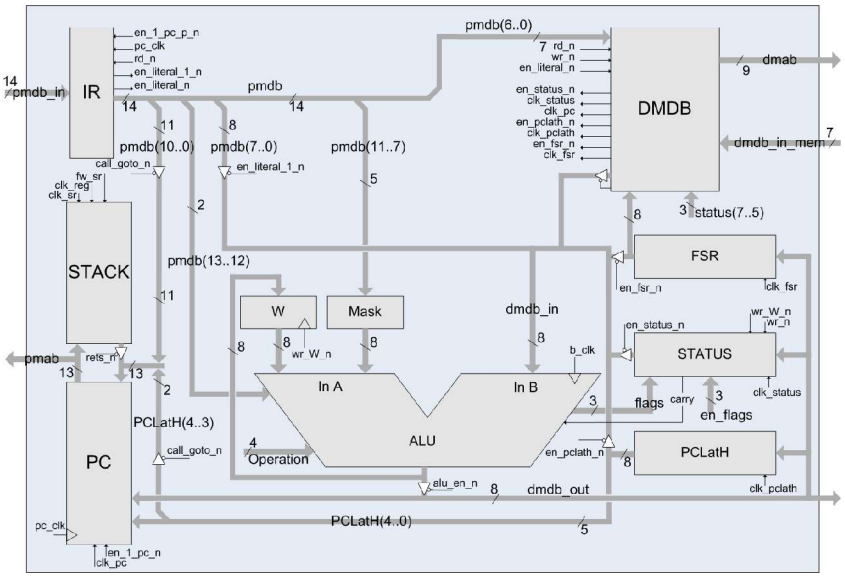

Fig. 3 - Internal architecture of the Operation Block

3. Design Optimization

As the ALU and the Control Block state machine alone take an 80% of the total power consumption of the 'initial design', our design improvements were performed on these blocks.

Control Block: Power consumption improvements were achieved on this block through selection of an appropriate state coding for the state machine. The state coding in the 'initial design' was implemented by the automatic synthesis tool without attempting to control the coding. In order to allow exploration of the Design Space in terms of state coding and power consumption, different codes were implemented directly in the VHDL description. Fig. 5(a) shows a comparison between results obtained with the power simulation tool on two different *benchmarks* for the 'initial design' state coding and the Gray coding used for the final version.

ALU: Operations performed on this block were grouped in different ways and each group implemented with combinatorial logic. Flip-flops were used to register data for each block input in order to avoid consumption associated with undesired data transitions. Also a C*lock Gating* technique was implemented to control the flip-flop clocks.

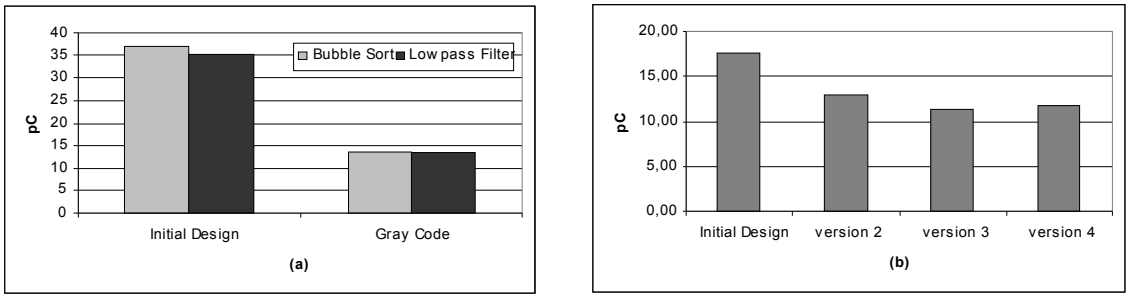

Fig. 5 – Consumption optimization. (a) Control Machine (b) ALU - Bubble Sort *benchmark*

4. Results

In order to test the IC we designed two printed circuit test boards. The first one, with no data or program memory was used to validate the functionality of the microprocessor. The opcode of each instruction and data from memory were emulated with manual switches. The clock was also manually generated and the data output and address buses state were displayed with LEDs.

The second PCB was designed to validate the functionality of the chip in a real application while measuring the power consumption of several blocks which were provided with separate supply pins (Fig. 6). The test setup included, apart form the fabricated circuit, external memory chips for program and data storage and provisions for accessing the test port. This port was designed for extended observability and some controllability of the internal blocks of the device under test so as to easy the validation tests and eventual hardware debugging. In order to measure the power consumption we used the same benchmarks as in previous power estimations and simulations.

Except for a minor bug, which can be solved by coding around, all instructions of the microprocessor set worked correctly.

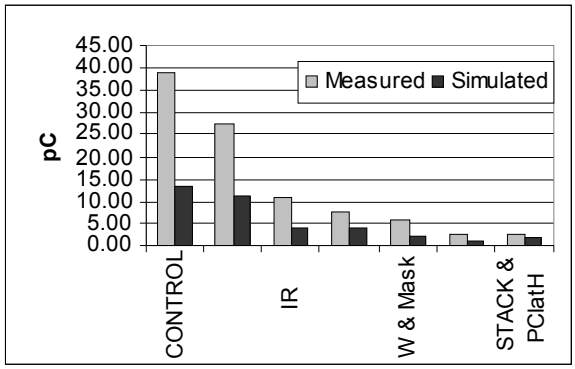

Fig. 6. Measured and Simulated consumption for different blocks

The fabricated microprocessor characteristics are:

- RISC Microprocessor
- Harvard Architecture
- 8 bits Data Bus, 14 bits Instruction Bus
- Frequency Range: 0 ~ 5 Mhz @ Vdd = 3.3 V
- Minimum Voltage operation: 1.9 V
- Current consumption in operation: 200 µA @ fclk = 2 Mhz
- Low Power mode (SLEEP): 1.2 µA @ fclk = 2 Mhz
- Easy portability to others technologies (standard cell oriented design)
- Technology: AMI ABN 1.5 µm
- Area: 4.6 mm x 4.6 mm
- Number of transistors: 16000

5. Conclusions

A first RISC microprocessor design experience has been carried out successfully using a *low power oriented methodology* [CAR 01] as the cell is fully functional and consumption data are consistent with the low power goal of the project.

Functional and consumption validations were performed on specially designed printed circuit boards. Particularly, a motherboard with I/O ports and program and data memory was implemented and an interactive game (Tic-Tac-Toe) was run successfully.

The simulation method used to fine tune the design [AMA 04] underestimates consumption by a factor around 0.35 for most individual blocks, except for those which were routed using a semi full custom technique. As the factor is quite consistent from block to block, the method is deemed valid for comparison among different architectural options. The difference between measured and simulated data were attributed to the short circuit power consumption of the logic cells (which is not estimated by the simulation tool) and the capacitance of the interconnection buses.

6. References

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