Ultra Low Power Automatic Tuning for gm-C Filters

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***Abstract*—A simple technique for on−chip tuning of ultra low power Gm−C filters is analyzed in this paper. The technique locks the filter $\frac{G_m}{C2\pi}$ frequency to an external reference clock. The proposed tuning method is tested with a low frequency first order high pass section. The tuning of this filter for different applications by changing the reference frequency is also explored. The circuit tunes the filter frequency in a range from 10 Hz to 200 Hz with a consumption of less than 800 nA.**

I. Introduction

Since the early 90's, continuous-time filters (CTF) had been a popular technique to achieve fully integrated analog filters [1], including ultra-low power, large time constants filters, as the ones needed in biomedical applications. However, time constants in CTF are obtained from the ratio of the values of different kind of devices (e.g. in Gm-C filters, transconductors and capacitors), and therefore they present very large variations in their values when compared to other alternatives such as switched capacitor filters, where the precision in the value of their time constants is dominated by well-matched structures of devices of the same kind (i.e. capacitors).

In order to achieve higher precision on the time constants of CTF an on-chip automatic tuning scheme is needed [1] [2].Indirect tuning schemes is a very popular option [2], since the tuning circuit never interferes with the signal path, although a price in power consumption is paid due to the need to duplicate part or the whole filter. These schemes, whose precision is based on the matching of these duplicated blocks, use an external reference to tune the filter, e.g. a clock signal. On this paper, we will contribute to this topic in two ways. Firstly, we propose and test an improved version of a simple, but seldom applied, scheme for on chip tuning of gm-C filters. The technique, which is mentioned in [3] and has antecedents in [4] and [5], is based on comparing the V-I ratio of the transconductor to be tuned with that of a switched capacitor resistor equivalent. Secondly, we explore the possibility to electrically tune our filter for different applications by changing the external reference (e.g. the frequency of the clock). This is a major advantage for any analog building block considering today's pressures to shrink the products time-to-market.

Therefore, we present here a reusable first-order gm-C CTF with on-chip automatic tuning. The filter can be tuned for over a decade of frequencies $(10Hz - 200Hz)$ in the range of interest of biomedical applications. The automatic tuning scheme is presented in Section II. The design is presented in section III and IV. Sections V and VI presents the results and the conclusions, respectively.

II. Automatic Tuning

Fig. 1a shows the on-chip tuning scheme described in [3]. The block labeled "Interface" stands for the required circuitry to adapt the integrator output to a signal suitable for driving a tunable resistor (e.g. a mosfet). In [4] this scheme was proposed, but not in the context of continuous time filters on-chip tuning, but as a mean to measure a transductor based on resistance or capacitance. The basic idea is the following: the switched capacitor implements a negative resistor. The sum of the currents through this negative resistor and the resistor to be tuned (R) is integrated and the integrator output used to adjust the tunable resistor. The loop will settle when both resistors are equal in magnitude. Fig. 1b shows a direct implementation of this scheme, implementing the tunable resistor with a transconductor. In this case the component at the output of the integrator due to the switched capacitor switching frequency is filtered and then a voltage controlled current source (VCCS) drives the bias current of the transconductor. [5] applies a slightly similar, but more complex scheme. The schemes of 1a and 1b have the drawback that while the inverting input of the operational amplifier that implements the integrator has not settled to the virtual ground, an error is introduced in the current through R and hence in the tuning. This implies the need for a high bandwidth for this amplifier, much increasing power consumption. We propose to use the scheme of 1c which, provided the output conductance of the transconductor is high enough, is insensitive to the voltage at the inverting input of the operational amplifier.

The block diagram in Fig. 1c shows the operating principle of the whole system. Through an externally input frequency f_{in}, a switched capacitor implements a reference resistor R_{SW}, which is compared in a control loop with a variable resistance determined by $(1/G_{m1})$, which in the scheme, will be equal with the settling of the loop. Because they are biased by the same signals, both transconductances will be identical $(1/G_{m1} = 1/G_{m2})$, and not only that, their value will be inversely proportional to a capacitor which is matched to the filter capacitor, thus the cutoff frequency of the filter f_{-3db} will be proportional to f_{in} as shown in the following equations.

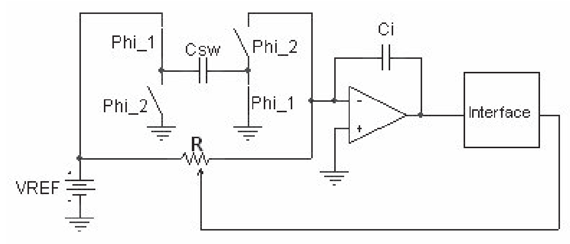
$$R_{SW} = \frac{1}{f_{in}C_{SW}} = \frac{1}{G_{m1}} = \frac{1}{G_{m2}} \tag{1}$$

and

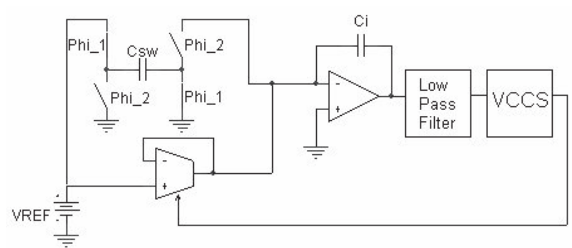
$$f_{-3db} = \frac{G_{m2}}{C_{HPF}2\pi} \quad (2)$$

So, the cutoff frequency of the filter is given by

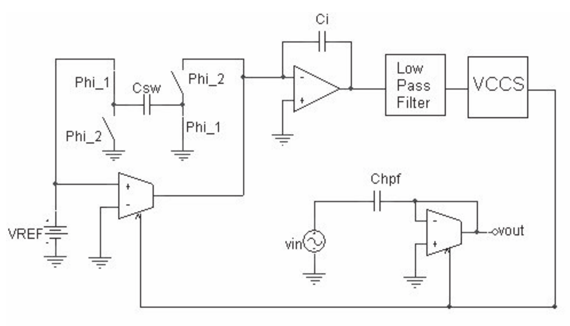
$$f_{-3db} = \frac{f_{in}}{2\pi} \quad (3)$$



(a) Blocks diagram of tuning scheme proposed in [3]



(b) Direct implementation of the tuning scheme of (a) for Gm-C filters



(c) Proposed implementation of the tuning scheme

Figure 1. Tuning method

III. DESIGN

A. Specifications

Table I summarizes the main specifications of the high pass filter: cutoff frequency (f_{-3db}) range, to be set by the external frequency, linear input range and supply voltage.

Table I
SPECIFICATIONS OF THE DESIGNED CIRCUIT

f_{-3db}	10 Hz - 200Hz
linear input range	$+/-$ 100mV
V_{DD}	2.2V - 3.3V

B. Reference Resistance (Switched-Capacitor)

As already mentioned, this block implements a reference negative resistor whose value can be approximated by eq.1. Switching phases were chosen as shown in Fig.2, where the discharge time of C_{SW} (Phi_2) takes most of the period, since this discharge is performed by the integrator operational amplifier and reducing this time increases the required bandwidth and hence consumption.

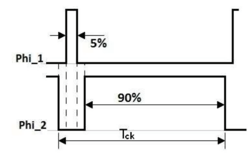


Figure 2. Phases of the switched capacitor

C. Integrator

The integrator amplifier is a two stage Miller OTA. There are two requirements that constrain the required operational amplifier f_T. First, it must discharge C_{SW}, imposing virtual ground at its inverting input in a reasonable time. An analysis in the dynamic of the integrator interacting with the Switched Capacitor and transconductor as shown in Fig. 3, allows to find how the inverting input evolves in time and the associated restriction for f_T.

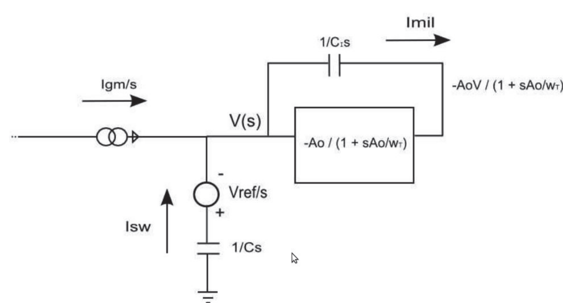


Figure 3. Dynamic of the Integrator

$$v(s) = \frac{I_{Gm}}{A_0 C_I} \frac{(1 - \frac{V_{REF}C_{SW}}{I_{Gm}})(1 + \frac{A_0}{\omega_T}s)}{1 + \frac{(C_I + C_{SW})}{C_I \omega_T} s^2} \quad (4)$$

and in the time domain

$$v(t) = \frac{G_{m1}V_{REF}}{C_I \omega_T}(1 - \exp(\frac{-C_I \omega_T}{(C_I + C_S)}t)) + ... \quad (5)$$

The second restriction in f_T, is the asymptotic value of the voltage at the inverting input, where the ec. 5 shows the main term, which should be zero, but is smaller as the f_T is higher. In our design we took f_T =30 kHz, getting a virtual ground of hundreds of μV, acceptable in our case.

D. Transconductors and VCCS

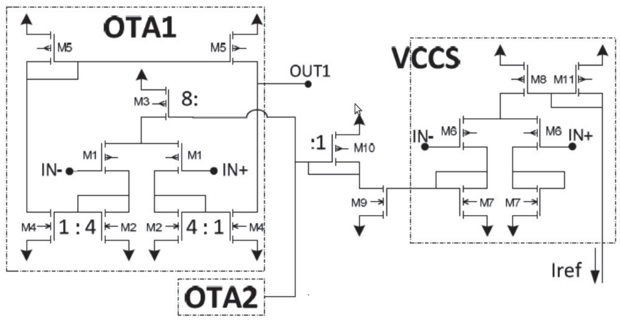


Figure 4. Schematic of the OTA(Transconductor) and VCCS.

The required linear range of the filter imposes strong inversion operation of input differential pair transistors. On the other hand, the high time constant filter demands low transconductance and hence low bias current, involving excessively long transistors. For this reason, the architecture of the transconductors is as shown in Fig. 4, where a scaling inside the block to lower its effective transconductance is applied.

The Voltage Controlled Current Source (VCCS) is shown in Fig.4. Its current to voltage ratio is a degree of freedom that is determined to assure stability and fast settling of the control loop.

E. Low Pass Filter

The voltage at the integrator output has a significant ripple due to the charge packets injected by the switched capacitor, so a low pass filter with a large time constant is necessary (cutoff frequency 6 Hz). Although an active filter could be used, for simplicity and consumption reduction we chose a passive one.

IV. Layout

The presented filter with automatic tuning was realized using 0.5 μm CMOS technology. Fig. 5 shows the layout view.

The block 1 in Fig. 5 is the operational amplifier, in which the Miller capacitor (right) takes most of the surface. Block 2, is the VCCS block. In block 3, there are the switches. In 4 are the two transconductors, located at minimal distance to improve matching. In the lower left corner, are the high-pass capacitor and switched capacitor. In the lower right is the integration capacitor. And finally, the upper half is the low-pass RC filter.

V. Simulations

In Fig. 6 is shown the simulated transient response of the extracted circuit tuning the filter to f_{-3db} = 100 Hz. The Fig. 6a shows the output voltage of the integrator block, showing an overshoot and then it settles to a constant average value. The Fig. 6b shows the current output of the VCCS, where it is visible the effect of the low pass filter. The speed of tuning is remarkable for the involved time constants, where

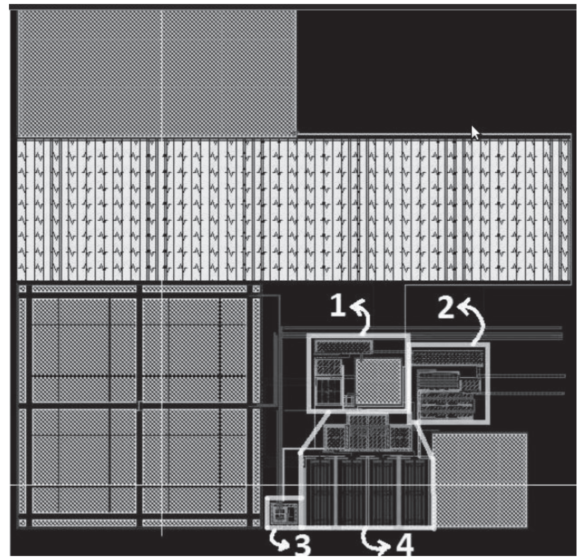
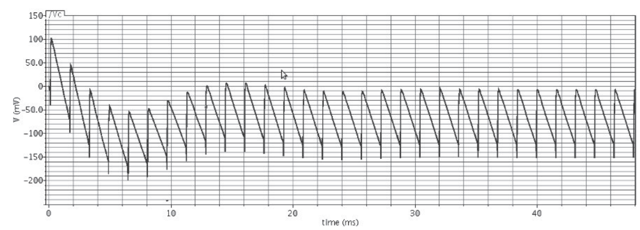
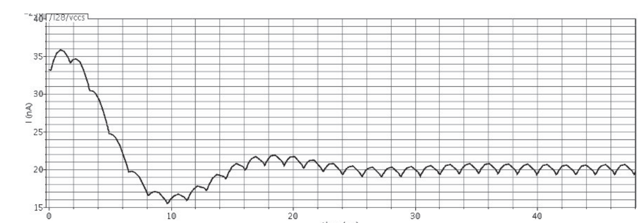


Figure 5. Layout view of the filter with Automatic Tuning.



(a) Voltage at output of integrator



(b) Output current of the VCCS

Figure 6. Transient response of the tuning circuit

approximately 25ms after the power up, the circuit would be tuned.

On the other hand Fig.7 shows the frequency response of the filter once tuned, resulting in a cutoff frequency of 102.3 Hz.

Similar simulations can be done to tune the corners, 10 Hz and 200 Hz, where tuning times are similar, while cutoff frequencies are tuned to 10.8 Hz and 205.7 Hz, respectively, all of these with V_{DD} = 2.2 V. The situation improves for V_{DD} = 3.3 V, where the cutoff frequency tuned are 101.8 Hz, 10.6 Hz and 203.7 Hz. All the simulations are performed from the extracted layout.

On the consumption side, the worst case corresponds to the tuning frequency of 200 Hz consuming 870 nA, 700 nA

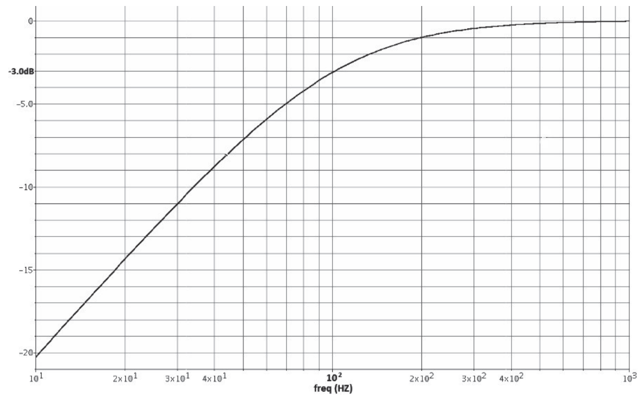


Figure 7. Frequency response of the filter once tuned

correspond to the integrator operational amplifier and 144 nA to the transconductors (72 nA each one). The minimum consumption occurs tuning 10 Hz, which is 724 nA. All these information is summarized in table II.

Table II
CONSUMPTIONS FROM THE 2.2 V V_{DD} POWER SUPPLY

	10 Hz	**200 Hz**
Total	724 nA	872 nA
OA	700 nA	700 nA
OTA	2 nA	72 nA
VCCS	17 nA	24 nA

VI. CONCLUSIONS

A simple and effective arrangement for on chip tuning of ultra low power Gm-C filters has been proposed and tested. The technique has been tested in the on-chip tuning of a first order high pass gm-C section. It has been also explored the suitability of the technique to adapt the filter to different applications by changing the external reference frequency. In this way the filter cutoff frequency was tuned in a span of more than a decade, from 10 Hz to 200 Hz. The on chip tuning circuitry took 25 ms to tune the circuit from power up, achieved a precision in the target frequency better than 8% and consumed around 800 nA.

VII. ACKNOWLEDGEMENTS

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