Bias Circuit Design for Low-Voltage Cascode Transistors

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ABSTRACT

This article presents a design methodology for the most simple cascode transistor's bias circuit, i.e. a diode-connected transistor, valid from weak to strong inversion. By taking advantage of a compact MOS transistor model, we show how the circuit can be easily designed to precisely fix the drain voltage of the cascoded transistor just above its saturation voltage. Test circuits were manufactured in a $0.35\mu m$ CMOS technology in order to test the design methodology under different operation regions (weak, moderate and strong inversion) and for long and short channel transistors. Standard deviation in measured drain voltage of the cascoded transistor is below 3% of its mean.

Categories and Subject Descriptors

B.7.m [**Hardware**]: Integrated Circuits—*Miscellaneous*

General Terms

Design, Performance

Keywords

CMOS, Low Voltage, Analog Design

1. INTRODUCTION

Cascode stages are widely use in different circuits to boost gain in amplifiers or to obtain a higher precision on current mirrors, without adding new current-consuming stages. However due to the inevitable loss of dynamic range, it is important to have bias circuits that maximize it. Usually, this means that the bias circuit should bias the cascode transistor in such a way that the cascoded transistor is biased on the edge of saturation.

Many circuits and design methodologies have been introduced in the past to solve this problem, and more recently, to solve it in all the regions of operation [1–3]. However, most of them use relative complex circuits which usually sacrifice area or consumption.

This article will show that the most simple bias circuit, a diode-connected transistor (gate connected to drain), is enough. It can be sized to precisely bias a cascode stage in any inversion level and, at the same time, have maximum dynamic range.

Although this technique is useful with any cascode transistor, we will take current mirrors as an example to explain and test it.

2. ACM MODEL AND SATURATION VOLTAGE

In order to design a circuit that fixes the drain voltage of a transistor just above saturation voltage, we need a transistor model with simple expressions for the voltage-current relationship. These expressions and they derivatives should also be valid in all regions of operation. The ACM Model [4] is a physics-based model which complies with all these requirements. In it, drain current is expressed as:

$$I_D = I_S(i_f - i_r) \tag{1}$$

where $i_{f(r)}$ is the forward (reverse) normalized current and I_S is the normalization current:

$$I_S = \frac{1}{2} n \mu C_{ox} \phi_T^2 \frac{W}{L} \tag{2}$$

Here n is the sub-threshold slope factor, slightly dependent on V_G, and μ, C_{ox}, ϕ_T, W and L have their usual meanings. In forward saturation, drain current can be approximated as

$$I_D \simeq I_S i_f \tag{3}$$

where $i_f \gg 1$ means strong inversion and $i_f \ll 1$ means weak inversion.

Pinch-off voltage is usually expressed as:

$$V_P = \frac{V_G - V_{T0}}{n} \tag{4}$$

and its relationship with the direct (reverse) normalized current and source (drain) voltage is

$$V_P - V_{S(D)} = \phi_T f(i_{f(r)}) \tag{5}$$

where

$$f(i_{f(r)}) = \sqrt{1 + i_{f(r)}} - 2 + \ln\left(\sqrt{1 + i_{f(r)}} - 1\right) \tag{6}$$

Therefore, the (normalized) output characteristic of the MOS transistor, according to the ACM model is

$$\frac{V_{DS}}{\phi_T} = \sqrt{1 + i_f} - \sqrt{1 + i_r} + \ln\left(\frac{\sqrt{1 + i_f} - 1}{\sqrt{1 + i_r} - 1}\right) \tag{7}$$

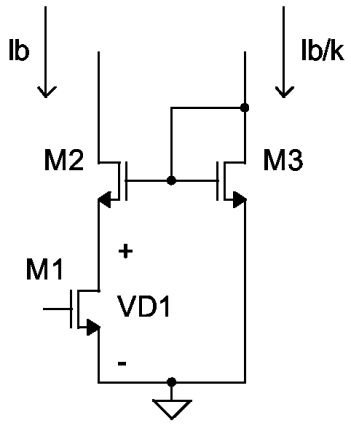

Figure 1: Proposed bias circuit for a cascode configuration.

We will define saturation voltage as in [1]. There, the authors define the "maximum" gain of a common-gate amplifier as:

$$A = \frac{gm_S}{gm_D} \tag{8}$$

where $gm_{S(D)}$ is the source (drain) transconductance, which in the ACM model is expressed as:

$$gm_{S(D)} = \frac{2I_S}{\phi_T}\left(\sqrt{1+i_{f(r)}}-1\right) \tag{9}$$

Therefore, using (7) we can write the saturation voltage, V_{DSsat}, as ([1, 4]) the V_{DS} voltage in which we achieve a certain ratio $A \gg 1$ between source and drain transconductance:

$$\frac{V_{DSsat}}{\phi_T} = \ln(A) + \left(1-\frac{1}{A}\right)\left(\sqrt{1+i_f}-1\right) \tag{10}$$

$$\frac{V_{DSsat}}{\phi_T} \simeq \ln(A) + \sqrt{1+i_f} - 1 \tag{11}$$

Using (5) its easy to see that this expression tends to the usual values, either on strong inversion ($i_f \gg 1$, $V_{DSsat} \simeq (V_{GS}-V_T)/n$) or in weak inversion ($i_f \ll 1$, $V_{DSsat} \simeq 4\ldots5\phi_T$). But, what is more, this expression comes very handy for analog designers, since inversion level, voltage gain and dynamic range are typical parameters in any design.

3. BIAS CIRCUIT DESIGN

The bias circuit should fix the gate voltage of the cascode transistor in such a way that the transistor connected at its source works in saturation. However, since this could cause a serious reduction in the dynamic range, there is a trade-off on the value of the gate voltage.

The most simple circuit to generate this voltage is a diode-connected transistor, such as M3 in Fig. 1. This circuit is certainly not new, however it is seldom used due to its allegedly loss of dynamic range due to the lack of control over voltage V_{D1}. We demonstrate that it is possible to size transistor M3 to precisely fix voltage V_{D1} near M1's saturation voltage, independently of the operating region of any of the transistors.

Let I_b and I_b/k be M2's and M3's bias current respectively. Therefore, according to equation (3) we have

$$\frac{I_{D2}}{I_{D3}} = k = \frac{i_{f2}(W/L)_2}{i_{f3}(W/L)_3} \tag{12}$$

and thus

$$i_{f3} = i_{f2}\frac{(W/L)_2}{k(W/L)_3} \tag{13}$$

With the help of equation (5) we can express the *pinch-off* voltage in transistors M2 and M3 as

$$V_{P2} = V_{D1} + \phi_T f(i_{f2}) \tag{14}$$

$$V_{P3} = \phi_T f(i_{f3}) \tag{15}$$

where $f(i_f)$ was defined in equation (6).

Here we should choose i_{f3} such that V_{D1} lies above M1's saturation voltage V_{DSsat1} by a safety margin ΔV_{margin}. Therefore,

$$V_{D1} = V_{DSsat1} + \Delta V_{margin} \tag{16}$$

Now, to relate equations (14) and (15) we will use the fact that $V_{G2} = V_{G3}$ and therefore $V_{P2} = V_{P3}$ ($V_{T02} = V_{T03}$). Thus, if we equal equations (14) and (15) and substitute V_{D1} and V_{DSsat1} with equations (16) and (11) respectively, we obtain the following design equation:

$$\sqrt{1+i_{f3}} - \sqrt{1+i_{f2}} - \sqrt{1+i_{f1}} + \ldots$$
$$\ln\left(\frac{\sqrt{1+i_{f3}}-1}{\sqrt{1+i_{f2}}-1}\right) = \ln(A) - 1 + \frac{\Delta V_{margin}}{\phi_T} \tag{17}$$

where i_{fi} is the inversion level of transistor Mi.

If we take M1 and M2 as already sized following other considerations such as speed or gain, then, we may define the following design methodology for transistor M3. First, we define ΔV_{margin} according to specifications and factor k according to the power budget. Then, we find numerically the inversion level of transistor M3 that complies with equation (17). Finally, with equation (13) we get $(W/L)_3$.

It is important to point out that both equations used in this design methodology are independent of the technology parameters as long as transistors M2 and M3 have the same V_{T0}. However, this assumption, might be wrong as we will discuss in the following example.

Let's consider the cascode current mirror in Figure 2, where for the sake of simplicity M1 and M2 are considered identical ($i_{f1} = i_{f2}$). From equation (13) we define factor α as the ratio between the inversion level of transistors M2 and M3. This is analog to the α factor defined in [1].

$$\alpha = \frac{if_3}{if_2} = \frac{(W/L)_2}{k(W/L)_3} \tag{18}$$

It is also clear that α gives us the ratio between (W/L) from transistors M2 and M3, taking into account current factor k.

Using equation (17) we can see in Figure 3 how the α factor varies with respect to the inversion level of transistors M1 and M2 (i_{f2}) for different values of A.

This Figure gives us a graphical idea of equation (17) and allow us to foresee that in many design situations we will find us with $(W/L)_2 \gg k(W/L)_3$. This implies that as long as we keep $k \geq 1$ in order to limit current consumption, we will have very different transistor's geometries, and therefore the

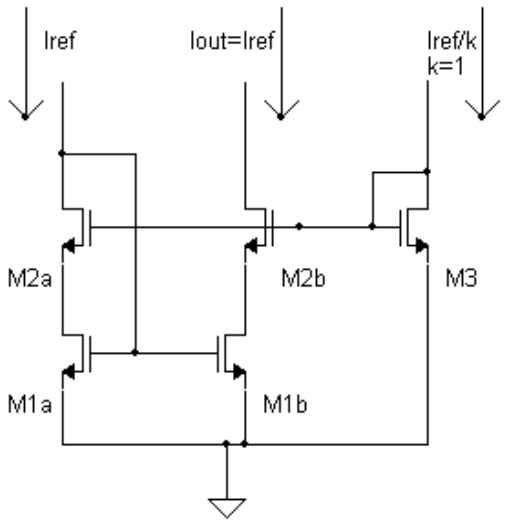

Figure 2: Cascode Current Mirror.

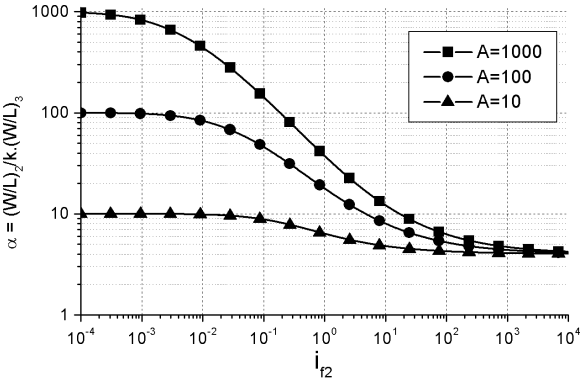

Figure 3: $\alpha = \frac{(W/L)_2}{k(W/L)_3}$ as a function of $i_{f2}(= i_{f1})$ when A varies.

constant V_{T0} assumption falls, specially when we consider short channel technologies.

To avoid this problem, we will build transistors M2 and M3 through series and parallel associations of a unitary transistor (Muni) [5]. For the sake of simplicity, we will take M1 and M2 identical again. Thus, as we can see in Figure 4, M1 and M2 will be formed by M parallel Muni transistors and M3 will be formed by N series Muni transistors.

We will show that this will allow the design methodology to be truly independent of transistor's V_{T0}, and therefore we can extend it to short-channel transistors as long as they have an output conductance small enough to reach the common-gate gain (A) considered in the definition of V_{DSsat}. The influence of other second order effects is also attenuated thanks to the matching of unitary transistors.

4. TEST CIRCUITS

To test the design methodology introduced on last section, we present four test circuits designed in a standard $0.35\mu m$ CMOS technology. All circuits have the same topology seen

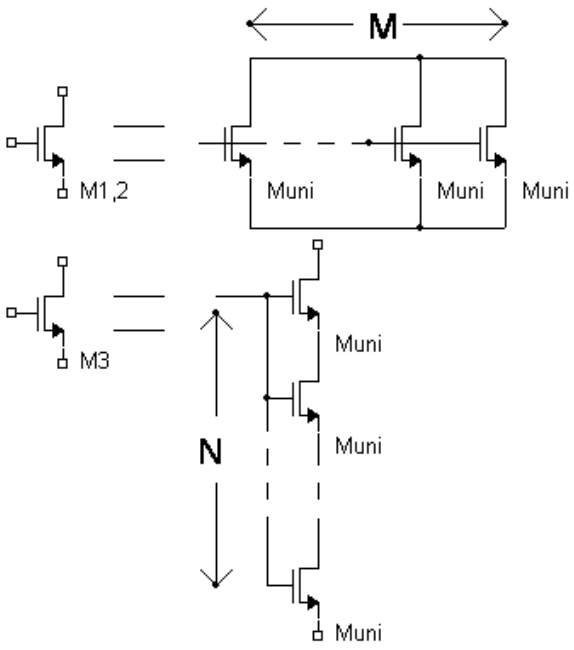

Figure 4: Series/Parallel association of transistors $M1, M2$ and $M3$

	L=5			L=0.35
	WI	**MI**	**SI**	**WI**
$\mathbf{I_D}(\mu\mathbf{A})$	0,05	0,5	5	0,5
$\mathbf{M_{UNI}}(\mathbf{W/L})$	1/5	1/5	1/5	0,5/0,35
M	3	3	3	4
N	25	7	3	18
$\mathbf{V_{D1}}(\mathbf{mV})$	262	332	541	262

Table 1: Test Circuits Design

on Figure 2. The first three use $L_{uni} = 5\mu m$ transistors and they have M1 and M2 biased in the verge of weak (WI, $i_f = 1$), moderate (MI, $i_f = 10$) and strong inversion (SI, $i_f = 100$). The last test circuit use $L_{uni} = 0.35\mu m$ transistors to test that series parallel association of transistors truly makes this design methodology insensitive to short channel effects. This last circuit has M1 and M2 biased in weak inversion (WI, $i_f = 1$). Table 1 shows the sizes and bias current of transistors and the expected V_{D1} voltage.

The design specifications were as follows: $\Delta V_{margin} = 5\phi_T$ and V_{DSsat} defined with $A = 100$. In all cases we considered $k = 1$.

5. RESULTS

Figures 5, 6 and 7 show the measured output characteristic of the $L_{uni} = 5\mu m$ cascode current mirrors (CCM) in weak, moderate and strong inversion respectively. Please note that the figures show a zoom of the characteristic around the saturation region. Each Figure also shows the output characteristic of the same current mirror without the cascode transistors (Simple Current Mirror, SCM). Finally, we show the evolution of voltage V_{D1} when V_{OUT} varies. We can clearly see in all cases that the equivalent saturation voltage of the cascode current mirror corresponds to the V_{OUT}

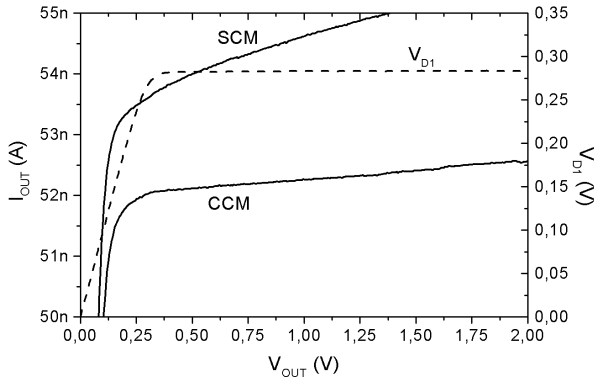

Figure 5: Cascode Current Mirror (CCM) and Simple Current Mirror (SCM) measured output characteristic when operating in WI ($L = 5\mu m$). In dashed line, measured V_{D1} as a function of V_{OUT}.

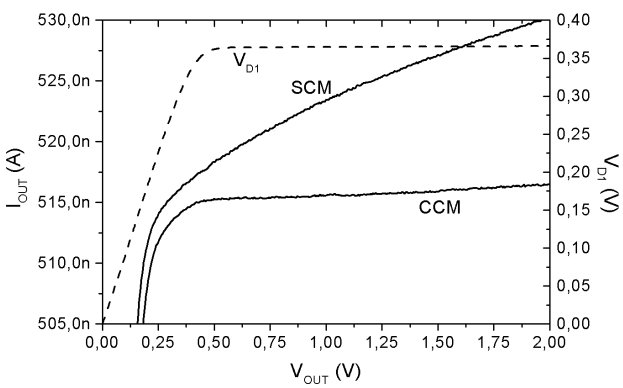

Figure 6: Cascode Current Mirror (CCM) and Simple Current Mirror (SCM) measured output characteristic when operating in MI ($L = 5\mu m$). In dashed line, measured V_{D1} as a function of V_{OUT}.

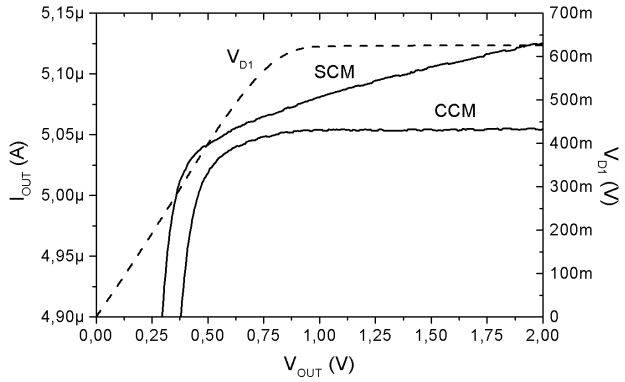

Figure 7: Cascode Current Mirror (CCM) and Simple Current Mirror (SCM) measured output characteristic when operating in SI ($L = 5\mu m$). In dashed line, measured V_{D1} as a function of V_{OUT}.

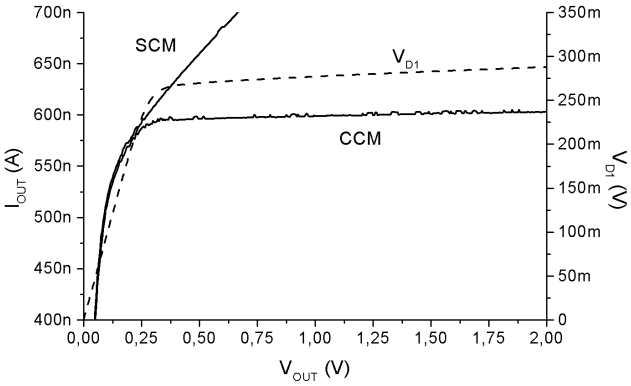

Figure 8: Cascode Current Mirror (CCM) and Simple Current Mirror (SCM) measured output characteristic when operating in WI ($L = 0.35\mu m$). In dashed line, measured V_{D1} as a function of V_{OUT}.

voltage where V_{D1} turns constant. It is visible that this equivalent saturation voltage corresponds approximately to twice the saturation voltage from the simple current mirror. This agrees with the fact that we are using transistors of the same size for M1 and M2.

Figure 8 shows a similar behavior on the experimental results of the short channel current mirrors, which means that the methodology holds where short channel effects are not negligible.

Last, Figures 9 and 10 show the behavior of voltage V_{D1} in different samples of the same run. We measured V_{D1} voltage for $V_{OUT} = 2V$ over 10 samples. Figure 9 shows that V_{D1} is always above the design value. Also, to find out the relative variation in each case, we normalized V_{D1} with respect to the mean in each measurement. This is presented in an histogram on Figure 10, where we can see that the maximum error is less than 8% and that the standard deviation is $\sigma = 2.58\%$. Therefore, all circuits fall between a 3σ interval of the mean. What is more, we can appreciate in Figure 9 that the short channel current mirrors show the largest dispersion, which is in complete agreement with the fact that mismatch is inversely proportional to gate area. Future works include measurements on more samples and a mismatch analysis on the circuit to compare with the experimental results.

6. CONCLUSIONS

In this paper we presented and validated a design methodology to bias high output swing cascode stages with the most simple bias circuit: a diode-connected transistor. The proposed methodology is valid for any level of inversion of the transistors of the circuit. This work proves that a diode connected transistor is apt to replace more complex cascode bias circuit previously reported with gains in terms of area and consumption.

We used a layout based on series-parallel association of unitary transistors which allowed us to extend the design methodology (obtained from a long channel transistor model)

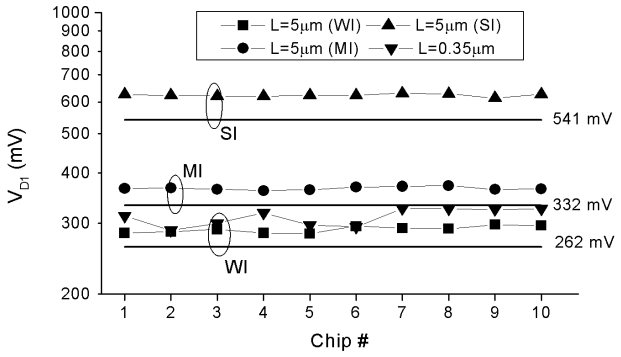

Figure 9: V_{D1} measurements for $V_{OUT} = 2V$ in 10 different chips and compared against its design value.

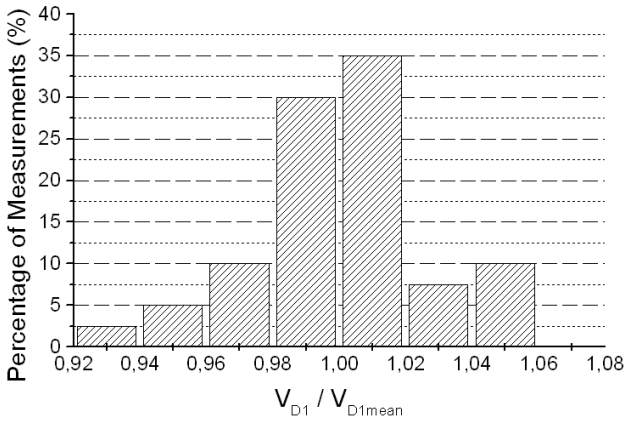

Figure 10: Histogram of measured V_{D1} normalized with each circuit's mean value.

to short channel transistors where V_{T0} variations with transistor's aspect ratio are much more important.

Experimental results validated the design methodology proposed and proved to be consistent along different samples from the same run.

7. ACKNOWLEDGEMENTS

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8. REFERENCES

[1] V. Vincence, C. Galup-Montoro, and M. Schneider, "A high-swing MOS cascode bias circuit for operation at any current level," in *Proc. Int. Symp. on Circuits and Systems (ISCAS)*, vol. V, May 2000, pp. 489–492.

[2] P. Heim and M. Jabri, "MOS cascode-mirror biasing circuit operating at any current level with minimal output saturation voltage," *Electronics Letters*, vol. 31, no. 9, pp. 690–691, Apr. 1995.

[3] B. Minch, "A low-voltage MOS cascode bias circuit for al current levels," in *Proc. Int. Symp. on Circuits and Systems (ISCAS)*, vol. III, May 2002, pp. 619–622.

[4] C. Galup-Montoro, M. Schneider, and A. Cunha, "A current-based MOSFET model for integrated circuit design," in *Low-Voltage / Low-Power Integrated Circuits and Systems: Low-Voltage Mixed-Signal Circuits*, E. Sanchez-Sinencio and A. Andreou, Eds. IEEE Press, ISBN 0-7803-3446-9, 1999, ch. 2, pp. 7–55.

[5] A. Arnaud, R. Fiorelli, and C. Galup-Montoro, "On the design of very small transconductance otas with reduced input offset," in *Proc. XVIII Symposium on Integrated Circuits and Systems Design, (SBCCI)*, Florianopolis, Brasil, Sept. 2005, pp. 15–20.