Efficiency Based Design Flow for Fully-Integrated Class C RF Power Amplifiers in Nanometric CMOS

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***Abstract*—In this work a design flow for class C radiofrequency (RF) power amplifiers (PA) with on-chip output networks in nanometric technologies is presented. This is a new parasitic-aware method intended to reduce time-consuming iterations which are normally required in fully-integrated designs. Unlike other methods it is based on actual transistors DC characteristics and inductors data -both extracted by simulation-. Starting from the output power specifications a design space map is generated showing the trade-offs between efficiency and components sizing, thus enabling the selection of the most appropriate design that satisfies the harmonic distortion requirements. As a proof of concept of the proposed method, a design example for an IEEE 802.15.4 2.4 GHz PA in a 90 nm CMOS technology is presented.**

I. Introduction

The increment of very low power wireless applications using on-chip transceivers, force Power Amplifier (PA) designers to reduce the consumption of this power hungry block as much as possible without jeopardizing its performance. The use of nanometric technologies, whereas it makes low power RF designs possible, it requires to handle the non-ideal characteristics of transistors and low supply voltages. Furthermore, full integration using on-chip, low quality factor inductors, also presents a challenge. This article presents a design approach that handles these aspects: allows the designer to select the most appropriate trade-off between efficiency and components size for a given output power and harmonic content, while taking into account actual transistors and inductors characteristics.

In constant envelope modulation schemes where linearity is not required at the output stage, as in the IEEE 802.15.4 standard, high efficiencies can be achieved due to the use of non-linear PAs with off-chip output networks (for example classes C or E). However, the utilization of fully integrated output networks adds considerable losses limiting the implementation of highly efficient PAs and making optimum design definition a challenging task. Some works have proposed parasitic-aware design flows [1], [2], but they are based on a "simulator on the loop" approach. Here, for the particular case of the class C PA, we present a solution with a simple parasitic-aware "feed-forward" approach, providing a global view of the design compromises and a way to select an initial design.

In order to solve the design trade-offs, input voltage (at the transistor gate) space -represented by its DC and RF signal components- is swept through its range using Matlab routines and a design space map is generated. This allows the designer to select the optimum PA, e.g. the one with maximum efficiency. To do so, in each design point the transistor behavior is analyzed and an optimum output network and transistor size are selected. The input network is not considered in the analysis and the efficiency studied is the one of the DC to RF power conversion.

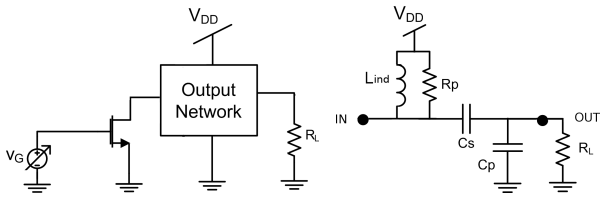
Traditional theoretical analysis of class C PAs efficiency considers a fairly ideal transistor [1], [3], [4], representing it as a simple gate-controlled current source. A more realistic approach in [5] considers a simple model of drain current dependence on drain voltage variations. Despite this approach is useful for long channel transistors, it is not the case with nanometric devices, because of its drain current strong dependence on drain voltage along with other second order and short channel effects.

Therefore an approach was developed, new as far as the authors know, which is based on actual normalized DC curves of drain current vs. gate and drain voltages. This enables to take into account second order and short channel effects, as well as sub-threshold operation. Starting from real transistor data allows to predict more accurately the simulation results, so as to reduce the number of design iterations.

Parasitic capacitances of the transistor are not considered in order to simplify the analysis, as their impact is small due to the technology used and the transistor dimensions considered when focusing in low power applications, e.g. IEEE 802.15.4 standard. Similarly, interconnections and package parasitics are not considered through this work. However, they play an important role in the design and they may be included in the output network design flow.

To study the efficiency of the output network the parasitics of the on-chip inductors were reckoned in our routines by acquiring inductor characteristics through simulation using the information provided in the foundry inductor library.

The article is laid out as follows: Section II introduces the PA architecture used in this work. In Section III the proposed design flow is described. Finally, Section IV shows a particular PA design following the procedure discussed previously.



(a) PA architecture (b) Proposed output network

Figure 1. PA architecture and output network.

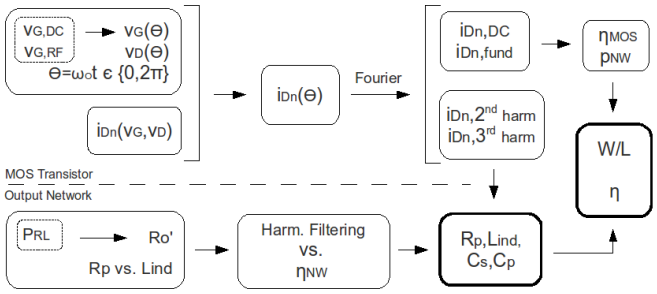


Figure 2. Flow diagram of the proposed method.

II. PA ARCHITECTURE

The schematic shown in Fig. 1a is composed by a MOS transistor and an arbitrary output network; it could represent either a class A, AB, B or C PA [3]. The operating class or conduction angle (fraction of the period where the transistor conducts) is to be determined by the gate bias v_G^{DC} and signal amplitude v_G^{RF}. Then, the expression of gate voltage v_G is

$$v_G = v_G^{DC} + v_G^{RF} sin(\omega_0 t) \tag{1}$$

with ω_0 the PA working frequency.

The output network is utilized: (i) to bias the drain to the supply voltage V_{DD}; (ii) to present a properly designed impedance value R_O to the transistor drain at ω_0 in order to obtain the desired output power; and (iii) to filter harmonic currents.

Assuming that harmonics are filtered, drain voltage is approximately sinusoidal

$$v_D = V_{DD} - v_D^{RF} sin(\omega_0 t) \tag{2}$$

where

$$v_D^{RF} = R_O I_{fund} \tag{3}$$

being I_{fund} the amplitude of the Fourier fundamental component of the drain current.

The MOS transistor drain efficiency η_{MOS} (RF power delivered to the output network over DC power taken from V_{DD}) and the output network efficiency η_{NW} (power delivered to the load over power taken from the transistor) are respectively

$$\eta_{MOS} = \frac{P_{NW}}{P_{DC}} = \frac{I_{fund} \times v_D^{RF}}{2 I_{DC} V_{DD}} \tag{4}$$

and

$$\eta_{NW} = \frac{P_{RL}}{P_{NW}} \tag{5}$$

So, PA total efficiency η can be written as

$$\eta = \eta_{MOS} \times \eta_{NW} \tag{6}$$

Drain voltage amplitude v_D^{RF} should be close to V_{DD} in order to have high η_{MOS} according to (4). Thus maximum ($v_{D,max}$) and minimum ($v_{D,min}$) of drain voltage swing must be determined considering the maximum drain voltage the technology can support (1.2 V for standard 90 nm MOS transistors in our case) and the minimum so that drain current is not cut off. There is some freedom in choosing the latter; for the studied technology $0.2V$ was found to be a good choice. Then, v_D^{RF} and V_{DD} are determined by

$$v_D^{RF} = \frac{v_{D,max} - v_{D,min}}{2} \tag{7}$$

and

$$V_{DD} = \frac{v_{D,max} + v_{D,min}}{2} \tag{8}$$

III. PA DESIGN FLOW

To generate the efficiency design space map, gate voltage parameters v_G^{DC} and v_G^{RF} are swept. The portion of the space explored is $v_G^{DC} + v_G^{RF} < v_{G,max}$. For the technology used $v_{G,max}$ is 1 V.

In each point, for a given output power (P_{RL}), transistor aspect ratio (W/L) and efficiency (η_{MOS}) are calculated, an optimum output network is designed (intended to maximize η_{NW}) and the PA total efficiency (η) is computed.

This procedure is separated into two analysis. The first one only considers transistor behavior, the second one designs the network. The former is independent of the output network used, whereas the latter is done using a particular topology. At the end of the procedure both analysis are combined to obtain the global result of efficiency and components sizing.

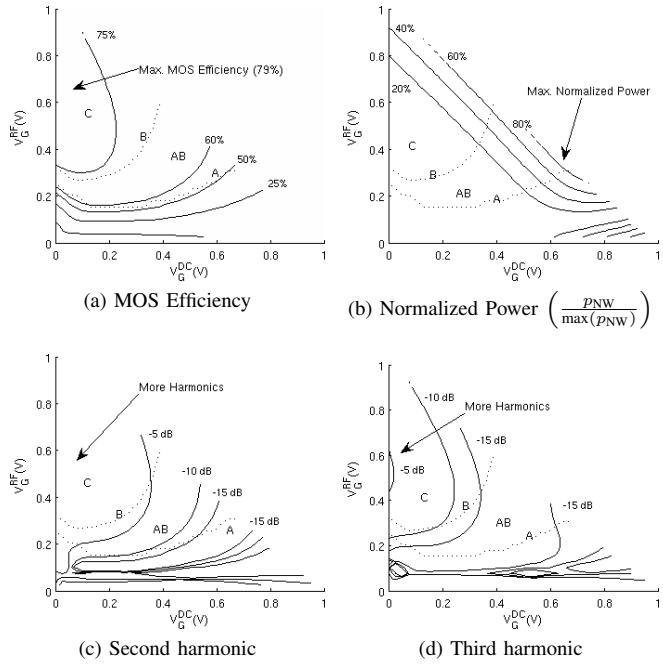
The complete design flow for each design point, implemented in Matlab routines, is shown in Fig. 2. Next subsections describe each step.

A. MOS Transistor analysis

As already mentioned, in order to model the transistor drain current accurately, its DC value is extracted from simulation (in SpectreRF with BSIM4 for the selected 90nm technology) varying both v_G and v_D. Then i_D data is normalized regarding transistor aspect ratio W/L, obtaining $i_{Dn}(v_G, v_D)$.

Using the $i_{Dn}(v_G, v_D)$ data the time domain normalized drain current $i_{Dn}(\theta)$ (with $\theta \in \{0, 2\pi\}$) is calculated starting from v_G and v_D time domain voltages, using (1) and (2). Then, its first four Fourier terms are calculated ($i_{Dn,DC}$, $i_{Dn,fund}$, $i_{Dn,2^{nd}harm}$ and $i_{Dn,3^{rd}harm}$). With the normalized current the conduction angle[1] θ_{cond}, indicator of the operating class and the amount of nonlinearity, is obtained.

[1]Here we calculate the conduction angle as the fraction of the period where the drain current is higher than the 1% of its maximum.



(a) MOS Efficiency (b) Normalized Power $\left(\frac{p_{NW}}{\max(p_{NW})}\right)$

(c) Second harmonic (d) Third harmonic

Figure 3. MOS Efficiency, normalized power and harmonics ($\frac{i_{Dn,2^{nd}harm}}{i_{Dn,fund}}$ and $\frac{i_{Dn,3^{rd}harm}}{i_{Dn,fund}}$) in the design space.

Then, from (4), η_{MOS} is calculated. Also p_{NW}, the power delivered to the output network normalized by W/L is computed using (9).

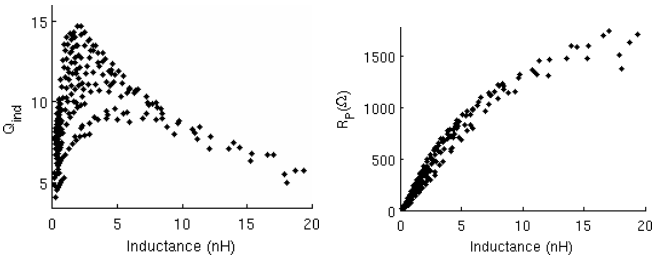
$$p_{NW} = \frac{i_{Dn,fund} \times v_D^{RF}}{2} \tag{9}$$

Figs. 3a and 3b show efficiency and normalized power contours versus (v_G^{DC}, v_G^{RF}). PA class divisions are also shown according to conduction angle. As expected, when moving from class A to class C, η_{MOS} rises (the maximum is obtained with zero bias), while normalized power drops. In Figs. 3c and 3d contours of the second and third harmonics of i_{Dn} are shown and, also as expected, harmonics rise when moving from class A to class C.

B. Output network analysis

In this work we chose to use a fully integrated π network, as depicted in Fig. 1b. Similar topologies can be found in other class C PA implementations, e.g. [6]. This network can comply with the requirements for the output network described in section II, but with the restriction that R_O must be greater than R_L. This is not a problem when low power outputs are needed (e.g. in IEEE 802.15.4), where R_O values are always higher than R_L (assumed to be 50 Ω).

This network has only one degree of freedom, for example having chosen a value for L_{ind} the values for C_s and C_p are exactly determined. It was chosen for its simplicity and for using only one inductor, as they are generally the main cause of network losses. The inductor losses, represented by its parallel resistance R_p, determine the network efficiency (network capacitors are supposed lossless in this work).



(a) Quality factor (b) Parallel resistance

Figure 4. Q_{ind} and R_p vs. L_{ind}.

Resistance R_O shown by the network at ω_0 is the parallel of R_p and $R_O{}'$, where $R_O{}'$ is the resistance converted from R_L by the π network (L_{ind},C_s and C_p) without considering the inductor losses. The power delivered to the load P_{RL} is the power taken by $R_O{}'$, so P_{RL} and the efficiency of the network η_{NW} (5) can be written as

$$P_{RL} = \frac{{v_D^{RF}}^2}{2{R_O}'} \tag{10}$$

and

$$\eta_{NW} = \frac{R_p}{R_p + {R_O}'} \tag{11}$$

Hence, a large value of parallel parasitic resistance R_p is required to achieve high efficiency. This parasitic resistance is related to the inductor quality factor as $R_p = Q_{\text{ind}} \times (\omega_0 L_{\text{ind}})$. Fig. 4 shows for the working frequency of 2.4 GHz the Q_{ind} and R_p values vs. inductance L_{ind} -for the inductor library of our technology-.

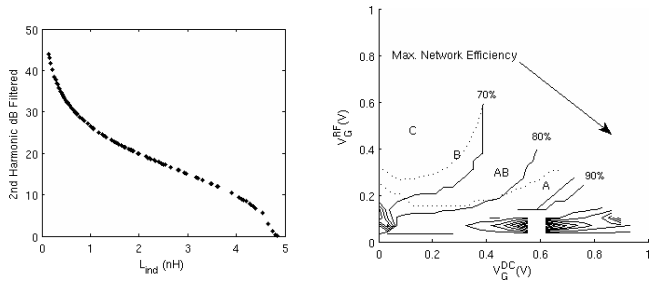
Given the required output power P_{RL} a network is designed (i.e. the capacitors values) for each inductor in the library, in order to show the correct ${R_O}'$ value (obtained using (10)). Then its amount of harmonic filtering is calculated. An example of filtering vs. inductance is depicted in Fig. 5a. The amount of filtering is calculated for the second and third harmonics (supposing the higher ones are negligible).

C. Total efficiency and components sizing

With the drain current harmonics ($i_{Dn,2^{nd}harm}$ and $i_{Dn,3^{rd}harm}$) and the harmonics filtering vs. network efficiency, the optimum network (the one that achieves the needed output filtering with highest efficiency) is chosen for each design space point. Fig. 5b shows an example of the network efficiency η_{NW} contours. As it is expected, due to the fact that η_{NW} increases with L_{ind} whereas filtering is reduced (see Figs. 4b and 5a), the network efficiency decreases when moving from class A to class C.

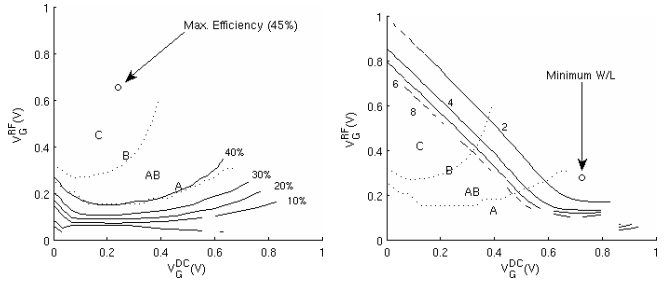
Then, combining normalized power delivered to the network p_{NW} (9) and network efficiency η_{NW} (5) the transistor aspect ratio is calculated as

$$W/L = \frac{P_{RL}}{\eta_{NW} p_{NW}} \tag{12}$$



(a) Second harmonic filtering vs. L_{ind} (b) Network efficiency η_{NW}

Figure 5. Harmonic filtering vs. L_{ind} and network efficiency contours.



(a) PA total efficiency (b) Transistor W/L (normalized to its minimum)

Figure 6. PA total efficiency and transistor W/L contours.

Finally total efficiency η is calculated with (6).

The contours of efficiency η and transistor aspect ratio W/L, (shown in Fig. 6), along with the ones of inductance and capacitance values form a design space map which can be used by the designer to select an optimum design. For example, the highest efficiency design can be obtained given certain design constrains for the size of the components. It is to be noted that this optimum may lay in any class region (A,AB,B,C) and not only in class C.

IV. Design example

This section presents a proof of concept regarding the design method proposed here. We studied the design space for a PA that achieves -20 dB for the second and third harmonics (as required by IEEE 802.15.4) at two output power requirements (0 dBm and -5 dBm). The highest efficiency configurations were selected and the predicted performances were compared with simulations carried out in SpectreRF using periodic steady state analysis.

The transistors used were 1.2 V standard NMOS with minimal channel length (100 nm). These low voltage transistors

v_G^{DC} (V)	v_G^{RF} (V)	W (μm)	L_{ind} (nH)	C_s (pF)	C_p (pF)	P_{RL} (dBm)		η (%)		$2^{\text{nd}}{}_{\text{Harm}}$ (dB)
						Pred.	Sim.	Pred.	Sim.	Sim.
0.4	0.5	76	1.7	6.7	3.8	0	-0.1	42.7	41.5	-20.3
0.2	0.8	23	4.0	1.6	2.7	-5	-5.1	41.9	40.1	-21.2

Table I
PREDICTED VS SIMULATED RESULTS

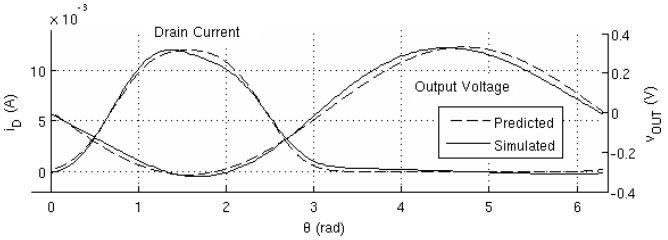


Figure 7. Comparison between Matlab and SpectreRF time-domain results.

were found to be suitable due to the low output power required. The load was set to $R_L = 50\Omega$ and to maximize the drain voltage swing (as explained in Section II) V_{DD} was chosen to be 0.7 V.

Table I presents the designs and their predicted and simulated performance. In Fig. 7 the waveforms of drain current and output voltage are given for the 0 dBm case.

Both performance and time-domain comparisons show good agreement between predicted and simulated results.

V. Conclusion

A design flow intended to find highest efficiency designs for Class C RF Power Amplifiers is proposed. This method provides the designer with a design space map of efficiency and components (transistors, inductors, capacitors) parameters starting from output requirements (load, power, harmonics) and actual transistors and inductors data.

The method has been verified by comparing its predicted results with simulations carried out in SpectreRF for an IEEE 802.15.4, 2.4GHz design example in a 90nm technology, with very satisfactory results.

VI. Acknowledgements

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