Common Source LNA Design Space Exploration in All Inversion Regions

Berardi Sensale, Rafaella Fiorelli and Fernando Silveira

Instituto de Ingeniería Eléctrica, Facultad de Ingeniería

Universidad de la República

Montevideo, Uruguay.

{bsensale,fiorelli,silveira}@fing.edu.uy

Abstract—**This work presents a design space exploration procedure valid in all inversion regions, from weak to strong, applied to the design of a CMOS CS-LNA. The exploration is done in terms of current consumption, gain and noise figure in the design space (I_D, $\frac{g_m}{I_D}$) providing insight into the trade-offs in the selection of the inversion level of the main LNA transistor. Finally comparisons between the MATLAB design space exploration and BSIM3v3 simulations using Spectre-RF are done, through the design example of a 900MHz CS-LNA implemented in a $0.35\mu m$ CMOS technology.**

I. INTRODUCTION

In autonomous RF applications, one of the main challenges at the moment of design are the strong power constraints, and the noise limitations (particularly for front-end circuits). To consider all the possible trade-offs involved in the design of these circuits it is interesting to make a design space exploration of their most important characteristics.

In this work it is presented the design space exploration of a single-ended common source low noise amplifier (CS-LNA), considering noise figure (NF) and gain as its basic characteristics, and taking into account all inversion levels.

Previous works have presented some design space explorations, but considering operation of the transistor in strong inversion [1], or in all inversion regions but not considering the inductor realization constraints and with noise expressions that require some corrections [2]. Another works [3], [4] present an optimization of an LNA but this case is for a common-gate structure; it is interesting to observe that in those works the all-region EKV model is used. In [5] a design of a CS-LNA is done in the weak inversion region, but no space exploration is done therein.

With the aid of MATLAB, the design space exploration is carried out using the gain and the NF of the CS-LNA. The transistor model used is the all-region ACM CMOS model. Size limitations due to using on-chips inductors are also studied and included in the exploration. But, in order to focus this work on the transistor characteristics exploration, the inductors are considered ideal, which is obviously not the actual case. The extension of this work to also include inductors resistance modeling will be treated in future work. Following a design flow, the complete set of the LNA parameters is obtained. In addition, a discussion of how the inversion level affects the current consumption, the gain and the noise figure of the CS-LNA is developed.

This work is organized as follows. In section II is done a brief review of the transistor model used. Section III gives the description and behavior of the CS-LNA. The design exploration and results are given in section IV and V. Finally a design example is described in VI.

II. ACM MODEL

For the theoretical deductions and simulations, the one-equation- all-region MOSFET model [6], [7] has been used to describe the transistor behavior. This is a physical-based compact model valid for all inversion levels which conserves charge and preserves the symmetry of the transistor. In this design, the transistors are considered to be working in the saturation region. In the ACM model, the drain current is expressed as the difference between the forward I_F and reverse I_R components,

$$I_D = I_F - I_R = I_S(i_f - i_r) \tag{1}$$

where

$$I_S = \frac{1}{2}n\mu C'_{ox}\phi_t^2\frac{W}{L} \tag{2}$$

I_S is the specific current, which is proportional to the aspect ratio of the transistor. V_G, V_S and V_D are the gate, source, and drain voltages, with reference to the substrate. μ is the effective mobility, ϕ_t is the thermal voltage, C'_{ox} is the gate oxide capacitance per unit area and n is the slope factor, slightly greater than unity and weakly dependent on the gate voltage. Parameters i_f and i_r are the normalized forward and reverse currents, or inversion levels at source and drain, respectively. Note that, in the saturation region, the drain current is almost independent of V_D; therefore, $i_f >> i_r$ and $I_D \cong I_F$. The small-signal transconductances g_m, g_{m_s} y g_{m_d} (gate, source and drain transconductances) are given by

$$g_{m_{s(d)}} = -\mu\frac{W}{L}Q'_{I_{S(D)}}\frac{2I_S}{\phi_T}\left(\sqrt{1+i_{f(r)}}-1\right) \tag{3}$$

$$g_m = \frac{g_{m_s}-g_{m_d}}{n} \tag{4}$$

The other small-signal parameters can also be derived in terms of the inversion levels. For the sake of simplicity a complete list of expressions is not here presented, but ACM
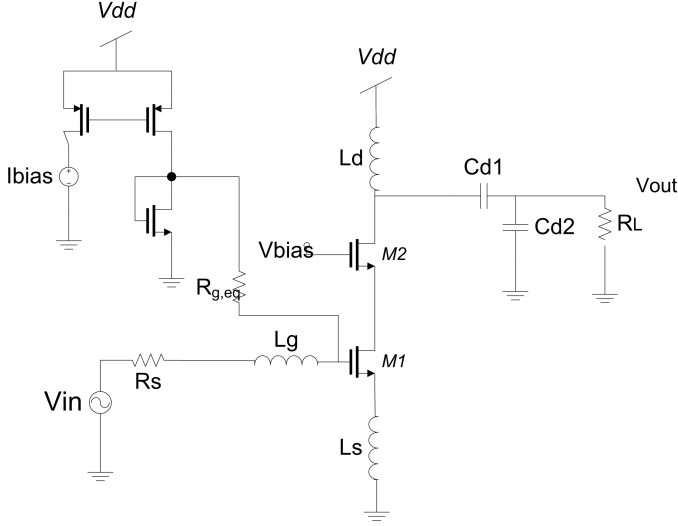
Figure 1. CS-LNA with source degeneration schematic view.

intrinsic capacitances and the transit frequency f_T equations [6] were employed throughout the design process.

Our previous experience in using this $0.35\mu m$ technology [8], [9] tells us that it is possible to neglect short channel, velocity saturation and mobility reduction effects, considering the fact that there is no interest in working in deep strong inversion. Therefore, the considered transistor model is a long channel one, and this election is asserted by the agreement between calculation and simulations.

III. CS-LNA DESIGN

A. Circuit description

The circuit is a single-ended common source narrowband (CS-LNA) with inductive source degeneration, as shown in Fig.1. It comprises the transistor M_1 and the inductors L_g and L_s, which fix the gain and the input impedance of the circuit. The cascode transistor M_2 isolates the output from the input. L_d, R_d and C_d are part of the output impedance network. In this work the sizes of M_1 and M_2 are taken equal.

Due to the topology characteristics it is a narrowband device, as the input impedance is real only at the resonant frequency. The input impedance is:

$$Z_{in}|_{s=j\omega_0}(s) = \left(s(L_g + L_s) + \frac{1}{sC_{gs}} + \frac{g_m}{C_{gs}}L_s\right)\Big|_{s=j\omega_0}$$
$$= \frac{g_m}{C_{gs}}L_s = \omega_T L_s \qquad (5)$$

where

$$\omega_0 = \frac{1}{\sqrt{(L_g + L_s)C_{gs}}} \qquad (6)$$

At f_0, G_m -the total equivalent transconductance of (L_g, L_s and M_1)- is Q_{in} times g_m, with Q_{in} the ratio between the input voltage and the gate-to-source voltage:

$$G_m(\omega)\Big|_{\omega=\omega_0} = \frac{i_{M_1}}{v_{in}} = \frac{i_{M_1}}{v_{gs_1}}\frac{v_{gs_1}}{v_{in}} = g_m \cdot Q_{in}$$
$$= \left(\frac{g_m}{\omega_0 C_{gs}(R_s + \omega_T L_s)}\right)\Big|_{\text{if } R_s = \omega_T L_s}$$
$$= \frac{1}{2\omega_0 L_s} \qquad (7)$$

From (7), considering a source resistance R_s and an output load R_L, the voltage gain is:

$$A = G_m \cdot \frac{R_L}{2} = \frac{\omega_T}{\omega_0}\frac{R_L}{4R_s} \qquad (8)$$

and the power gain is

$$G = \left(\frac{\omega_T}{\omega_0}\right)^2 \frac{R_L}{4R_s} \qquad (9)$$

The *NF* of this circuit is:

$$NF = 10log(F) \qquad (10)$$

with *F*, the Noise Factor, given by [1], [10]:

$$F \cong 1 + \frac{\gamma}{\alpha}\frac{\chi}{Q_L}\left(\frac{\omega_0}{\omega_T}\right) + 4\left(\frac{\omega_0}{\omega_T}\right)^2 \frac{R_s}{R_L} \qquad (11)$$

where γ is the channel thermal noise coefficient and $\alpha = \frac{g_m}{g_{d0}}$ -following the notation of [1]-; Q_L is the quality factor of L_g and χ is equal to [1], [11]:

$$\chi = 1 - 2|c|\sqrt{\frac{\delta\alpha^2}{5\gamma}} + \frac{\delta\alpha^2}{5\gamma}(1 + Q_L^2) \qquad (12)$$

where c is the correlation coefficient between M_1 gate and drain current noise ($c \simeq -0.395j$) and δ is the gate noise coefficient.

B. Design flow

For a complete CS-LNA design, the following parameters must be computed: L_g, L_s, M_1 width W_{M_1}, M_1 transistor current I_D. M_1 transistor length L_1 is chosen the smallest available to reach the highest f_T for a certain I_D. Requirements of *NF*, current consumption, Z_{in} and gain must be fulfilled.

The design flow is as follows. A couple (I_D, $\frac{g_m}{I_D}$) is chosen. This determines i_f, W_{M_1} [12], C_{gs} and ω_T. With a fixed R_s, L_s is obtained from (5) and L_g from (6). Gain G is calculated using (9) and *NF* using (10) and (11).

IV. DESIGN SPACE EXPLORATION ALGORITHM

The proposed algorithm for designing RF CS-LNA considers the design space defined by the DC bias current I_D of the active transistor M_1 and the $\frac{g_m}{I_D}$ ratio of this transistor. In this design space the current consumption was considered for a given NF and gain of the LNA.

The algorithm is summarized as follows: the design space is covered by a grid of couples ($I_D, \frac{g_m}{I_D}$). For each of these couples, the $NF = NF(I_D, \frac{g_m}{I_D})$ and the gain $G = G(I_D, \frac{g_m}{I_D})$ are obtained.

Having explored the design space, as it is shown in the following example (in the next section), for a given NF, there is a $\frac{g_m}{I_D}$ value that results in an optimum of consumption.

In this algorithm there are also calculated the values of the components L_g and L_s.

A. Inductors constraints

The inductor values are themselves a limitation in the design, as they are on-chip. The limitations, which come from the range of inductors available in the technology and area constraints, determine the feasibility of manufacturing the circuit.

In this design space exploration, only the limitation in the inductor L_g is considered but constraints in L_s can also be added. The former cannot neither be higher than a certain value L_g^{max} nor smaller than L_g^{min}.

As L_g is also obtained from the couple $(I_D, \frac{g_m}{I_D})$, this constraint is added to the design space. It means that now, not all the design space can be used, but only the L_g valid zone .

V. RESULTS AND DISCUSSION

In the following example, maps of NF and gain generated by the algorithm are shown and briefly explained. Using a $0.35\mu m$ CMOS technology and working with the ACM model, the design space of a CS-LNA is generated. We will consider the following design requirements: working frequency $f_0 = 900MHz$, voltage supply $Vdd = 2.5V$, gain higher than 6dB, NF less than 3dB and current I_D less than 7mA. Also the output and input impedance must be 50Ω.

The design space considering only the NF evaluation is shown in Fig. 2. In this graph, we can visualize the existence of a minimum current value for each NF curve. Adding now the gain plot, we chose a possible design point, which is shown in Fig. 3. In Fig. 3 the loci of constant gain correspond to the straight lines of constant $\frac{g_m}{I_D}$. The gain is determined by the transistor f_T, which, given the transistor length, is constant for a given inversion level or equivalently $\frac{g_m}{I_D}$ ratio. Hence constant gain is equivalent to constant $\frac{g_m}{I_D}$ ratio. At this particular point all the design requirements previously mentioned are reached. For the chosen point the obtained transistor is working in moderate inversion, and particularly for this technology it results to be a very wide device, so its layout should be made using a multi-finger technique.

Lets consider now the gate inductor constraints. In Fig. 4, the plot of the L_g valid zone for this technology is marked jointly with the NF curves -the gain curves were taken away for a clearer view-. Our design point previously chosen falls into the zone. It is interesting to highlight that the complete design space exploration takes into account the NF, gain and L_g constraints in the same graph.

In Table I the parameters calculated in Matlab for this particular point of the design are shown.

Analyzing the NF and gain curves, some comments regarding the selection of the inversion level can be made. On one side, small NF forces the transistor to work in strong
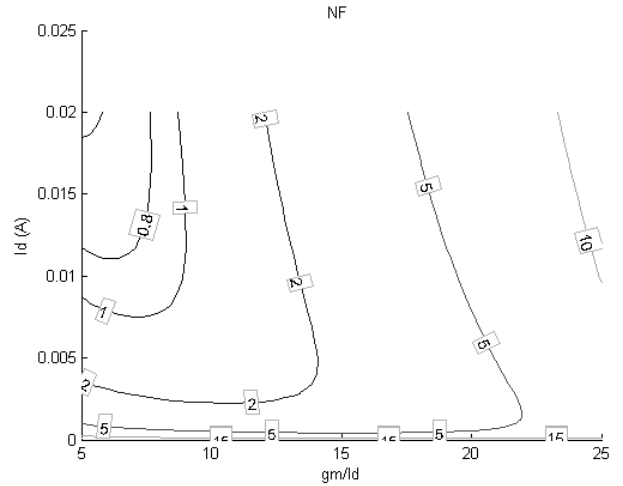

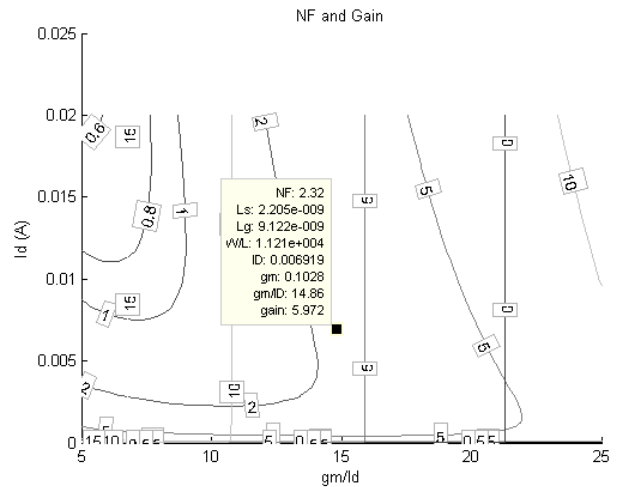Figure 2.   Design space exploration considering only the *NF*

Figure 3.   Design space exploration considering *NF* and Gain. Design point chosen

inversion with higher current consumption. On the other side, if a higher *NF* is permitted in the design, the transistor can work in moderate or even in weak inversion, improving the consumption but decreasing the gain. It is also interesting to note that the small gain values obtained at moderate and weak inversion are because of the technology used. The technology f_T is too close to the operating frequency; this will improve for smaller channel length technologies [13], [14], and hence the gain will improve (see (9))

VI. DESIGN EXAMPLE

This section presents the complete design of the CS-LNA and the simulation results using Spectre-RF for the above selected design point.

To complete the design, the values of L_d, R_d, C_{d1} and C_{d2} were calculated for a 50Ω output load R_L, and are shown in Table II.
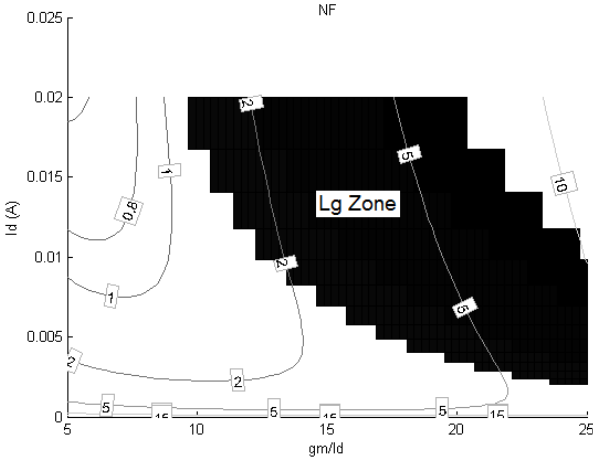
Figure 4. Design space exploration considering *NF* and L_g

Parameter	Calculated in Matlab	Simulated in Cadence
I_D (mA)	6.92	6.5
$\frac{g_m}{I_D}$	14.86	16
g_m (S)	0.103	0.105
NF(dB)	2.32	3.02
G(dB)	5.97	5.7

Table I
PARAMETERS CALCULATED WITH MATLAB AND SIMULATED WITH
SPECTRE-RF

In Table I the values of the simulated NF, gain and I_D, among others, are compared with the ones obtained with the Matlab design exploration. Very good agreement exists between calculated and simulated results.

In Figs. 5, 6, 7 and 8 the S-parameters are shown. Reverse isolation value is good [10], and good output matching was also reached ($Z_{out@900MHz} = (45 + 6j)\Omega$). The input impedance was not as expected, but has a value of $Z_{in@900MHz} = (36 + 17j)\Omega$, what means that the transistor input capacitance value is higher than expected. Also the the simulated *NF* is shown in Fig. 9.

In Fig. 10 is plotted the *IIP3*, which has a simulated value of 6.3dBm.

VII. CONCLUSIONS

This work has presented a design space exploration to design RF CS-LNA's using an all-region CMOS transistor model.

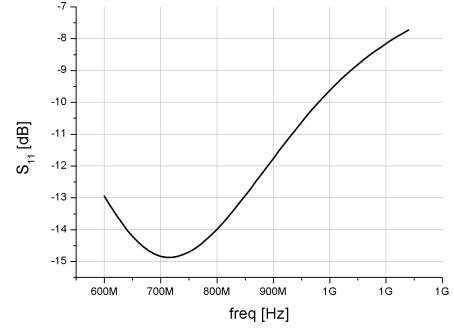| Parameter	Value
W/L	11210
L (μm)	0.35
L_g (nH)	9.12
L_s (nH)	2.205
L_d (nH)	3.5
$R_d(\Omega)$	75
C_{d1} (pF)	20.9
C_{d2} (pF)	10.5

Table II
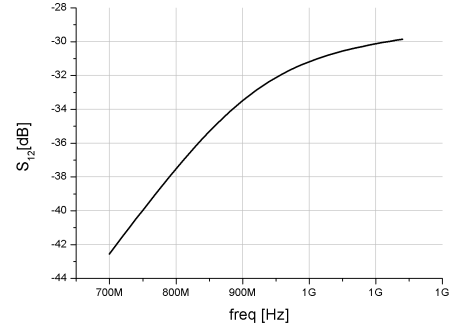DESIGN COMPONENTS

Figure 5. S_{11} parameter
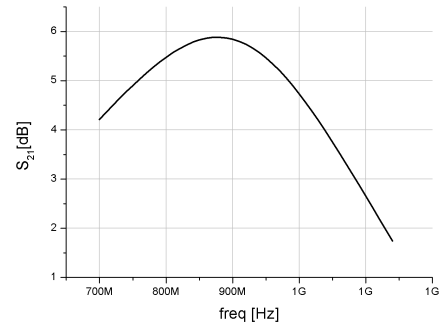

Figure 6. S_{12} parameter
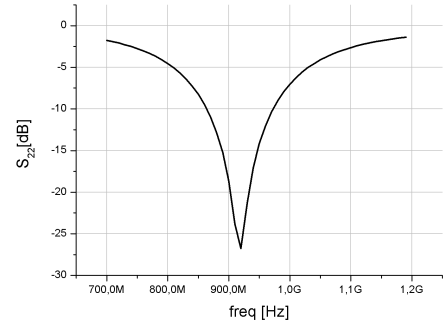

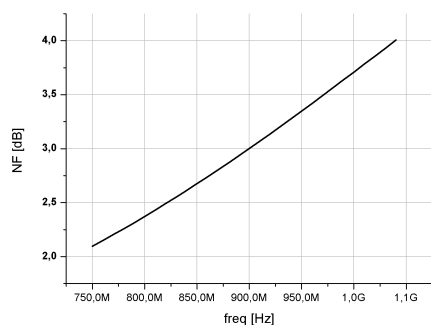Figure 7. S_{21} parameter
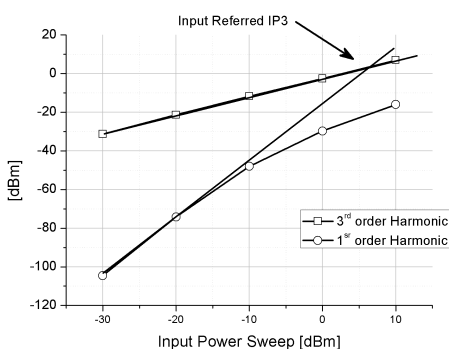

Figure 8. S_{22} parameter

Figure 9. *NF*

Figure 10. *IIP3*

It has been shown how the inversion level affects the NF, the current consumption and the gain. Moreover, it was pointed out the fact that changing the inversion level the trade-off between NF and current consumption can be exploited. Also it has been studied the importance of considering the inductor size constrains in the design space exploration. Finally, an example of a design was considered and very good agreements between the MATLAB calculations and the Spectre-RF were observed.

VIII. ACKNOWLEDGEMENTS

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