# A Control Strategy for Multi-Phase Buck Converters under Dynamical Selection of Active Phases

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***Abstract*—In multi-phase buck converters the efficiency at light load can be substantially improved by deactivating some phases and reducing the switching losses associated. This paper analyzes the perturbations introduced by the phase-enable logic and proposes a correction term to mitigate the effect of the transitions on the output voltage. The strategy proposed is verified using simulations.**

## I. Introduction

In low-voltage, high-current, DC voltage regulation applications the multi-phase buck converter is the industry-standard topology for its numerous advantages in terms of ripple reduction, thermal distribution, efficiency and transient response. Typical applications include voltage regulation for microprocessors, graphics processing units (GPUs) and other complex digital circuits. These applications are characterized by high currents, but also by constant changes in the load current. In particular, during periods of inactivity the digital circuit may reduce drastically the current consumption. At low currents, the efficiency of the multi-phase converter is very poor due to the predominance of switching losses.

It was shown [1], [2] that the efficiency of the multi-phase buck converter can be optimized by reducing the number of active phases at low currents. Using analytical loss models or experimental measurements it is possible to define the efficiency-optimal number of phases as a function of the load current. In these two papers the discussion centered around steady-state operation.

In [3] the strategy of logarithmic current sharing is introduced. Efficiency optimization is achieved both by changing the number of active phases dynamically and by using lower-rated phases at light load with reduced switching losses. The paper addresses possible stability problems due to the change of active phases and introduces hysteresis in the phase-enable logic to avoid limit cycles.

The perturbation generated during the turn-on and turn-off of phases is addressed in [4]. The duty-cycle of each phase is updated for a few PWM periods with a precomputed value until equalization of the phase currents is achieved.

When considering the effect of a change in the number of active phases, it is important to distinguish between two types of perturbations. One is introduced by the load current change that triggers the update in the number of active phases. This perturbation is managed by the feedback loop in the usual way and the design strategies for minimizing the deviation in the output voltage are well-known in the literature. The other type of perturbation is generated by the modification of the number of active phases itself, which is seen by the feedback controller as a change in the plant. This perturbation creates a transient while the controller adjusts its internal states to the new steady-state condition.

The purpose of this paper is to present a control strategy that mitigates the perturbations introduced by a change in the number of active phases during the subsequent period of adjustment of the phase currents and controller states to the new steady-state values.

## II. Modelling

### A. Switched model

An $N$-phase buck converter model is depicted in Fig. 1(a). Each phase is an arrangement of an ideal switch $S$, an ideal diode $D$ and an inductor $L$ with equivalent series resistance $R_L$. These elements are considered identical among phases. The output filter is a capacitor $C$ with equivalent series resistance $R_C$. The input voltage $V_I$ is assumed constant. The independent current source $i_O$ models the load of the converter.

Notice that the model does not include synchronous rectification although typical applications do in order to improve efficiency. The reason is that to completely deactivate a phase, in a synchronous rectification implementation of a multi-phase converter, the low-side MOSFET is commanded emulating a diode. Thus, for simplifying matters, the model of Fig. 1(a) includes diodes (instead of switches) representing the low-side MOSFETs.

The dynamical behavior of each phase is described by a hybrid automata [5] as illustrated in Fig. 1(b). The discrete input variable $\sigma_k$ denotes the command for the switch ($\sigma_k = 0$ for open switch and $\sigma_k = 1$ for closed switch).

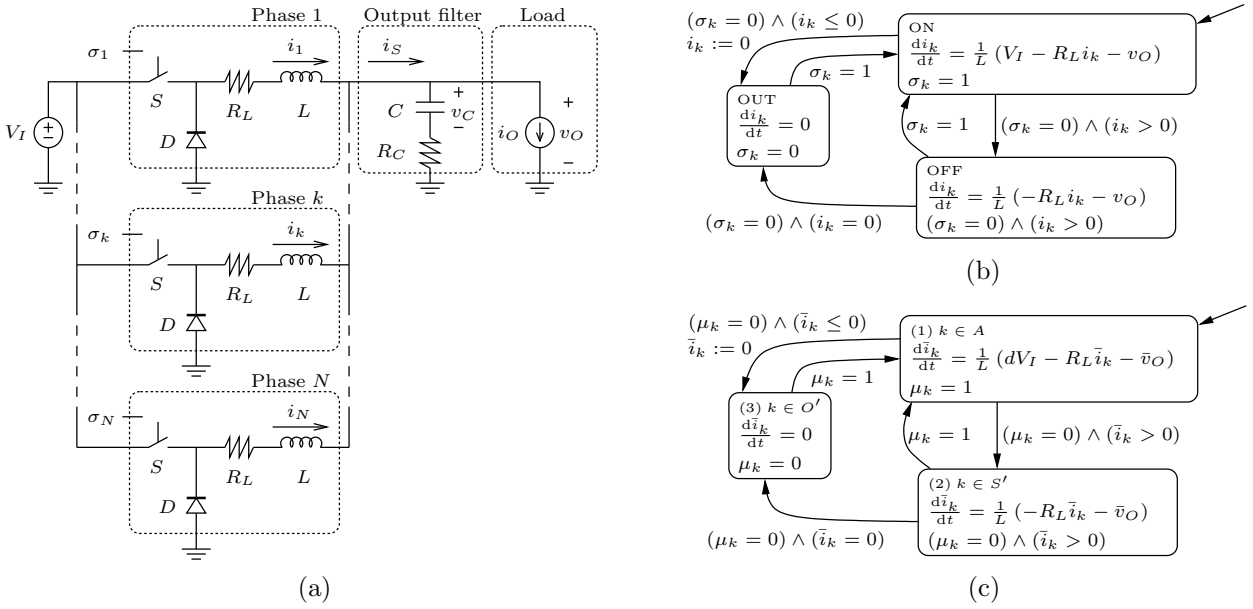


Fig. 1. (a) Model of an $N$-phase buck converter. (b) Each phase $k \in \{1, \ldots, N\}$ modelled as a hybrid automata. (c) Each phase $k \in \{1, \ldots, N\}$ modelled as a hybrid automata after averaging.

The other input is the continuous variable $v_O$. The only continuous state variable is $i_k$ and the discrete states are named: ON, OFF and OUT.

The model is completed with the output stage equations:

$$\frac{\mathrm{d}v_C}{\mathrm{d}t} = \frac{1}{C}\left(i_S - i_O\right) \ , \quad v_O = v_C + R_C\left(i_S - i_O\right) \ ; \quad (1)$$

where $i_S = \sum_{k=1}^{N} i_k$.

The PWM modulator generates $N$ PWM signals $\sigma_1, \ldots, \sigma_N$ that drive the switches. The usual interleaving technique is assumed with the peculiarity that not necessarily all phases need to be simultaneously active. The set of all phases $P = \{1, \ldots, N\}$ is continuously partitioned into two disjoint subsets: the set of active phases $A$ and the set of inactive phases $I = P \setminus A$. The PWM modulator performs the interleaving technique among the phases of the set $A$, with fixed period $T$ and duty cycle $d$; while imposing $\sigma_k = 0 \ \forall k \in I$. It is assumed that, internally, the PWM modulator continuously synthesizes all the possible PWM signals that might be necessary if a sudden asynchronous change in $n$ occurs. It is also assumed that a rotative usage of the phases (as suggested by Fig. 2) is implemented so as to improve the reliability and life of the converter, as proposed in [1].

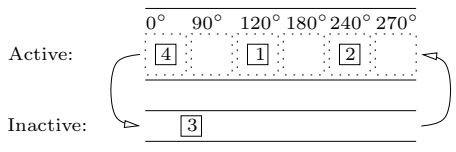


Fig. 2. Rotative usage of the phases in a 4-phase buck converter. Phases are activated and deactivated cyclically as suggested by the circular buffer. The figure illustrates the state in which $n = 3$ phases are active (4, 1 and 2) and one phase is inactive (phase 3). The phase that will be firstly deactivated is assigned 0°, the following is assigned $360°/n$ and so on until the last phase in the active set which is assigned $360°(n-1)/n$.

### *B. Averaged model*

If the number of active phases is selected optimally (regarding efficiency) as a function of the load current, it is reasonable to assume that continuous-conduction mode (CCM) holds for each active phase; so only discrete states ON and OFF of Fig. 1(b) are relevant for any phase $k \in A$. The following differential equation results from averaging between these two states:

$$\frac{\mathrm{d}\bar{i}_k}{\mathrm{d}t} = \frac{1}{L}\left(dV_I - R_L\bar{i}_k - \bar{v}_O\right) \quad \text{for} \quad k \in A \ , \quad (2)$$

where a bar denotes averaging over period $T$, i.e., $\bar{x}(t) = \frac{1}{T}\int_{t-T}^{t} x(\tau)\mathrm{d}\tau$ for any signal $x$.

Among the inactive phases belonging to the set $I$, two disjoint sets are defined: the set $S = \{k \in I : i_k > 0\}$ of phases that "are still" supplying current and the set $O = \{k \in I : i_k = 0\}$ of phases whose current "has extinguished". Clearly, $S \cup O = I$ because for an inactive phase $k$, the switch is open and the diode blocks reverse current; so there is no chance for $i_k$ to be negative. If synchronous rectification is used, when a phase is inactive both switches are open and the situation is the same. By definition, phases belonging to the set $S$, must be on discrete state OFF of Fig. 1(b); and phases belonging to the set $O$, must be on discrete state OUT of Fig. 1(b). Averaging for the phases of these sets yields:

$$\frac{\mathrm{d}\bar{i}_k}{\mathrm{d}t} = \frac{1}{L}\left(-R_L\bar{i}_k - \bar{v}_O\right) \ \forall k \in S \quad \text{and} \quad \frac{\mathrm{d}\bar{i}_k}{\mathrm{d}t} = 0 \ \forall k \in O \ . \quad (3)$$

Defining sets $S' = \{k \in I : \bar{i}_k > 0\}$ and $O' = \{k \in I : \bar{i}_k = 0\}$ related to the sets $S$ and $O$ (but now referring to averaged quantities) and using the previous averaging results (2)–(3), a new model, for each phase of the converter, is built (now under constant-frequency PWM operation). The new model is given by the generic hybrid automata depicted in Fig. 1(c), where the following notation is introduced with reference to the activation and deactivation commands for any phase $k \in P$: $\mu_k = 1\,\forall k \in A$ and $\mu_k = 0\,\forall k \in I$ respectively. A phase $k$ may be active or inactive, depending on which phases are selected as active within the rotative selection scheme, but, at any instant of time, the sum $\sum_{k=1}^{N} \mu_k$ must be equal to $n$, defined as the cardinality $|A|$ of the set $A$. When the phase is active, the continuous input $d$ (duty cycle) drives the temporal evolution of the continuous state variable $\bar{i}_k$. The remaining input is the continuous signal $\bar{v}_O$. The discrete states are named: (1) $k \in A$, (2) $k \in S'$ and (3) $k \in O'$.

The following averaged versions of (1) complete the averaged model:

$$\frac{\mathrm{d}\bar{v}_C}{\mathrm{d}t} = \frac{1}{C}\left(\bar{i}_S - \bar{i}_O\right) \;, \quad \bar{v}_O = \bar{v}_C + R_C\left(\bar{i}_S - \bar{i}_O\right) \;; \tag{4}$$

where $\bar{i}_S = \sum_{k=1}^{N} \bar{i}_k$.

It follows from the definition of $\bar{i}_S$ that:

$$\frac{\mathrm{d}\bar{i}_S}{\mathrm{d}t} = \sum_{k\in A} \frac{\mathrm{d}\bar{i}_k}{\mathrm{d}t} + \sum_{k\in S'} \frac{\mathrm{d}\bar{i}_k}{\mathrm{d}t} + \sum_{k\in O'} \frac{\mathrm{d}\bar{i}_k}{\mathrm{d}t} \;. \tag{5}$$

The time-derivative terms can be substituted from the corresponding expressions in Fig. 1(c), which yields:

$$\frac{\mathrm{d}\bar{i}_S}{\mathrm{d}t} = \frac{1}{L}\left(ndV_I - R_L \sum_{k\in A\cup S'} \bar{i}_k - (n+m')\,\bar{v}_O\right) \;; \tag{6}$$

where $m' = |S'|$. The set $P$ is partitioned into the disjoint sets $A$, $S'$ and $O'$; but since $\bar{i}_k = 0\;\forall k \in O'$ the sum $\sum_{k\in A\cup S'} \bar{i}_k$ is equal to $\bar{i}_S$, so:

$$\frac{\mathrm{d}\bar{i}_S}{\mathrm{d}t} = \frac{1}{L}\left(ndV_I - R_L\bar{i}_S - (n+m')\,\bar{v}_O\right) \;. \tag{7}$$

Taking Laplace transform in (4) and in (7), and operating to eliminate $\bar{v}_C(s)$ and $\bar{i}_S(s)$ yields:

$$\frac{\frac{L}{n}Cs^2 + \left(\frac{R_L}{n} + R_C\right)Cs + 1}{R_CCs + 1}\bar{v}_O(s) + \frac{m'}{n}\bar{v}_O\,(s) = V_I d(s) - \frac{R_L}{n}\left(\frac{L}{R_L}s + 1\right)\bar{i}_O(s) \;. \tag{8}$$

## III. Control

The output voltage $v_O$ is expected to meet certain voltage requirements. Typically, these requirements are given in the form of a reference load line $v_R = V_{LL0} - R_{LL}i_O$ with parameters $V_{LL0} > 0$ and $R_{LL} > 0$. The error $e = v_R - v_O$ should lie inside a tolerance band. Bounds on the load current variability, such as minimum and maximum values ($i_{O,MIN}$ and $i_{O,MAX}$) and maximum slew rate ($SR_{i_O,MAX}$), are usually known.

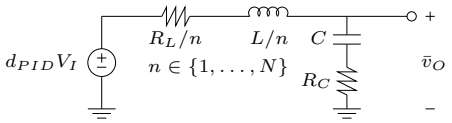


Fig. 3. Family of plants given by (10).

The control architecture used in this work is voltage-mode control (VMC) with a PID controller, but results can be extended to other architectures. Assuming that the duty cycle does not saturate; from (8) follows that it is possible to actively cancel the effect of $\bar{i}_O$ and $m'$ on $\bar{v}_O$, by choosing:

$$d(s) = d_{PID}(s) + \underbrace{\frac{1}{V_I}\frac{R_L}{n}\left(\frac{L}{R_L}s + 1\right)\bar{i}_O(s)}_{d_{FF}(s)} + \underbrace{\frac{1}{V_I}\frac{m'}{n}\bar{v}_O(s)}_{d_{PDTC}(s)} \;, \tag{9}$$

where the first term is left unspecified for the moment. Direct substitution of (9) in (8), verifies the aforementioned cancellation effect:

$$\frac{\bar{v}_O}{d_{PID}}\,(s) = \frac{R_CCs + 1}{\frac{L}{n}Cs^2 + \left(\frac{R_L}{n} + R_C\right)Cs + 1}V_I \;. \tag{10}$$

The second term in (9) is nothing but a standard feed-forward (FF) action of the load current [6] that masks the effect of the load current on the output voltage. The third term in (9), is the main contribution of this paper and will be referred to as phase deactivation transient compensation (PDTC). It is different from zero only during the short transients that take place after one or more phases are deactivated, compensating the dynamics. The unspecified first term $d_{PID}(s)$ in (9) is the PID control action provided by the feedback controller, that only needs to be appropriately and robustly tuned for the family of rather simple plants given by (10) $\forall n \in P$ (which can be electrically interpreted as depicted in Fig. 3). Alternatively, $d_{PID}(s)$ may be the control action of a PID controller dynamically selected from a family of $N$ finely tuned controllers, one for each possible plant.

Although the proposed control strategy is based on the averaged model, it is reasonable to expect similar cancellation effects when applied to the switched model.

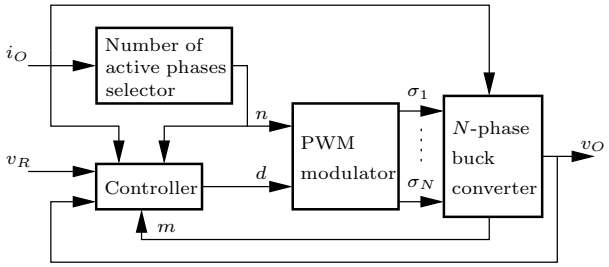


Fig. 4. Block diagram of the whole proposed system.

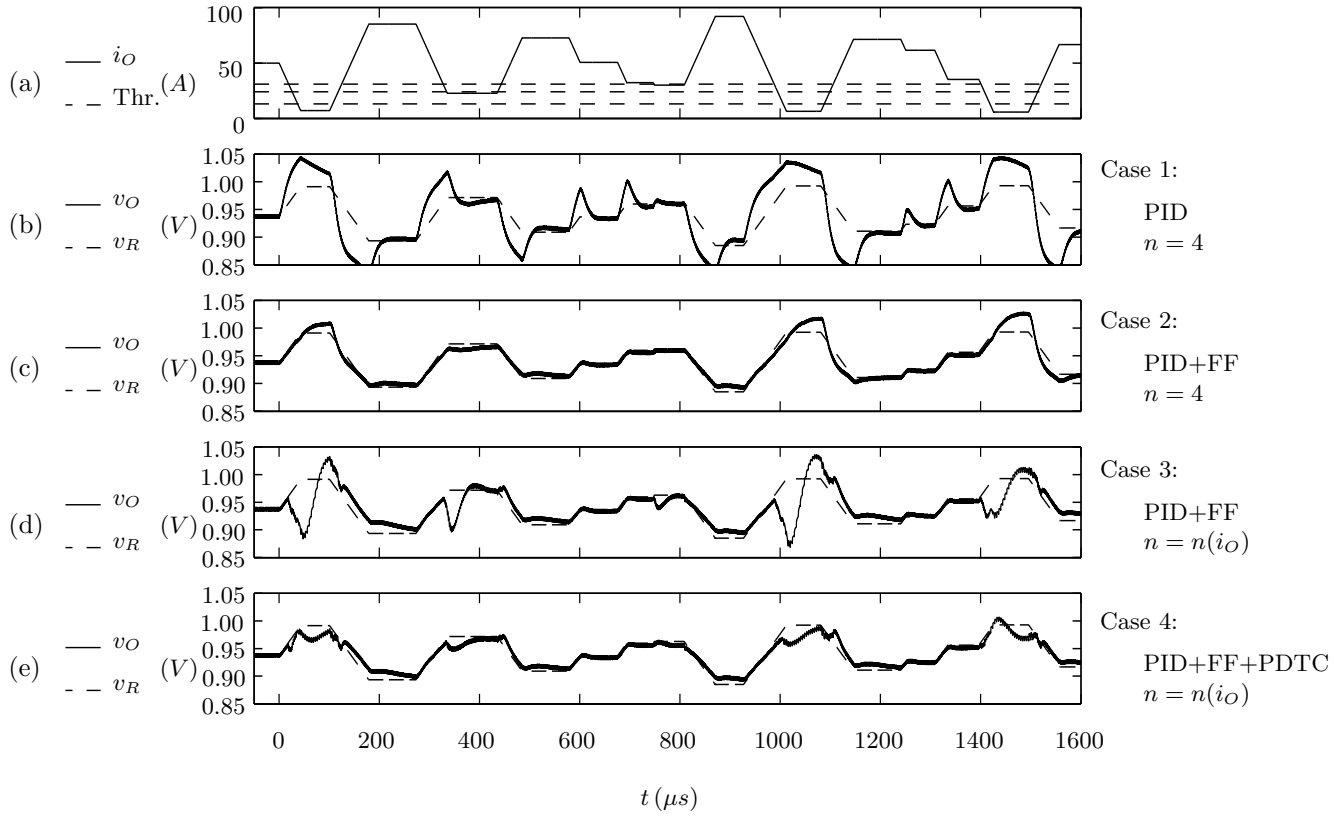


Fig. 5. Simulation results. (a) Random load current and thresholds that define the selection map $n = n(i_O)$. In the remaining subfigures, the output and reference voltages are plotted for the following cases. (b) PID and $n = 4$ independent of $i_O$. (c) PID plus FF and $n = 4$ independent of $i_O$. (d) PID plus FF and $n = n(i_O)$. (e) PID plus FF plus PDTC and $n = n(i_O)$.

TABLE I
CLOSED-LOOP SIMULATION RESULTS

| Case | Control strategy | | Number of active phases | Subfigure in Fig. 5 | $(v_R - v_O)_{RMS}$ (mV) | Average number of switchings per $\mu s$ |
|---|---|---|---|---|---|---|
| 1 | PID: | $d = d_{PID}$ | $n = 4$ | (b) | 36.31 | 2.000 |
| 2 | PID+FF: | $d = d_{PID} + d_{FF}$ | $n = 4$ | (c) | 10.14 | 2.000 |
| 3 | PID+FF: | $d = d_{PID} + d_{FF}$ | $n = n(i_O)$ | (d) | 25.96 | 1.641 |
| 4 | PID+FF+PDTC: | $d = d_{PID} + d_{FF} + d_{PDTC}$ | $n = n(i_O)$ | (e) | 10.82 | 1.640 |

In this case, the proposed control strategy (9) should be interpreted with non-averaged signals and with $m'$ substituted by $m = |S|$. A block diagram of the whole proposed system is depicted in Fig. 4. Note that it is not necessary to precisely measure each phase current to compute $m$, all that is needed is to keep track of how many of the inactive phases are conducting current. One possible practical mean to monitor $m$ would be to measure the switching node voltage of each phase during the OFF-time, and detect whether it is below the diode's threshold voltage or not.

## IV. RESULTS

Closed-loop simulation results, using the switched model for a 4-phase converter, are shown in Fig. 5 and Table I. Representative parameter values [1] were chosen and a random load current signal was constructed within typical specifications [2]. Four cases, detailed in Table I, were simulated for the same load current signal. In cases 3 and 4 a static selection map $n = n(i_O)$ for selection of the number of active phases is used with the thresholds indicated in Fig. 5(a) located at $13\,A$, $24\,A$ and $31\,A$, defining the boundaries between $n = 1$ and $n = 2$, 2 and 3, and 3 and 4 respectively. For each strategy, the same PID algorithm [3] was used. Its parameters were robustly

[1] $N = 4$, $T = 4\,\mu s$, $C = 1\,mF$, $R_C = 1.65\,m\Omega$, $L = 800\,nH$, $R_L = 10\,m\Omega$, $V_I = 12\,V$, $V_{LL0} = 1\,V$ and $R_{LL} = 1.25\,m\Omega$.

[2] $i_{O,MIN} = 5\,A$, $i_{O,MAX} = 100\,A$ and $SR_{i_O,MAX} = 1\,A/\mu s$.

[3] $d_{PID}(s) = K\left(1 + \frac{1}{T_I s} + \frac{T_D s}{\frac{T_D}{N_D}s+1}\right)e(s)$ where $K = 0.251\,V^{-1}$, $T_I = 67.4\,\mu s$, $T_D = 14.1\,\mu s$ and $N_D = 8.52$.

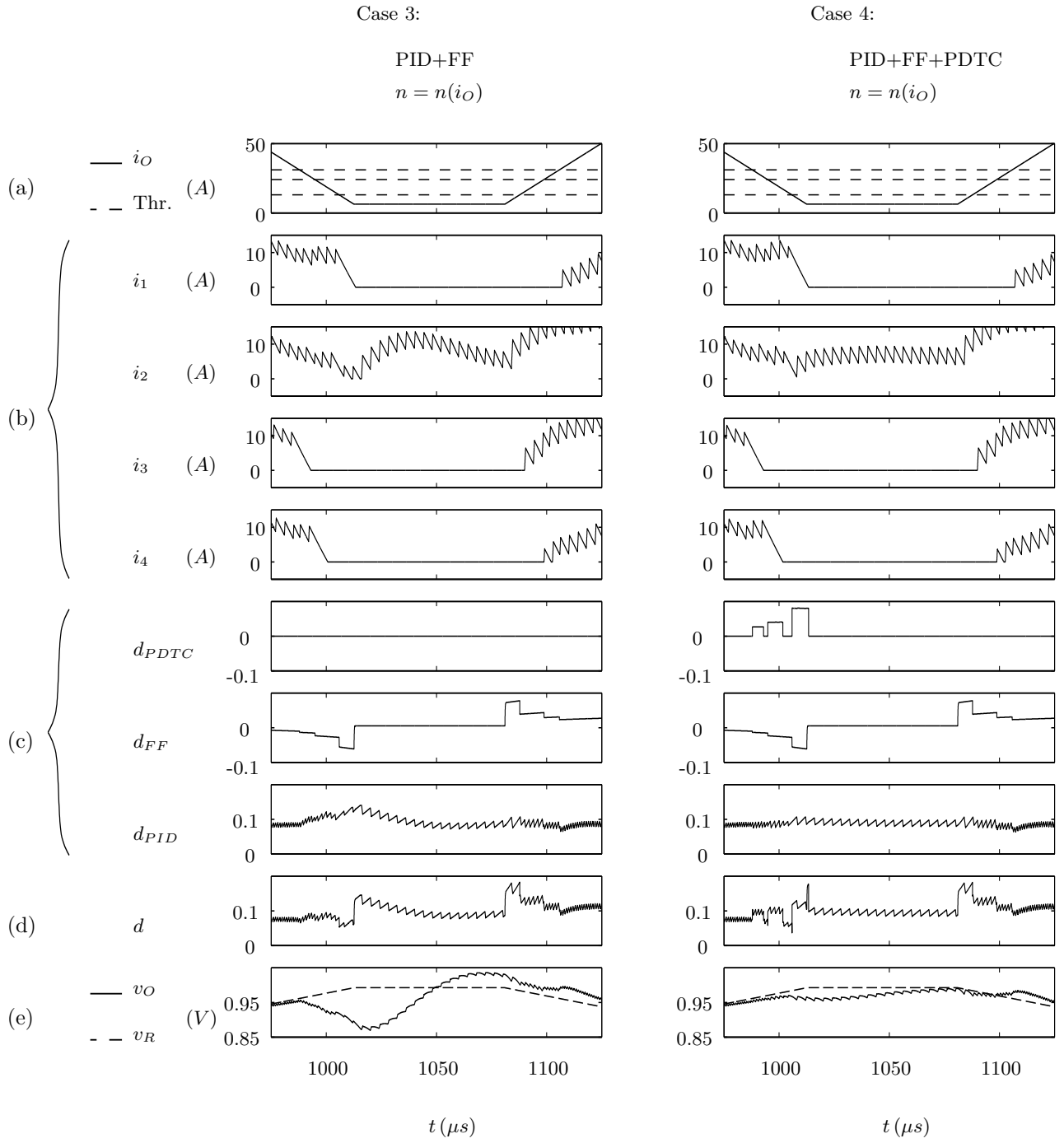


Fig. 6. Comparison of cases 3 and 4 of Fig. 5 during time interval: $[975, 1125]\,\mu s$. (a) Load current and thresholds that define the selection map $n = n(i_O)$ (the same for both cases). (b) Phase currents. (c) Duty cycle components: $d_{PID}$, $d_{FF}$ and $d_{PDTC}$. Obviously, for case 3: $d_{PDTC} = 0\,\forall t$. (d) Duty cycle: $d = d_{PID} + d_{FF} + d_{PDTC}$. (e) Output and reference voltages.

tuned to achieve a maximum gain crossover frequency equal to $41.2\,kHz$ (for the case $n = 4$) and a minimum phase margin equal to $59.7^\circ$ (for the case $n = 1$).

Notice that dynamical selection of the number of active phases diminishes the average number of switchings per $\mu s$ (consequently reducing switching losses), but voltage regulation performance deteriorates. PDTC mitigates this undesirable effect, almost restoring the performance that is obtained when all phases are constantly active.

In Fig. 6, cases 3 and 4 of Fig. 5 are compared during a time interval when three phases are deactivated and activated again. Notice the subtle difference in signal $d$ between the two cases during deactivation and how this results in better voltage regulation for case 4.

## V. Conclusions

The mitigation of perturbations introduced by changes in the number of active phases in a multi-phase buck converter is addressed. It is shown that a simple additive correction to the duty-cycle command can substantially reduce the dynamical effect of the phase-enable logic. Although a VMC control architecture is used, the design methodology can be equally applied to other architectures like the different versions of current-mode control (CMC) found in commercial controller chips.

These results facilitate the introduction of a higher-level phase-enable logic to improve the efficiency of the converter at light load without introducing substantial performance deterioration due to the dynamic selection of the number of active phases.

Future work includes experimental verification of the control method proposed and analysis of the effect of component tolerances.

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