# Phase noise - consumption trade-off in low power RF-LC-VCO design in micro and nanometric technologies

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## ABSTRACT

An LC-VCO design optimization, based on the $g_m/I_D$ methodology, is presented throughout this work, highlighting how, by applying all regions of inversion of the MOS transistor, the trade-off between phase noise and current consumption can be optimized for the application. Both transistor compact model equations and transistor data acquired from simulation are used to obtain $g_m/I_D$ curves as well as normalized capacitances. Influence of tank elements' characteristics in the VCO performance is also discussed. Results of applying the methodology in the design of two VCOs in 0.35$\mu$m and 90nm CMOS processes are described. Measurement results for the 915MHz VCO designed in 0.35$\mu$m CMOS technology are also presented, obtaining a current consumption of 3mA with a phase noise ($\mathcal{L}$) of $-107dBc/Hz$ @$1MHz$. The 2.4GHz VCO designed in a 90nm radiofrequency technology shows a current consumption of 400$\mu A$ with a $\mathcal{L}$ of $-111.4dBc/Hz$ @$600kHz$.

## Categories and Subject Descriptors

B.7.1 [**Hardware**]: Integrated Circuits

## General Terms

Design, Algorithms, Theory, Performance

## Keywords

Radio-frequency, VCO, Power consumption, Design methodology

## 1. INTRODUCTION

VCOs are responsible for a significant part of power consumption in integrated circuits for wireless systems. Therefore, in low power radiofrequency chips it is important to exploit the consumption - spectral purity (phase noise) trade-off in order to spend just the current necessary to fulfil the application requirements. In this work we present an LC-voltage controlled oscillator (VCO) design optimization based on the $g_m/I_D$ methodology [1]. The idea is to study the VCO design space and to choose the optimum design, considering current consumption $I_D$ and phase noise $\mathcal{L}$ both as functions of $g_m/I_D$ -an intrinsic transistor characteristic, related to the inversion level and with a small variation range-. Following this methodology we obtain circuits with low current consumption without jeopardizing $\mathcal{L}$.

There is a direct mapping between $g_m/I_D$ values and the inversion regions. In the CMOS technologies used in this work, at room temperature, weak (WI) and strong (SI) inversion correspond approximately to $g_m/I_D$ values of more than $18V^{-1}$ and less than $8V^{-1}$, respectively; moderate inversion (MI) is amid them. We exploit the feasibility of designing RF transistors in MI and WI; a fact that has been well proven in several works [2] [3] [4]. There exist previous works on VCOs working in subthreshold region [5] [6], but designs trade-offs have not been systematically explored in them. Therefore, it is our aim to present here an in-depth description of this optimization approach valid both for micro and nanometer technologies.

Validation of the design optimization is done by the design of two VCOs. One is implemented in a 4-metal, 0.35$\mu$m CMOS technology with oscillation frequency for the 915MHz ISM band. The other, designed in a 7-metal, 90nm CMOS technology, works in the 2.4GHz band. Measurements of the 915MHz-VCO and SpectreRF simulations of the 2.4GHz VCO (which at the moment of this work is under test), show very good results, specially the latter which achieves both very low current consumption and good phase noise values.

Here we also discuss briefly a fundamental matter in VCO design optimization: tank components' characteristics. It is well known that LC-VCO performance is strongly dependent on its tank components -inductors and varactors-, specially their quality factors. Lossy components mean higher current consumption as the oscillation condition imposes a higher transconductance as tank resistance increases. In micrometer technologies we got used to have on-chip inductors with very bad quality factors; then inductor losses dominated in the tank losses. In nanometric technologies -specially the ones focused to RF-, the inductors' quality factor has improved considerably. Then, varactors losses could become comparable to inductor ones. This change in the design ap-

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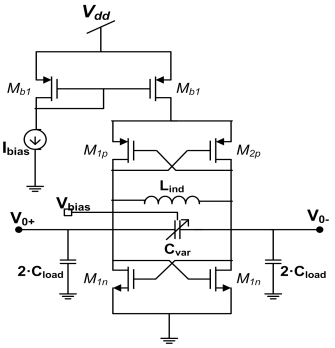



**Figure 1: Cross-coupled pair LC-VCO architecture used.**

proach must be also taken into account in the optimization.

This paper is laid out as follows. In Section 2 we discuss the LC-VCO topology used, the VCO operation and the relation between $\mathcal{L}$, $I_D$ and $g_m/I_D$. In Section 3 we expose the design methodology based on $g_m/I_D$; covering the parameters involved, studying two $g_m/I_D$-curve acquisition methods, and discussing the involved trade-offs. In Section 4 the two previously mentioned designs are presented as well as the corresponding measurements of the 915MHz-VCO. Finally Section 5 presents the main conclusions of this work.

# 2. CIRCUIT DESIGN

## 2.1 Topology

The LC-VCO architecture with two cross-coupled pair pMOS and nMOS transistors blocks shown in Fig. 1, was chosen for this work. Basically the cross-coupled blocks generate a negative resistance between its transistors' drains that cancels the tank parasitic resistance, making the oscillation maintains itself after it starts. A pMOS current source is chosen as it has smaller flicker noise values than a n-MOS one with equal transconductance, meaning less contribution to the VCO phase noise [7].

## 2.2 VCO operation

Let's describe briefly the LC-VCO behaviour by means of a simple set of equations. These equations are valid for the topology used in this work but with minor changes, they can be adjusted to other LC-VCO circuits. Later on we will use these equations to explain the methodology.

The VCO oscillates when tank losses are cancelled by an equivalent negative conductance $G$, related to pMOS and nMOS transistors conductances $g_{m,p}$ and $g_{m,n}$ by (1). To simplify the design methodology we consider both values $g_{m,p}$ and $g_{m,n}$ equal to each other; naming this value $g_m$.

$$G = -\Big(\frac{g_{m,p}}{2} + \frac{g_{m,n}}{2}\Big) \equiv -g_m \tag{1}$$

In this case, the VCO starting condition is

$$g_m = \alpha \cdot g_{tank} = \alpha \cdot (g_{var} + g_L + g_{ds,n} + g_{ds,p}) \tag{2}$$

where $g_{tank}$ is the tank equivalent conductance; $g_{var}$ and $g_L$ are the varactor and inductor parasitic conductances , and $g_{ds,n}$ and $g_{ds,p}$ are the transistors output conductances. The oscillation factor $\alpha$, with $\alpha > 1$, usually around 3, is included to guarantee the oscillation.

The oscillation frequency $f_0$ is

$$f_0 = \frac{1}{2\pi\sqrt{L_{tank} \cdot C_{tank}}} \tag{3}$$

where $L_{tank}$ can be approximated by $L_{ind}$ and $C_{tank}$ is

$$C_{tank} = C_{var} + C_{eq,p} + C_{eq,n} + C_{ind} + C_{load} \tag{4}$$

where $C_{eq,p}$ and $C_{eq,n}$ are the pMOS and nMOS equivalent capacitances, $C_{ind}$ the inductor equivalent parasitic capacitance , $C_{var}$ the varactor capacitance and $C_{load}$ the output load capacitance.

## 2.3 Phase Noise as a function of $g_m/I_D$ and $I_D$

LC-VCO phase noise has been studied extensively [8] [9] and several models exists to describe its behaviour. Here we apply the Linear Time Variant model (LTV) proposed by [9], as it proves to be both accurate and easy to use for LC-VCOs.

In terms of $g_m/I_D$ and $I_D$ the corresponding $1/f^2$ phase noise zone is, considering only the white noise sources of cross coupled transistors,

$$\mathcal{L}(\Delta\omega) = \left(\gamma k_B T \Big(\frac{\pi}{8}\Big)^2 \frac{1}{Q^2} \Big(\frac{g_m/I_D}{I_D}\Big) \Big(\frac{\omega_0}{\Delta\omega}\Big)^2\right) \tag{5}$$

where $\gamma$ is the white noise factor, $k_B$ is the Boltzmann constant, $T$ is the room temperature, Q is the tank quality factor, $\omega_0$ is the carrier oscillation frequency and$\Delta\ \omega$ is the offset frequency from that carrier.

For the transistors flicker noise the $1/f^3$ phase noise zone is:

$$\mathcal{L}(\Delta\omega) = \left(\frac{K_F}{8}\Big(\frac{\pi}{8}\Big)^2 \frac{1}{Q^2 \cdot L}\Big(\frac{1}{W_n} + \frac{1}{W_p}\Big)\Big(\frac{g_m}{I_D}\Big)^2\Big(\frac{\omega_0^2}{\Delta\omega^3}\Big)\right) \tag{6}$$

where $K_F$ is a flicker noise model constant. The examples studied in this work do not show the effect of flicker noise at the offset frequencies studied. However, in other possible designs, the influence of this zone has to be considered. Also, other effects -i.e. variations in transistor output conductance, bias noise- have to be included in the future to improve the methodology results.

Increasing $g_m/I_D$, i.e. moving to WI, decreases consumption, since $g_m$ is fixed by (2). On the other hand, (5) shows that regarding phase noise, increasing $g_m/I_D$, increases phase noise. It is clear that increasing $g_m/I_D$, i.e. moving to WI, while decreases consumption, also increases phase noise; for the $1/f^2$ zone this can be compensated by a rise in the current. These trade-offs are the ones that this work contributes to explore, making it possible to optimize consumption while achieving the required phase noise level.

# 3. PROPOSED LC-VCO DESIGN METHODOLOGY.

The design methodology presented here can be used in any LC-VCO topology. To give a proof of concept we continue using the circuit of Fig. 1.

## 3.1 Components' parameters included in the design flow

The components' parameters to be used in the design flow are: (i) inductance value $L_{ind}$ and its parasitics; (ii) varactor capacitance $C_{var}$ and parasitic resistance and (iii) cross-coupled pMOS and nMOS widths $W$ (the length $L$ used is the minimum imposed by the technology to increase transistors' $f_T$).

The proposed methodology is based on the MOS parameters' description in terms of the $g_m/I_D$ ratio [1]. Particularly for the saturated transistor this ratio can be expressed in terms of the inversion level $i = I_D/I_S$ [10], with $I_S$ the normalization current proportional to the aspect ratio $W/L$, the slope factor $n$, the mobility $\mu$ and the gate capacitance $C_{ox}$. Next subsection presents the acquisition of the $g_m/I_D$ vs $i$ curve.

Besides the MOS characteristics, the technology back-end establishes the varactor behaviour, i.e. (i) capacitive curve versus bias voltage -fixing the VCO gain $K_{VCO}$ ($K_{VCO} = f_0/V_{bias}$)-, (ii) quality factor $Q_{var}$, (iii) capacitive and resistive losses.

On the other hand, technology front-end fixes the inductor characteristics: (i) value $L_{ind}$, (ii) quality factor $Q_{ind}$ and (iii) resistive and capacitance losses.

## 3.2 Acquisition of $g_m/I_D$ vs $i$ curves

$g_m/I_D$ vs $i$ is an universal characteristic curve for any long channel MOS. When short (or narrow) channel effects become significant, this curve depends slightly on the transistor $W$ and $L$ and its mobility $\mu$ as well as on parameters of the particular process. This means that to achieve an improved fitting, depending on the expected MOS dimensions (particularly its length) we have to use, in accordance, a $g_m/I_D$ curve generated with similar MOS dimensions.

In this work we implement two ways of obtaining the $g_m/I_D$ versus $i$ curves. Depending on the particular application and technology data available, one or the other can be used. In Section 4 each method is implemented and their pros and cons discussed.

*By Compact Model equations*

Compact models like ACM [10] or EKV [11] give us long-channel MOS simple equations which relate the inversion coefficient $i$ with the MOS transconductance $g_m$ and its various capacitances among others. The $g_m/I_D$ curve can be easily obtained only by fitting the slope factor $n$ with data available by measurement or by simulation.

However, for short channel transistors, long-channel equations are no longer valid, and should be changed by others containing short channel effects. In this situation more parameters, as those related to threshold voltage dependence on length, mobility degradation and velocity saturation, should be fitted.

*By Simulation*

Electrical simulation might be used to extract $g_m/I_D$ and capacitances curves versus $i$. A way of performing this is by using the circuit of Fig. 2 and obtaining its operation point for a set of gate voltages $V_G$ (swept between 0V and supply voltage $V_{DD}$) and a drain voltage $V_D$ -fixed approximately around its expected value in the VCO application-. As the MOS characteristics depend slightly on $W$ and $L$, width and length of the $M_1$ transistor should be in the expected design range. Thereafter, it is immediate to obtain $i$, $g_m/I_D$ and the normalized capacitances.

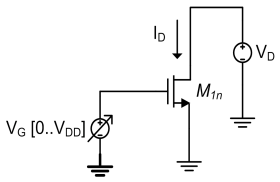



**Figure 2: Test circuit for acquiring $g_m/I_D$ and capacitance curves.**

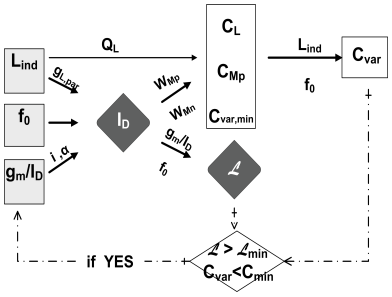



**Figure 3: Proposed $g_m/I_D$ design methodology**

Particularly for the 2.4GHz VCO design, instead of calculating $i$ we plot $g_m/I_D$ versus $I_D/(W/L)$, with minimum $L$. Doing this avoids us to fit parameters such as mobility and slope factor, which are affected by short channel effects in this technology.

## 3.3 Methodology

To clarify the following discussion we utilize the methodology scheme of Fig. 3.

Let's begin our explanation by choosing the carrier frequency $f_0$ and a pair $(g_m/I_D, L_{ind})$, -with $L_{ind}$ included in the inductor's available range-.

From each pair $(g_m/I_D, L_{ind})$ we calculate $I_D$ using the VCO oscillating condition given by (2), as $g_m$ is fixed by $g_L$. Other conductances are discarded to simplify the explanation; however output MOS and varactor conductances are included in the complete methodology.

From the $g_m/I_D$ versus $i$ (or versus $I_D/(W/L)$) curves of pMOS and nMOS transistors, -considering minimum technology transistor length $L$-, we calculate pMOS and nMOS widths $W_{Mp}$ and $W_{Mn}$ and their equivalent parasitic capacitances $C_{Mp}$ and $C_{Mn}$. Then, $C_{var}$ is obtained from (3) and (4). Oscillator phase noise is computed using (5) and (6).

Whether the current consumption or the phase noise are higher than the specifications; or whether the varactor capacitance is lower than a certain $C_{var,min}$ -imposed by technology and the desired VCO frequency range-, another pair $(g_m/I_D, L_{ind})$ should be picked up. The following relations can be represented as level curves with a Matlab routine: $(g_m/I_D, L_{ind})$ vs $I_D$; $(g_m/I_D, L_{ind})$ vs $\mathcal{L}$ and $(g_m/I_D, L_{ind})$ vs $C_{var}$. One example of these level curves for the 0.35$\mu$m VCO is depicted in Fig. 4; where phase noise is plotted versus $g_m/I_D$ for various inductor values.

# 4. DESIGN EXAMPLES

The $g_m/I_D$ methodology makes us possible to play with some VCO variables and find an optimum design point, which might achieves -or not- the initial specifications and

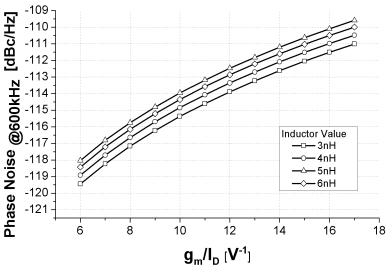



**Figure 4: 915MHz VCO Phase Noise versus $g_m/I_D$.**

restrictions, depending on the technology.

It is expected to obtain this optimum in the MI region. In strong inversion $\mathcal{L}$ is reduced and $C_{var}$ risen, but these advantages are counteracted by a considerable increase in $I_D$. Exactly the opposite happens in weak inversion, where a substantial reduction of $I_D$ is opposed to a growth in $\mathcal{L}$ and transistor widths -the latter is equivalent to very small or even negative $C_{var}$-. Working in MI, small currents can be obtained without jeopardizing $\mathcal{L}$ or $K_{VCO}$. In the following examples this fact will be quite evident.

Therefore, the purpose of this section is to show the application of the proposed design optimization methodology to two CMOS cross-coupled VCOs' implementations. These oscillators were designed for the IEEE802.15.4 915MHz and 2.4GHz bands.

## 4.1 915MHz LC-VCO @ 0.35$\mu$m technology

In this example the $0.35\mu m$ minimum transistor length makes us possible to use the ACM model for quasi-static (QS) long-channel CMOS transistors. For 915MHz it is possible to design in this technology transistors with a $g_m/I_D$ up to 15 [3], considering $f_T/10$ as a QS frequency limit [12].

This technology does not have varactor cells, thus these components were designed using a MOS capacitor in the inversion zone. Monolithic inductors were designed in the uppermost metal layer. However they do not achieve quality factors higher than 3 or 4. Hence, from (2), the high parallel inductor resistance obtained leads to high MOS transconductances values , which directly stands for high current consumption. It leads us to design the MOS with a $g_m/I_D = 11$, which is near the lower limits of MI in this technology.

Transistor and inductor sizes of the final design obtained with a MATLAB routine are shown in Table 1. The inductor parasitics were obtained with ASITIC [13]. Phase Noise computed in the routine at 600kHz from the carrier was $\mathcal{L} = -113.2$dBc/Hz.

| Parameter | Value | Parameter | Value |
|---|---|---|---|
| L | 5nH | $R_{L,par}$ | 90Ω |
| $C_{L,eq}$ | $90fF$ | $C_{load}$ | 600fF |
| $I_{bias}$ | $3mA$ | $g_m$ | $30mS$ |
| $C_{var}$ | $700fF$ | $W_{var}$ | $1600\mu m$ |
| $W_n$ | $336\mu m$ | $W_p$ | $782\mu m$ |

**Table 1: 0.35$\mu m$, 915MHz VCO components and bias current final values.**

*Simulation*

The VCO of Table 1 was simulated in Cadence SpectreRF Tool using the BSIM3v3 [14] model provided by the foundry. The inductor model used in the SpectreRF simulations was obtained with the SpectreRF Spiral Inductor Modeler Tool[1] . Simulated phase noise with a 915MHz carrier at a 600kHz-offset was $\mathcal{L} = -121$dBc/Hz.

*Measurements*

The VCO spectral density measurements were done employing the $HP8546$ EMI Receiver with an encapsulated chip. Its 939MHz-centered spectrum is shown in Fig. 5a. Table 2 lists a set of three phase noise experimental data at a carrier offset of 600kHz.

$K_{VCO}$ measurements were also performed; a comparison between them and SpectreRF simulations are given in Table 3 and in Fig. 5b.

Table 4 shows a comparison of this work with others working at similar frequency range. Considering the poor quality factor of the inductors, the technology used in this work and the fact that the phase noise was measured off-chip, the obtained results are interesting.

| Carrier offset $\Delta f$ | Measured L[dBc/Hz] |
|---|---|
| 100kHz | -87 |
| 600kHz | -102 |
| 1MHz | -107 |

**Table 2: Phase noise measured @ $V_{DD} = 3V$, $I_{bias} = 3mA$ and $V_{bias} = 1V$**

| | $K_{VCO}$ | Freq. range | Tuning |
|---|---|---|---|
| Simulated | -169MHz/V | 945MHz-850MHz | 11% |
| Measured | -214MHz/V | 937MHz-810MHz | 15% |

**Table 3: Simulated and measured $K_{VCO}$.**

| Ref. | Techno | $f_0$[GHz] | $\mathcal{L}$[dBc/Hz] | $I_{bias}$[mA] | $Q_{ind}$ |
|---|---|---|---|---|---|
| [15] | 0.25$\mu$m | 1.25 | $-127_{@0.6MHz}$ | 3.6 | 10 |
| [16] | 0.25$\mu$m | 1 | $-129_{@1MHz}$ | 3.3 | - |
| [17] | 0.18$\mu$m | 0.76-1 | $-120_{@1MHz}$ | 5 | - |
| (*) | 0.35$\mu$m | 0.94 | $-107_{@1MHz}$ | 3 | $\simeq$3 |

**Table 4: Comparison among our 915MHz VCO -marked with (*)- and previous published works.**

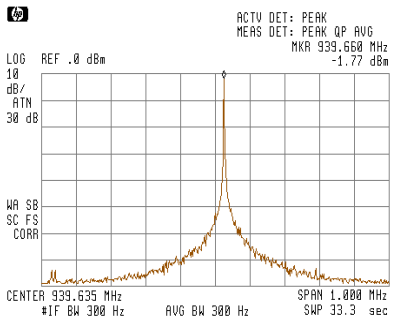
## 4.2 2.4GHz LC-VCO @ 90nm technology

Our aim in this design was to obtain an LC-VCO with both very-low-power and low phase noise in a nanometer technology. We decided to work with the $g_m/I_D$ and capacitances curves obtained by simulation. The circuit is in fabrication at the date of this work.

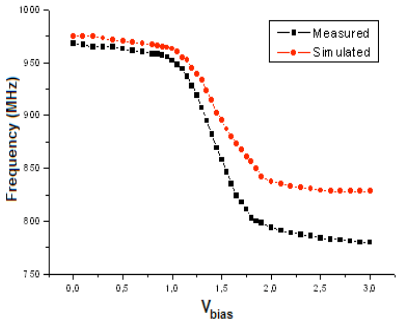
The 7-metal stack layer allows the design of very high inductor quality factors Q (up to 20), which lead to a wider $g_m$ range, compared with the $0.35\mu m$ LC-VCO. Moreover, 90nm transistors have considerably high $f_T$ values to allow us working towards WI region while neglecting non-quasistatic effects. The varactor $C_{var}$ was implemented with two *ncap* varactors - an nMOS in N-well- connected in series.

Again, using a MATLAB routine, we obtain the corresponding level curves to choose the operation point. As an

[1]The inductor model obtained from the SpectreRF Tool is more complete than the one obtained by ASITIC. However we use ASITIC in the methodology as it straightaway gives us the inductor Π model.




(a) Spectrum




(b) $K_{VCO}$

**Figure 5: 915MHz VCO measurements.**

example, in Fig. 6, for two inductor values -the value finally used and a smaller one- it is plotted the capacitance of each *ncap* versus $g_m/I_D$ and the $C_{var,min}$ below which the design is not valid. Also, for the same inductors, in Fig 7 it is depicted the phase noise versus $g_m/I_D$ ($I_D$ is hence fixed for each case). This figure shows that changing the $g_m/I_D$ (inversion level) lets us to tune the phase noise vs. consumption trade-off, implying significant changes in consumption. It also clearly shows that a higher inductor reduces the consumption but increases the phase noise.

With the MATLAB routine, it was possible to choose a design point in the upper MI region with a $g_m/I_D$ of 17.5; with a current $I_D$ of $380\mu A$ for a $\mathcal{L}$ of $-111.2dBc/Hz_{@600kHz}$ from the carrier. Both current and phase noise are very low. The final VCO parameter values finally implemented are listed in Table 5

*Simulation*

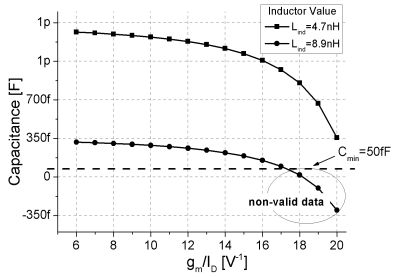



**Figure 6: Varactor capacitance as a function of $g_m/I_D$ for two inductor values.**

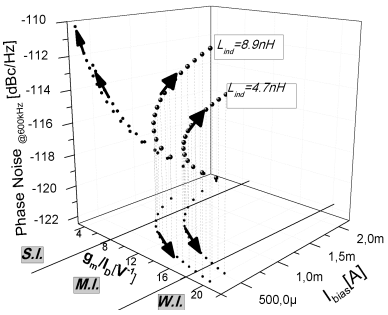



**Figure 7: Phase noise versus $g_m/I_D$ for the 2.4GHz VCO for two inductor values ($I_D$ gets fixed).**

| Parameter | Value | Parameter | Value |
|---|---|---|---|
| $V_{DD}$ | 1.2V | $I_{bias}(=2I_D)$ | $400\mu A$ |
| L | $8.9nH((290\mu m)^2)$ | $C_{L,eq}$ | $75fF$ |
| $R_{L,par}$ | $\simeq 400\Omega$ | $g_m$ | $2.6mS$ |
| $C_{var,min}$ | $50fF$ | $C_{Load}$ | $0F$ |
| $W_{nMOS}/L$ | $10 \times 5\mu m/100nm$ | $W_{pMOS}/L$ | $10 \times 5.1\mu m/100nm$ |

**Table 5: 90nm, 2.4GHz VCO components and bias current final values.**

The performance evaluation of this VCO was done with the SpectreRF tool using the BSIM4 [14] transistor model. With the VCO oscillating at 2.35GHz[2], its phase noise at 600kHz from the carrier has a value of $\mathcal{L} = -111dBc/Hz$, very near to the MATLAB result.

Table 6 shows a comparison of this work with others working at similar frequency range. If the measurement results agree with the simulations, we have obtained a VCO which consumes half the current that [5] with similar phase noise figure at the frequency offset used in [5].

| Ref. | Techno | $f_0$[GHz] | $\mathcal{L}$[dBc/Hz] | $I_D$ | Obs. |
|---|---|---|---|---|---|
| [18] | $0.35\mu m$ | 1.55-2.0 | $-127_{@0.4MHz}$ | 7mA | BiCMOS |
| [5] | $0.18\mu m$ | 2.63 | $-106_{@0.4MHz}$ | 1mA | - |
| [19] | $0.18\mu m$ | 1.8 | $-127_{@0.6MHz}$ | 10mA | $Q_{ind}$=16 |
| [20] | $0.35\mu m$ | 2 | $-120_{@0.6MHz}$ | 1.1mA | $Q_{ind}$=8 |
| [21] | 90nm | 1.75 | $-107_{@1MHz}$ | 6.3mA | New Arch. |
| (*) | 90nm | 2.35 | $-107.5_{@0.4MHz}$ | 0.4mA | Simulated |

**Table 6: Comparison between our 2.4GHz VCO - marked with (*)- and previous published works.**

## 4.3 Tank Elements

The correct modelling of tank elements in the MATLAB stage proved to be as important as transistor modelling, to obtain mapping curves and final design as accurate as possible. For inductor modelling, ASITIC program turned to be useful in terms of speed and accuracy, in many of the simulated inductor geometries and values.

Considering varactors, generally their quality factors drop at high frequencies. Therefore, is not always valid our initial assumption of smaller varactor parasitic resistance respect of that of the inductor, as it happens in the 90nm CMOS technology used for this work. Besides, it is not always possible to accurately model varactors in MATLAB. This situation also occurred in the 90nm-technology, which leaded to lat-

[2]This shift in the carrier frequency from 2.4GHz is because of output buffer load, added to perform the measurements

ter adjustments in varactor and inductor sizes of the 2.4GHz VCO design to achieve the desired frequency.

## 5. CONCLUSIONS

A new LC-VCO design optimization methodology using the $g_m/I_D$ approach has been proposed throughout this work. By applying the LC-VCO design scheme proposed, with the $g_m/I_D$ transistor curves and the passive components' models, it is obtained the corresponding VCO design space. When considering jointly current consumption and phase noise, it makes possible the study of current consumption optima. The election of a certain point of this design space fixes all component's values as well as bias current $I_D$. Following this procedure, the designer saves a considerable number of trials and simulations.

The presented approach aids the designer to more easily select the operating point for typical values, which is usually the first step in a design. Future work on this topic should address how much is affected the selected design point with the spread of parameters as well as to include in the design procedure the possible trade-offs between optimization of the design point for typical parameter values and performance variation with process parameters spread and temperature.

The analysis has been validated with two design examples in micro and nanometric technologies, by simulations and measurements. Both of them have low current consumption and reasonable phase noise figures.

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