Model Current-Mode Control With Ease and Accuracy

By Rendon Holloway, Principal Engineer, Fairchild Semiconductor, San Jose, Calif., and **Gabriel Eirea**, Ph.D., Instituto de Ingenieria Electrica, Universidad de la Republica, Uruguay

A proposed new model for current-mode control retains the strengths of existing models such as ease of use and the ability to capture subharmonic oscillations, while improving on weaknesses like dc gain accuracy.

Current-mode control (CMC) is widely used in dc-dc converters for high-performance applications. In spite of its implementation simplicity, the dynamics are complicated and designing the control loop can be challenging. Many research efforts in the last two decades have refined dynamic models that capture the most relevant aspects of the controller behavior. Today's designers can choose from a vast pool of theoretical resources when developing a CMC solution.

A new model is being proposed that maximizes the advantages of the most popular model, while improving on its weaknesses. This model is based on already existing models but outperforms them in the design practice.

Eliminating Inductor Dynamics

The main idea behind CMC is that the inductor can be turned into a current source, thus eliminating the dynamics of the inductor in the loop. The controller sets a current reference and a fast inner-loop follows this reference cycle by cycle.

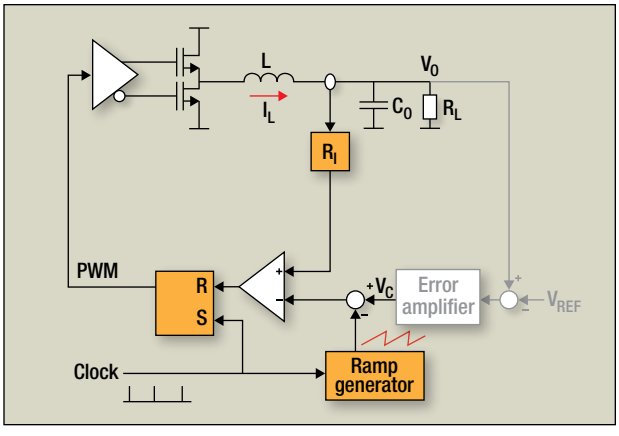

Fig. 1. *In peak current-mode control, the inductor's peak current follows a reference. The error amplifier compensates for the dynamic response of the output voltage.*

A typical implementation for a buck converter is shown in Fig. 1. This is the so-called peak CMC, because the inductor peak current follows the reference, as shown in the Fig. 2 waveforms. (Note that the inductor current shown in Fig. 2 corresponds to the *sensed* current, i.e., $R_I \times I_L$) There is an outer voltage loop with an error amplifier that compensates for the dynamic response of the output voltage. The current loop is an inner loop that provides tight control on the peak inductor current.

There are similar architectures for average CMC and valley CMC, although they are not as popular. The compensation ramp shown in Fig. 1 is introduced to avoid subharmonic oscillations for duty cycles larger than 0.5. The slope of the compensation ramp (S_E in Fig. 2) plays an important role in the response of the system, as will be shown later.

Assuming that current tracking is perfect, the system effectively becomes a first-order model. The inductor current can be assumed to be equal to the reference current (V_C/R_I in Fig. 1). The control-to-output transfer function for a buck converter becomes:

$$\frac{V_O}{V_C} = \frac{1}{R_I} \frac{R_L(R_C C_O s + 1)}{(R_L + R_C)C_O s + 1}, \qquad \text{(Eq. 1)}$$

where R_C is the ESR of the output capacitor.

Because this first-order transfer function is very easy to compensate, the design of the error amplifier is ideally simplified.

The assumption that current tracking is perfect is only valid for slow variations of the control signal, thus this model is only meaningful at low frequencies. If there is a need to push the bandwidth of the closed-loop system to frequencies above approximately one-tenth of the switching frequency, then a more detailed description of the dynamics

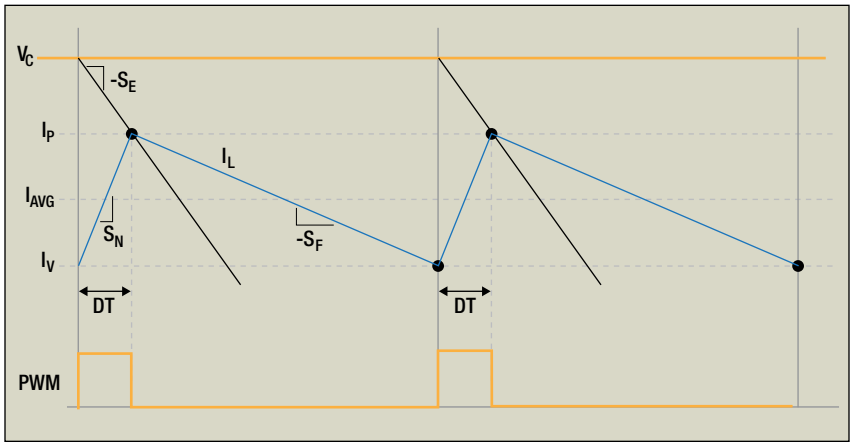

Fig. 2. *The slope of a compensation ramp using current-mode control avoids subharmonic oscillations for duty cycles larger than 0.5.*

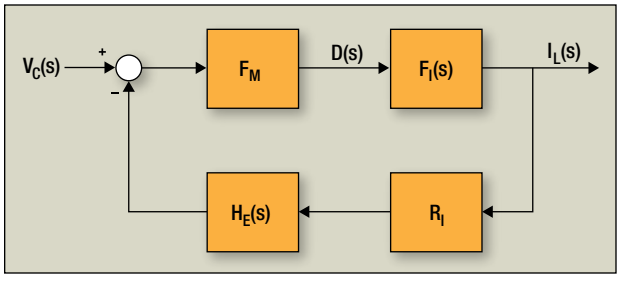

Fig. 3. *In Ridley's continuous-time model for current-mode control, the inner current loop allows one to predict low-frequency behavior and high-frequency subharmonic oscillations.*

of the current modulator is needed.

Over the years, many researchers have proposed models for CMC that take into account the dynamics at frequencies approaching the switching frequency. These models are developed under different assumptions about two main aspects of the loop dynamics.

The first assumption is the duty-ratio constraint that relates the duty cycle to the average values of the programmed current, the inductor current, the input voltage and the output voltage. Typical for this constraint are the use of a piecewise linear inductor waveform, in which the slopes may be constant or may change with the input and output voltages, and the definition of average inductor current, which can be computed as in steady-state or transient operation.

The second assumption is the sampling effect inherent to the modulation method. Typical for the sampling effect are the inclusions of either a fixed delay or a zero-order hold effect. It was noted that the modulator creates frequency components at the output that were not present at the input and that, for perturbations above one-tenth of the switching frequency, the additional components at the output are significant. This fact, together with the time-varying nature of the modulator, poses a warning against the validity of linear time-invariant (LTI) models for characterizing the behavior of the current loop at high frequencies. However, practice has demonstrated that LTI models are very useful for the design process, because they can capture enough information as to predict the stability and performance of the controller.

A unified model for different current-mode architectures and using general gain parameters was presented by Robert Sheehan of National Semiconductor ("A New Way to Model Current-Mode Control," June 2007, *Power Electronics Technology*). The unified model is consistent with the general models derived and can be extended to emulated CMC using sampling and hold techniques.

A very popular and widely accepted model was first introduced by Raymond B. Ridley ("A New, Continuous-Time Model for Current-Mode Control," *IEEE Transactions on Power Electronics*, 1991, vol. 6, no. 2, pp. 271-280). That model is derived using a sampled-data analysis and takes into account the sampling effect of the modulator by introducing a zero-order hold. As a result, both low-frequency behavior and high-frequency subharmonic oscillations can be predicted. The inner current loop is then modeled as shown in Fig. 3:

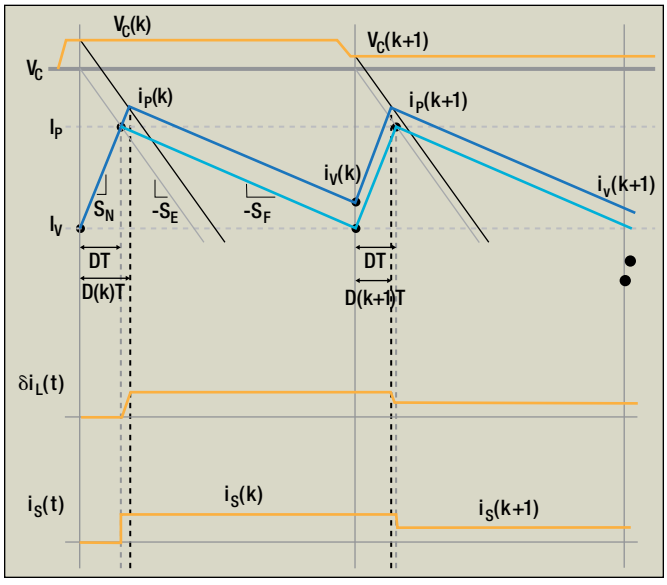

Fig. 4. *Waveforms with a perturbation in the command.*

$$F_M = \frac{1}{(S_N + S_E)T_S}. \quad \text{(Eq. 2)}$$

where F_M is the modulator gain, S_N is the on-time slope of the sensed inductor waveform, namely $R_I \times V_I/L$ in a buck converter, S_E is the slope of the compensation ramp and T_S is the switching period.

$$F_I(s) = \frac{S_N + S_F}{R_I s}, \quad \text{(Eq. 3)}$$

where F_I is the approximate transfer function (ignoring parasitics and assuming the output voltage is constant) from the duty cycle to the inductor current and the sampling gain is:

$$H_E(s) = \frac{sT_S}{e^{sT_S} - 1}. \quad \text{(Eq. 4)}$$

A rational approximation of Eq. 4 can be computed using a Padé approximation of order (2, 2) of the exponential function. This is useful for analysis purposes and for using some simulation tools that only allow rational transfer functions. The resulting sampling-gain approximation becomes a two-zero function given by:

$$H_E(s) \approx 1 + \frac{s}{\omega_N Q_Z} + \frac{s^2}{\omega^2_N}, \quad \text{(Eq. 5)}$$

where $\omega_N = \pi/T_S$ and $Q_Z = -2/\pi$.

It has been noted in literature (Mayer and King, The University of Toledo) that some of the assumptions yield an inaccurate dc gain in the loop-transfer function. This was confirmed in practice by the authors. In the following section, the source of this inaccuracy is identified and a new model with an accurate dc gain is proposed.

Proposed New Model

The new model proposed here incorporates most of the assumptions of Ridley's continuous-time model with one small but important difference in the computation of the average inductor current. From Fig. 2, the sensed peak current (I_P) can be expressed in terms of V_C as:

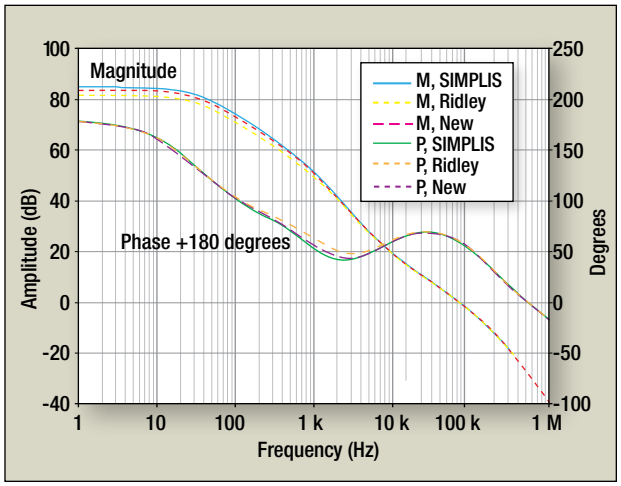

Fig. 5. *A comparison of loop transmission Bode plots for the switched model (SIMPLIS), Ridley's model, and the proposed new model.*

$$I_P = V_C - S_E dT_S, \quad \text{(Eq. 6)}$$

and in terms of the average sensed inductor current (I_L) as:

$$I_P = I_L + S_N d\frac{T_S}{2}. \quad \text{(Eq. 7)}$$

(Note that the average inductor current is computed as in steady-state operation, under the assumption that the inductor current returns to the same valley value at the end of the cycle.)

From Eqs. 6 and 7:

$$V_C - S_E dT_S = I_L + S_N d\frac{T_S}{2}. \quad \text{(Eq. 8)}$$

Then, under the assumption that slope S_N is constant, the modulator gain can be expressed as:

$$F_M = \frac{d}{(V_C - I_L)} = \frac{1}{\left(S_E + \frac{S_N}{2}\right)T_S}. \quad \text{(Eq. 9)}$$

This expression is different from the one used in Ridley's continuous-time model. Actually, this modulator gain was reported even earlier (Middlebrook, Caltech), but in the context of a different derivation method.

Following Ridley's derivation, a perturbation in the command voltage is introduced and the variation in the inductor current is computed (Fig. 4). The variation in the inductor current is approximated by the sampled waveform $i_S(k)$. Then, the closed-loop-transfer function between the command voltage V_c and the sampled inductor current (i_S) can be computed in the discrete-time domain, resulting in:

$$H(z) = \frac{i_S(z)}{v_C(z)} = \frac{1}{R_I}\frac{S_N + S_F}{S_N + S_E}\frac{z}{z + \frac{S_F - S_E}{S_N + S_E}}. \quad \text{(Eq. 10)}$$

The equivalent continuous-time transfer function can be obtained as:

$$H(s) = \frac{1 - e^{-sT}}{sT} H(z)\Big|_{z=e^{sT}} \quad \text{(Eq. 11)}$$

$$H(s) = \frac{1}{R_I}\frac{1+a}{sT_S}\frac{e^{sT_S} - 1}{e^{sT_S} + a}, \quad \text{(Eq. 12)}$$

Parameter	V_{IN}	V_{OUT}	I_{OUT}	L	C	ESR	R_I	T_S	S_E
Value	5 V	1.2 V	1 A	3.3 µH	47 µF	10 mΩ	1.5 Ω	769 ns	2.25 V/µs

Table. *Parameters used in the simulation.*

where $a = (S_F - S_E)/(S_N + S_E)$.

In Fig. 3:

$$H(s) = \frac{F_M F_I(s)}{1 + F_M F_I(s) H_E(s) R_I} \quad \text{(Eq. 13)}$$

The new sampling gain $H_E(s)$ is computed as:

$$H_E(s) = \frac{sT_S}{e^{sT_S} - 1} \frac{S_N(e^{sT_S} + 1) + 2S_F}{2(S_N + S_F)}. \quad \text{(Eq. 14)}$$

A rational approximation can be obtained applying the same Padé approximation, resulting in:

$$H_E(s) \approx 1 + \frac{s}{\omega_N Q_Z} + \frac{s^2}{\omega^2_N} \quad \text{(Eq. 15)}$$

where $\omega_N = \pi/T_S$ and $Q_Z = -(S_N/S_F + 1)2/\pi$.

This expression is almost equal to the one in Eq. 5 with a slight difference. Although both the dc gain and the frequency of the double zero are the same, the quality factor is different.

Comparison of Models

The loop-transfer function of both the proposed new model and Ridley's model are compared with that obtained from a switched model simulated with the SIMetrix/SIMPLIS software tool. The advantage of the SIMPLIS simulator is that it can compute a periodic operation point and introduce perturbations to obtain a small-signal transfer function around said operation point, thus computing numerically the transfer function. The former models were simulated using SIMetrix SPICE and performing a traditional ac analysis.

For this example, a buck converter with Fairchild's FAN2013 controller was used. The FAN2013 is a 2-A low-voltage current-mode synchronous pulse-width-modulated buck regulator designed for applications like hard-disk drives, set-top boxes, notebook computers and communications equipment. The circuit parameters used in these simulations are listed in the table.

The results are shown in Fig. 5. The new model proposed here shows a more accurate dc gain and improved mid-frequency phase characteristics than Ridley's model. References to prior work mentioned in this article are listed in the online version at www.powerelectronics.com. **PETech**