

Common Gate LNA Design Space Exploration in All Inversion Regions

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Abstract—The design of CMOS CG-LNAs using a design space exploration proposed for all inversion regions, from weak to strong, is performed in this work. The exploration is done in terms of current consumption, gain and noise figure in the design space $(I_D, \frac{g_m}{I_D})$ showing the trade-offs of designing the CG-LNA in moderate or weak inversion. Finally comparisons between the MATLAB design space exploration and BSIM3v3 simulations using Spectre-RF are done, through the design example of a 900MHz CG-LNA implemented in a $0.35\mu m$ CMOS technology.

Index Terms—Common Gate LNA, Low power consumption, All inversion regions, Design Methodology, ACM model.

I. INTRODUCTION

In autonomous front-end RF applications, exist either strong power and noise constraints. Therefore, the design of these circuits carry on several trade-offs which can be seen clearly by using a design space exploration of their characteristics.

In this work it is presented the design space exploration of a single-ended common gate low noise amplifier (CG-LNA), considering noise figure and gain as its basic characteristics. All the inversion levels were considered.

In [1] it is performed a design space exploration but considering only strong inversion transistor operation. In ([2], [3]) present a graphical optimization of a CG-LNA, using the all-region EKV model, but in these works no study of inductor constraints was done. In [4] the ACM model is used to design a LNA but in this case it is a common source LNA.

With the aid of MATLAB, the design space exploration of the CG-LNA is done using power gain G_T and noise figure (NF). The all-region ACM CMOS transistor model is used. Limitations imposed by using on-chips inductors are also studied and included in the exploration. The CG-LNA proposed does not have an input matching network, so limitations in the load resistance for achieving the desired input impedance are also considered. Following a design flow, the complete set of the LNA parameters are obtained. A discussion of how the inversion level affects the current consumption, the gain and the noise figure of the CG-LNA is developed.

In section II is done a brief review of the transistor model used. In section III are given the description and behaviour of the CG-LNA. The design exploration and results are given in section IV and V. Finally a design example is described in VI.

II. ACM MODEL

For the theoretical deductions and simulations, the one-equation- all-region MOSFET model ([5] [6]) has been used to describe the transistor behaviour. This is a physical-based compact model valid for all inversion levels. In this design, the transistors are considered to be working in the saturation region. In the ACM model, the drain current is expressed as the difference between the forward I_F and reverse I_R components,

$$I_D = I_F - I_R = I_S(i_f - i_r) \quad (1)$$

where

$$I_S = \frac{1}{2}n\mu C'_{ox}\phi_t^2 \frac{W}{L} \quad (2)$$

I_S is the specific current, which is proportional to the aspect ratio of the transistor. V_G , V_S and V_D are the gate, source, and drain voltages, with reference to the substrate. μ is the effective mobility, ϕ_t is the thermal voltage, C'_{ox} is the gate oxide capacitance per unit area and n is the slope factor, slightly greater than unity and weakly dependent on the gate voltage. Parameters i_f and i_r are the normalized forward and reverse currents, or inversion levels at source and drain, respectively. Note that, in the saturation region, the drain current is almost independent of V_D ; therefore, $i_f \gg i_r$ and $I_D \cong I_F$. The small-signal transconductances g_m , g_{m_s} y g_{m_d} (gate, source and drain transconductances) are given by

$$g_{m_{s(d)}} = -\mu \frac{W}{L} Q'_{I_S(D)} \frac{2I_S}{\phi_T} \left(\sqrt{1 + i_{f(r)}} - 1 \right) \quad (3)$$

$$g_m = \frac{g_{m_s} - g_{m_d}}{n} \quad (4)$$

The other small-signal parameters can also be derived in terms of the inversion levels. For the sake of simplicity a complete list of expressions is not here presented, but ACM intrinsic capacitances equations [5] were employed throughout the design process.

The considered model is a long channel model. Nevertheless, considering the technology analyzed ($0.35\mu m$), and the fact that there is no interest in working in deep strong inversion, the effect of short channel effects, velocity saturation and mobility reduction may be neglected, as the agreement between calculations and simulations show.

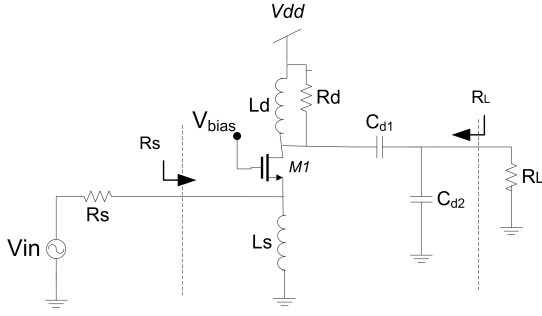


Figure 1.

III. CG-LNA DESIGN

A. Circuit description

The circuit, shown in Fig. 1, is a single-ended common gate narrowband (CG-LNA). It consists of the transistor M_1 which fixes the gain and the real part of the input impedance and the inductor L_s , that cancels the imaginary part of the input impedance. L_d , R_d , C_{d1} and C_{d2} are part of the output matching network and include the parasitic capacitances of M_1 .

Due to the topology characteristics it is a narrowband device, as the input impedance is real only at the resonant frequency. The input impedance is

$$Z_{in} |_{s=j\omega_0} (s) = \frac{1}{g_m + g_{mb}} \frac{2r_{ds} + R_L}{2r_{ds}} \quad (5)$$

when

$$\omega_0 = \frac{1}{\sqrt{L_s C_{gs}}} \quad (6)$$

At resonance, Z_{in} must be equal to R_s , as no input matching network is used. It means that, for a fixed R_s and a fixed transistor size, the load resistance R_L is fixed and equal to ([1]):

$$R_L = 2(R_s n g_m - 1) r_{ds} \quad (7)$$

It is interesting to note that for certain values of g_m and R_s , R_L can be negative, as so an input matching network would be needed.

The g_{ds} is the transistor small signal output conductance. It is modelled as proportional to the transistor transconductance, assuming that in moderate and weak inversion the DIBL effect dominates over the channel length modulation effect ([7]).

The power gain is

$$G_T = \frac{R_L}{4R_s} \quad (8)$$

The NF of this circuit is:

$$NF = 10 \log(F) \quad (9)$$

with F , the Noise Factor, given by ([1]):

$$F \cong 1 + \frac{\gamma}{n g_m R_s} + \frac{2R_s}{(n g_m R_s - 1) r_{ds}} \quad (10)$$

where γ is the channel thermal noise coefficient.

B. Design flow

For a complete CG-LNA design, the following parameters must be computed: L_s , M_1 width W_{M_1} , M_1 transistor current I_D . M_1 transistor length L_1 is chosen the smallest available to reach the highest f_T for a certain I_D . Requirements of NF , current consumption, Z_{in} and gain must be fulfilled.

The design flow is as follows. A couple $(I_D, \frac{g_m}{I_D})$ is chosen. This determines g_m , i_f , W_{M_1} ([8]) and C_{gs} . L_s is obtained from (6). R_L is calculated from (7). Power gain G_T is calculated using (8) and NF using (9) and (10).

IV. DESIGN SPACE EXPLORATION ALGORITHM

The proposed algorithm for designing RF CG-LNA considers the design space defined by the DC bias current I_D of the active transistor M_1 and the $\frac{g_m}{I_D}$ ratio of this transistor. In this design space the current consumption was considered for a given NF and power gain of the CG-LNA.

The algorithm is summarized as follows: the design space is covered by a grid of couples $(I_D, \frac{g_m}{I_D})$. For each of these couples, the $NF = NF(I_D, \frac{g_m}{I_D})$ and the power gain $G_T = G_T(I_D, \frac{g_m}{I_D})$ are obtained.

Having explored the design space, as it is shown in the following example in the next section, for a given NF , the minimum of current consumption is in weak inversion.

A. Inductor and load resistance constraints

The inductor values are themselves a limitation in the design, as they are on-chip inductors. The limitations come from the range of inductors available in the technology used and area constraints, and it marks the feasibility or not of having the circuit completely integrated.

In the design space exploration, the constraints in the L_s inductor is considered. It cannot be higher than L_s^{max} or lower than L_s^{min} , limits imposed by the technology used.

As L_s is also obtained from the couple $(I_D, \frac{g_m}{I_D})$, this constraint is added in the design space. It means that there is only a valid zone of the design space that can be used to choose a design.

As previously mentioned, the R_L resistance is also limited by the couple $(I_D, \frac{g_m}{I_D})$. If no matching network is to be used, certain zone of the design space is neglected for the design, in case negative R_L resistance values are needed.

V. RESULTS AND DISCUSSION

In the following example, the maps of NF and gain generated by the algorithm are shown and briefly explained. Using a $0.35\mu m$ CMOS technology and working with the ACM model, the design space of a CG-LNA is generated. We will consider the following design requirements: working frequency $f_0 = 900 MHz$, voltage supply $V_{dd} = 2.5V$, power gain $G_T \cong 10dB$, NF less than 3dB and current I_D less than 2mA. Also the output and input impedance must be 50Ω . The output network must be also designed.

The design space considering only the power gain evaluation is shown in Fig. 2. The zone where $R_L < 0$ is discarded in the routine as G_T is expressed in dB. In Fig. 3 it is shown the

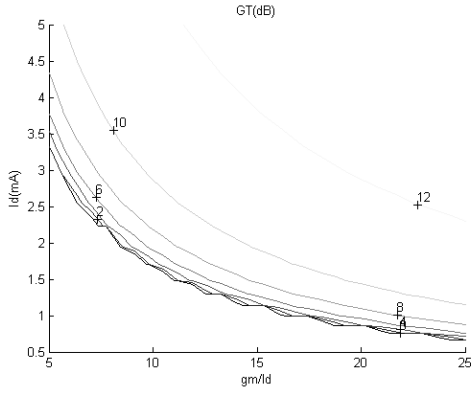


Figure 2. Design space exploration considering G_T

NF curves jointly with the inductor's valid zone, and also the design point chosen. The power gain and the NF are plotted separately to simplify the study. The design point chosen reaches all the design requirements previously mentioned.

In Table I the parameters calculated in Matlab for this particular point of the design are shown

Analyzing the NF and G_T curves, some comments regarding to the selection of the inversion level can be made. For a particular value of NF , we can achieve lower current consumption if we move towards weak inversion. Also, for a certain G_T , the power consumption decreases as we increase $\frac{g_m}{I_D}$. It is interesting to note that both characteristics have the same tendency when we work in moderate or weak inversion.

The proposed method, allows to perform a simple design space exploration that provides fairly accurate results when compared with simulation results. Nevertheless some limitations of the accuracy of the applied model must be discussed. For weak inversion the f_T is near the operating frequency - and particularly for the point chosen where the technology f_T is around 2GHz. As we are not considering non quasi-static effects in the ACM model equations used, there is an error in the parameters calculated in this zone. On the other hand when going towards strong inversion, though usually this will not be the region of interest for operation in this architecture, some error would be associated with neglecting the velocity saturation and mobility reduction effects.

VI. DESIGN EXAMPLE

In this section the complete design of the CG-LNA and the simulation results using Spectre-RF, using the above design point are shown.

To complete the design, the values of L_d , R_d , C_{d1} and C_{d2} were calculated for a 50Ω output load R_L , and are shown in Table II.

In Table I the values of the simulated NF , gain and I_D , among others, are compared with the ones obtained with the Matlab design exploration. Very good agreement exists between calculated and simulated results.

In Figs. 4, 5, 6 and 7 the S-parameters are shown. Reverse isolation value is good [1]. The input and output impedance

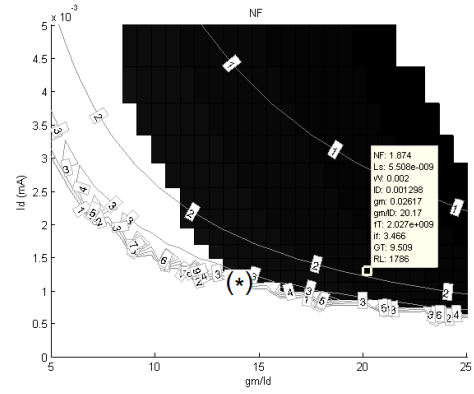


Figure 3. Design space exploration considering NF , with the constraints of R_L and L_s . Design point shown. (In the zone marked with an $*$) the NF rises to values up to 12dB and then decreases until the R_L value is 0.)

Parameter	Calculated in Matlab	Simulated in Cadence
I_D (mA)	1.3	1.27
$\frac{g_m}{I_D}$	20	21
g_m (S)	26m	26.5
NF (dB)	1.87	2.1
G_T (dB)	9.5	9.8

Table I
PARAMETERS CALCULATED WITH MATLAB AND SIMULATED WITH SPECTRE-RF

values are : $Z_{in@900MHz} = (30 + 13j)\Omega$ and $Z_{out@900MHz} = (32 + 11j)\Omega$. These values are not 50Ω as expected; to adjust them some iterations in the component values of the output network and the source inductance are needed.

Also it is shown the simulated NF in Fig. 8. In Fig. 9 is plotted the $IIP3$, which has a simulated value of 4.6dBm.

VII. CONCLUSIONS

A design space exploration to design RF CG-LNA using an all-region CMOS transistor model has been presented in this work. It has been shown how the inversion level affects the NF , the current consumption and the gain. Moreover, it has been shown how operation in moderate or even in weak inversion decrease the current consumption without decreasing G_T or NF . The R_L constrains has been considered and also it has been studied the importance of considering the inductor size constrains in the design space exploration. Finally, an example of a design was considered and very good agreements between

Parameter	Value
$W(\mu m)$	2000 * 0.35
$L(\mu m)$	0.35
L_s (nH)	5.5
L_d (nH)	10
$R_d(\Omega)$	1800
C_{d1} (pF)	1.7
C_{d2} (pF)	6.6

Table II
DESIGN COMPONENTS

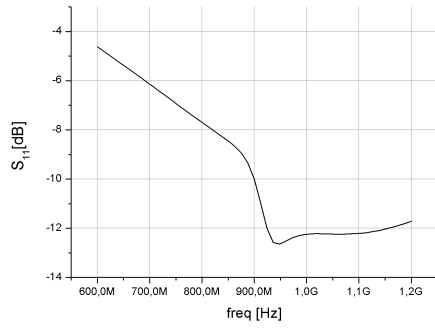


Figure 4. S_{11} parameter

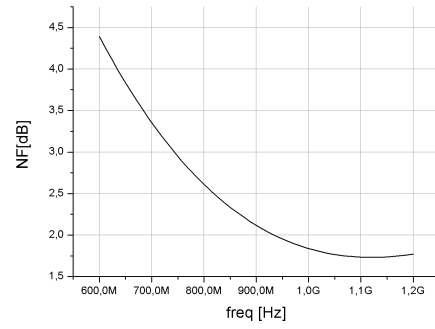


Figure 8. NF

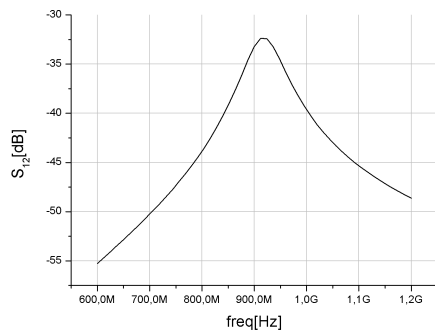


Figure 5. S_{12} parameter

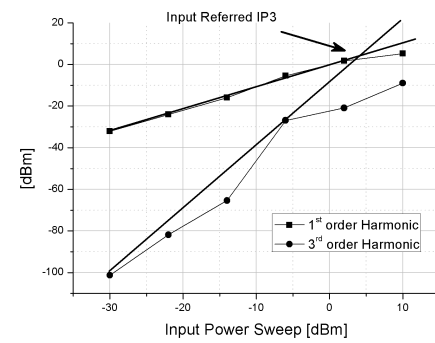


Figure 9. $IIP3$

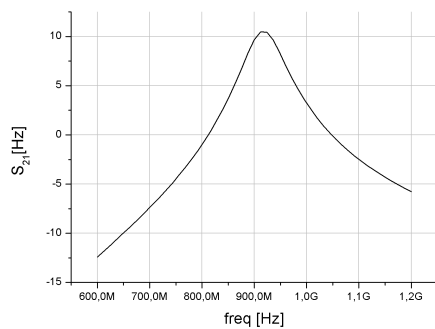


Figure 6. S_{21} parameter

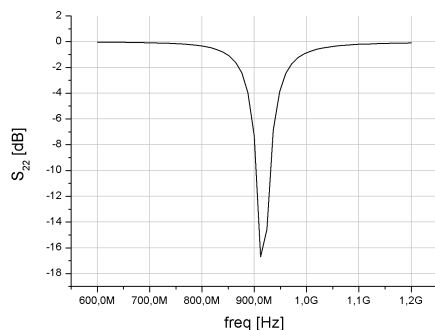


Figure 7. S_{22} parameter

the MATLAB calculations and the Spectre-RF were observed.

VIII. ACKNOWLEDGEMENTS

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