Ultra-low Power Temperature Sensor

Pablo Aguirre and Conrado Rossi
Instituto de Ing. Eléctrica, Facultad de Ingeniería
Universidad de la República
Montevideo, Uruguay.
{paguirre,cra}@fing.edu.uy

***Abstract*— We propose an architecture and circuit for temperature sensors integrated within systems on a chip. The circuit is based on special properties of devices when biased by a current with a particular dependence with temperature. We present results from a test circuit fabricated on a standard $0.8\,\mu\mathrm{m}$ CMOS technology which draws under 40 nA from a 1.6 V to 3.0 V supply at room temperature. Measurements show that the circuit is suitable for temperature sensing with a $\pm$0.5 K uncertainty in the 290 K to 350 K range.**

Keywords: Temperature Sensor, Microelectronics, Low Power.

I. Introduction

The current state of electronic systems design allows the integration of an increasing number of circuits in a single chip. A wide spectrum of applications benefit from the inclusion of sensing functionality in these systems-on-chip (SoCs). In particular, temperature is the most frequently used measurand in sensor technology [1]. It is not only important by itself but also as a compensation parameter for other sensors, so there is a frequent need to include temperature sensors at the chip level in many sensing systems.

Moreover, ultra low power sensing circuits allow these so-called intelligent sensors to be used in portable or even implantable applications where very long battery life together with limited size is paramount. Examples can be found in biomedical, cold chain monitoring and industrial applications.

The main goal of our research in temperature sensors is to achieve the minimum possible consumption while low voltage is also a desirable characteristic. The desired precision is around 0.5 K for a temperature range from 230 K to 400 K, except in the case of biomedical applications where the temperature range is much limited but the precision should be around 0.05 K.

We researched ways to obtain basic PTAT (proportional to absolute temperature) and NTC (negative temperature coefficient) cells for our temperature sensors. In [2] we detail the theory behind the cells and provide simulation results in the 230 K to 400 K range while [3] reviews preliminary experimental results. The present work presents further analysis on our measurements.

II. Notation

The following notation will be used throughout this paper.

Temperature relative to an arbitrary reference (often, $T_R = 300\ K$) will be denoted as

$$x = \frac{T}{T_R} \tag{1}$$

The R subscript will be applied to any variable taken at the reference temperature.

We will use the following notation for the thermal voltage:

$$U_T = \frac{kT}{q}, \qquad U_{TR} = \frac{kT_R}{q} \tag{2}$$

The usual models for MOS transistors are used for the different operating regions [4] where we will consider first order variations of the threshold voltage (V_T) with temperature:

$$V_T = V_{TR} + k_{VT}(x-1), \qquad k_{VT} < 0 \tag{3}$$

and the usual equation for the temperature dependence of mobility:

$$\mu = \mu_{_R}\, x^{k_\mu}, \qquad k_\mu < 0 \tag{4}$$

III. Proposed Architecture

In accordance to the SoC philosophy briefly mentioned in the Introduction, we consider temperature sensors that are integrated on the same chip to the rest of the system. Thus, it is important to take into account the whole sensing subsystem from the temperature sensitive components, through the signal conditioning, if existent, to the A/D converter. That is, in terms of architecture we will consider a complete sensing system with digital output.

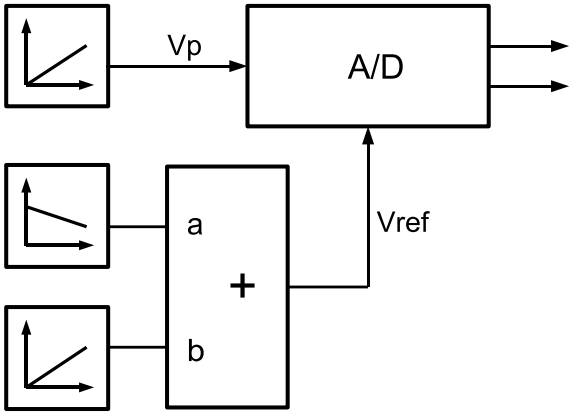


Fig. 1. Block Diagram of classic Temperature Sensor

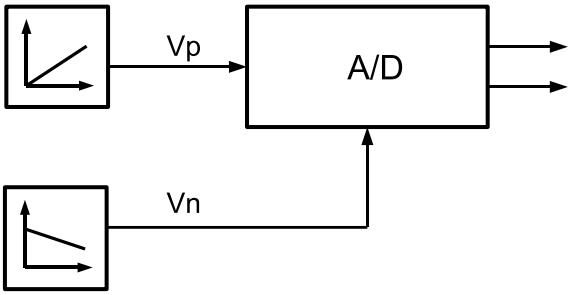


Fig. 2. Block Diagram of proposed architecture

The building blocks usually needed for a digital output Temperature Sensor are: a proportional to absolute temperature (PTAT) generating block, a constant reference (bandgap) block and an A/D converter. (Fig. 1)

As shown, the bandgap reference is in general obtained by summing a PTAT voltage with an NTC voltage, thus cancelling out the temperature variation to the first order. The negative temperature dependence is usually implemented with a diode-connected bipolar transistor (BJT).

Generally, a PTAT voltage will be expressed as:

$$V_p = k_p x \tag{5}$$

and an NTC voltage can be described to the first order as:

$$V_n = V_0 + k_n x, \qquad k_n < 0 \tag{6}$$

Some of the signal processing implied in Fig. 1 can be performed in the digital domain [5]. We propose to represent the temperature information through a digital word (Fig. 2) which is the ratio of a PTAT voltage (V_p) and an NTC reference (V_n).

The classical approach of Fig. 1 has two calibration parameters: V_{ref} and k_p and the main errors are caused by imperfect compensation of the NTC voltage with the PTAT signal and non-linearities in the bandgap circuit.

The proposed diagram on Fig. 2 has three calibration parameters: V_0, k_n and k_p. The main error arises from not considering higher order terms in Eq. 6. In this case, the correct determination of the extra parameter is equivalent to the perfect compensation inside the bandgap of the former option. So, both of them are equivalent in terms of calibration, but our proposal exhibits the flexibility of digital computation instead of performing compensation of parameters in the analog circuit.

This approach takes signal processing from the analog to the digital domain, probably with advantages in terms of consumption [6]. Curvature compensation can be performed digitally at a system level in both cases.

In practice, the A/D conversion can be done by using an arbitrary (even not fully known) reference (V_{ref}) for the A/D, so obtaining digital words:

$$D_n = \frac{V_n}{V_{ref}}, \qquad D_p = \frac{V_p}{V_{ref}} \tag{7}$$

We can later compute:

$$\theta = \frac{D_p}{D_n} = \frac{V_p}{V_n} \tag{8}$$

which is independent of $\mathrm{V_{ref}}$, thus simplifying the A/D converter.

IV. Implemented Circuit

In order to implement the architecture of Fig. 2 we need to design a circuit that generates V_p and V_n while keeping a low current consumption. After researching several options, our best choice is to base the circuit on the cell proposed by Oguey *et al.* [7] (Fig. 3) which acts as a current reference fixing the current in its branches and therefore, as we will show further on, determines the currents on the overall circuit.

The Oguey Cell is a modification of the PTAT (Proportional To Absoute Temperature) circuit, the most ubiquitous one both in temperature sensors and voltage references [5], [8]–[10]. Although it is usually implemented with bipolar transistors, it can be implemented with MOSFETs biased in weak inversion as well [11]. In both cases the carrier transport is dominated by difussion phenomena, and thus, they obey similar exponential equations.

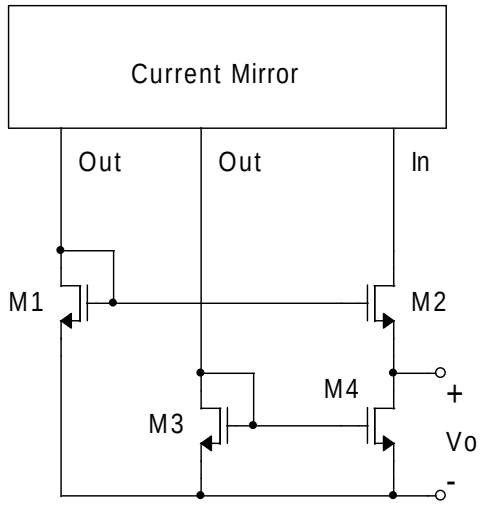


Fig. 3. Oguey Cell

The PTAT cell embedded in the Oguey circuit determines V_o which does not depend on the branch currents (Fig. 3):

$$V_o = \alpha_T U_T = x\,\alpha_T U_{TR}, \quad \alpha_T = \ln(AB) \quad (9)$$

where

$$I_{D1} = A\,I_{D2} \qquad S_2 = B\,S_1 \quad (10)$$

The branch currents, being fixed by the size of the transistors, present the following temperature dependence:

$$I_2 = I_4 = I_{4R}\,y(x)\,x^{k_\mu+2} \quad (11)$$

where

$$y(x) = \frac{n(x)}{n_R} \quad (12)$$

is the relative variation of the slope factor n with temperature and I_{4R} is the value of I_4 at some arbitrary reference temperature.

Expression of I_{4R} as a function of geometrical and technology parameters yields design equations which we have thoroughly reported in [2]. Proper sizing of M3, M4 and the current mirror allows us to independently choose I_{4R} and V_{G4R}.

For usual dopant concentrations and in the temperature range we are interested in, the theoretical value for the mobility exponent is $k_\mu = -1.5$ [12] while $k_\mu = -1.8$ for the technology of our prototypes. Besides, $y(x)$ varies just $\pm 5\%$ in a 200 K to 400 K range. Thus, I_4 has a weak temperature dependence and can be used as a *quasi-constant current* to bias

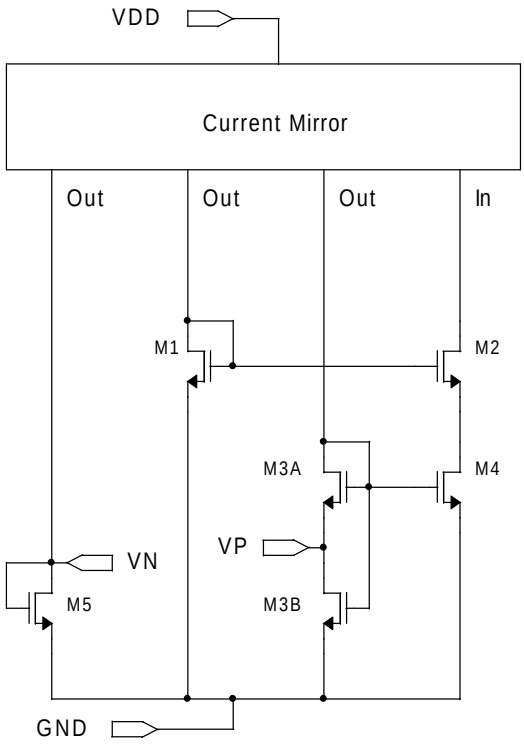


Fig. 4. Simplified circuit schematic

not only the embedded PTAT source but other circuits as well.

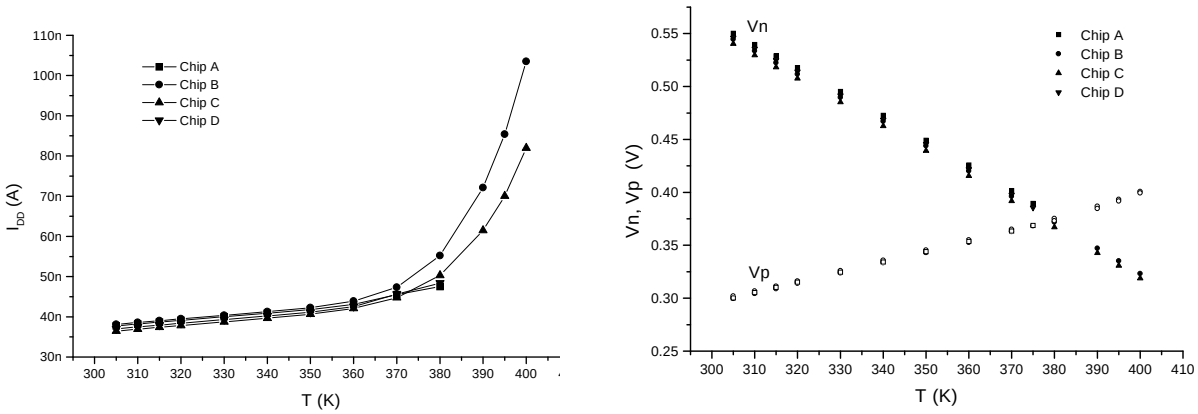
In [2] we have introduced the idea of using the above defined quasi-constant current in two basic circuits: a diode-connected MOS (Fig. 4, M5) and a MOS voltage divider (Fig. 4, M3A and M3B). We combined the aforementioned subcircuits in a comprehensive cell which generates several voltages with the main purpose of checking the proposed architecture.

A simplified scheme of the circuit is shown in Fig. 4. The Oguey circuit is formed by M1 to M4 as in Fig. 3 and biases all the branches with the quasi-constant current.

Mosfet M3 in the Oguey Cell, was split up in two serial transistors M3A and M3B implementing a MOS voltage divider, operating in strong inversion and biased with the quasi-constant current. In this way we obtain the PTAT voltage V_p [2].

The same current biases M5, a diode connected MOS operating in weak inversion. It generates V_n which displays a negative dependence with temperature [2].

In this circuit, any mismatch has the effect of changing one or more parameters of the output voltages. This is no worse than the parameter uncertainty due to technology parameter spread. Both effects have to be dealt with by proper calibration.



(a) Current consumption

(b) PTAT and NTC voltages

Fig. 5. Measurement results as a function of temperature for 4 prototypes

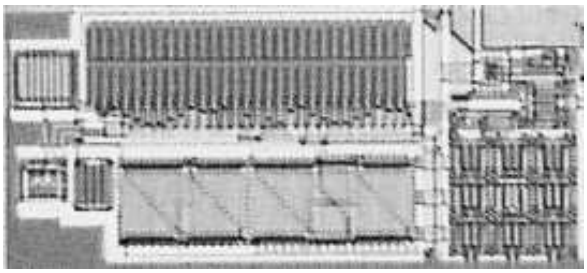


Fig. 6. Microphotograph of the fabricated cell

V. Experimental Results

The test circuit was fabricated on a standard $0.8\,\mu m$ CMOS technology. Fig. 6 shows a microphotograph of the circuit, which has an area of $(465 \times 210)\,\mu m^2$.

Four samples (chips A-D) were tested, measuring outputs V_p and V_n and chip consumption I_{DD} at several combinations of ambient temperature and supply voltage V_{DD}.

Chips B and C were swept from 305 K to 400 K (aprox. 32^{o}C to 127^{o}C) while chips A and D were limited to 375 K. These tests were performed in a custom built oven under computer controlled temperature achieving an error of $\pm$10 mK.

All chips worked correctly with negligible output variations for $1.6\,\mathrm{V} \leq \mathrm{V_{DD}} \leq 3.0\,\mathrm{V}$ as predicted by simulations. Therefore, we only present results obtained at $\mathrm{V_{DD}} = 3.0\,\mathrm{V}$ which are representative of the behaviour through the whole supply operating range.

Fig. 5(a) shows the current through the power supply (I_{DD}) as a function of temperature for each sample. I_{DD} is proportional to the branch currents (I) in Fig. 4. The total current drawn from the supply is under 50 nA for $\mathrm{T} < 370\,\mathrm{K}$ and under 105 nA for $\mathrm{T} < 400\,\mathrm{K}$ [3].

The expected quasi-constant current model holds true up to 350 K, exponentially departing from it thereof. We traced this misbehaviour to leakage currents, mainly from the nwell area beneath the PMOS mirror and from the drain and source areas of M1 and M2. Measured output voltages are depicted as a function of temperature in Fig. 5(b). We present voltage data for the full temperature range. However some departure from the predicted values is expected for $\mathrm{T} > 350\,\mathrm{K}$ due to the effects of the increased leakage currents.

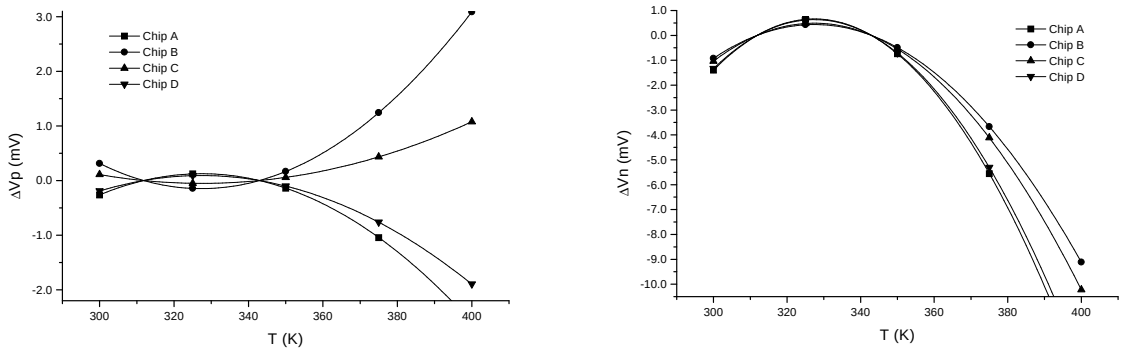
We further analyzed the experimental data by performing least squares linear and parabolic fits on them in the 305 K to 350 K range, beneath the onset of leakage. We estimated the curvature error of V_p and V_n (Fig. 7) as the difference between the parabolic and linear fits. Based on these graphs, we measured the linearity error defined as the maximum departure from the linear fit in a given temperature range.

For $300\,\mathrm{K} \leq \mathrm{T} \leq 350\,\mathrm{K}$, V_p presents a 0.97 mV/K slope with better than 0.32 mV linearity error while V_n displays a -2.2 mV/K slope with better than 1.4 mV linearity error.

Based on the parabolic fit, we computed θ (Eq. 8) as a function of temperature and simulated a two point calibration process obtaining parameters V_0, k_p and k_n. Using this parameters we computed the temperature from the values of θ, thus obtaining a calibration curve for our sensor. Fig. 8 shows that the temperature error is less than $\pm$ 0.5 K in the 290 K to 350 K range.

VI. Conclusions

We present a circuit which generates a quasi-constant current and NTC and PTAT voltages, useful for voltage references and temperature sensors. The circuit needs no resistors, thus it can be fully integrated while keeping a reduced area even for a current under



(a) Vp (b) Vn

Fig. 7. Linearity Error of Output Voltages

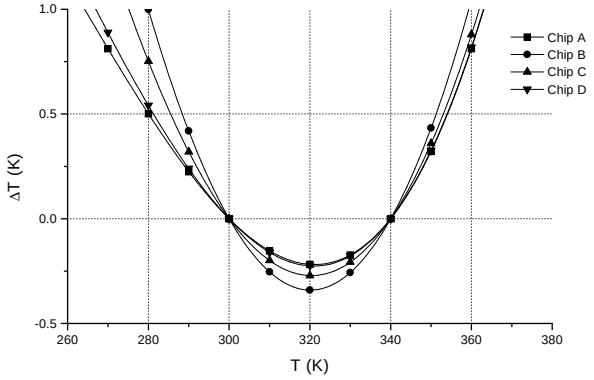


Fig. 8. Temperature Sensor Error due to Nonlinearity

50 nA (for $T \leq 370\,K$).

We evaluated the slope and linearity of the output voltages and their effect on the overall measurement error. The results show that the architecture and circuit are suitable for the required precision although the range was limited by leakage.

We are currently working on the tradeoff between temperature limits, leakage currents, consumption and area. Future work also includes assessing the effects of noise. This will allow us to obtain a complete, fully integrated, temperature sensor based on this approach.

VII. Acknowledgements

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