Wireless EEG miniaturized platform

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***Abstract*—This work presents the design, manufacture, and preliminary tests of the proof-of-concept of a miniaturized platform for acquiring electroencephalography signals, where the input stage is based on a high-CMRR current-efficiency custom-made integrated neural preamplifier.**

I. Introduction and Specifications

The proof-of-concept of a platform for acquiring EEG signals, targeting BCI applications and others, is presented. The required bandwidth in Hz is [0.1 300], and the input signal's amplitudes in μV are [200 400]. These amplitudes require an analog-to-digital converter of at least 12 bits. On the other hand, the platform needs eight channels. Then, Bluetooth Low Energy (BLE) is used to handle a sampling rate of 1 ksps, enabling data transmissions of 128 kbps. The platform must be portable by small animals; therefore, the targeted size is 6.25 cm^3 (25 mm x 25 mm x 10 mm), including PCB, batteries, and all components. Likewise, the ideal autonomy is 12 hours, and a minimum of 2 hours is acceptable.

II. Proposed Solution

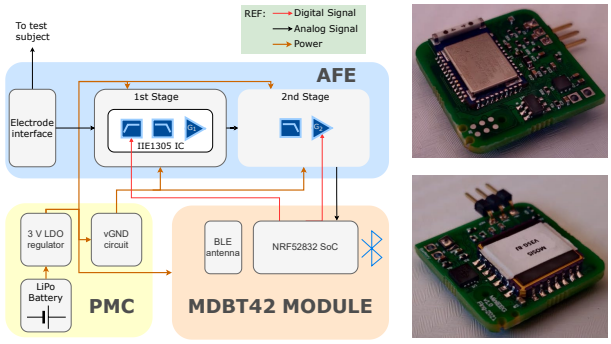

Fig. 1. Block diagram.

The device comprises an analog front-end (AFE) and the Raytac MDBT42-512KV2 module (see Fig. 1), which includes the Nordic Semiconductors NRF52832 System on Chip (SoC). The AFE has two stages. The input stage is based on a high-CMRR and current-efficiency (low NEF) neural preamplifier developed in [1] (G1 = 50 dB). The second stage is an additional stage of filtering and gain (G2), including the LT6011 operational amplifier and the MCP4012 digital potentiometer (R_{POT}) commanded by the SoC through an UP/DOWN protocol, allowing the configuration of the gain G2. The SoC includes an ARM Cortex M4 microcontroller with 64 kB of RAM and 512 kB of FLASH, allowing on-chip advanced signal processing. In addition, the SoC/Module includes eight analog inputs (12 bits), a BLE radio, and an integrated antenna. The Power Management Circuit (PMC) consists of a 3.7 V 50 mAh 1 cm^3 Li-Po battery, a TPS717 linear regulator that generates VDD = 3.0 V, and a circuit to set a reference voltage at the midpoint of VDD (vGND). The average total current consumption of the board is estimated to be 6.6 mA. The embedded software is implemented using *FreeRTOS*, including a simple test that permits configuring the AFE and acquiring and sending one EEG channel to the PC.

III. Testbench Results and Conclusions

Fig. 2 presents measurement results. The left side of the figure shows the AFE frequency response. The total gain (G1$\times$G2) is configurable between 63 dB and 101 dB, while the high-pass frequency can be set between 0.1 Hz and 100 Hz. The low-pass frequency is fixed at around 350 Hz. The lower right side presents the variations of the total gain according to the value of the digital potentiometer (R_{POT}). The upper right side shows the power spectral density of a signal received at the PC. The signal was sent from the platform by BLE after being amplified, filtered, and digitized. The input signal is a tone of 500 μV and 30 Hz. These preliminary results are promissory. The next step will be to test the platform using laboratory animals.

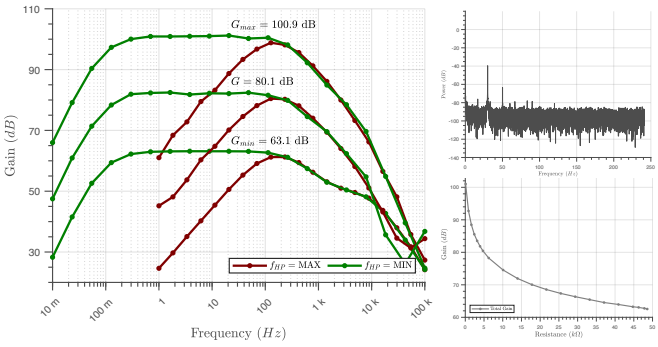

Fig. 2. Preliminary measurement results.

References

[1] J. Oreggioni, A. A. Caputi, and F. Silveira, "Current-efficient preamplifier architecture for CMRR sensitive neural recording applications," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 12, no. 3, pp. 689–699, June 2018.