A sub-μW intracranial EEG integrated preamplifier

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***Abstract*—This work presents an amplifier targeting the acquisition of intracranial electroencephalography signals with low power consumption, low voltage supply, low noise, and high common-mode rejection ratio (CMRR). A prototype was designed in a 180 nm FD-SOI CMOS technology and characterized by simulations. It presents an input noise of 3.2 μV_{rms}, a current consumption of 0.5 μA, and it operates from a 1.8 V voltage supply, which represents a power consumption of 0.9 μW. The bandwidth ranges from 0.1 Hz to 1 kHz, the gain is 40 dB, the CMRR is greater than 79.4 dB, and the Noise Efficiency Factor (NEF) is 2.7.**

***Index Terms*—Analog integrated circuits, sub-threshold design, EEG, low power, DDA, high CMRR.**

I. Introduction

We present the first stage of a platform for acquiring intracranial EEG (electroencephalography) signals to study epilepsy on rats (see Fig. 1). The bandwidth of interest ranges from 0.1 to 300 Hz, and the signal's amplitude varies between 200 and 400 μV. Given these characteristics, the preamplifier must show low noise and a high Common Mode Rejection Ratio (CMRR). In addition, for long-term experiments, high autonomy is required. Therefore, low power consumption and high current efficiency (low Noise Efficiency Factor, NEF [1]) are also necessary.

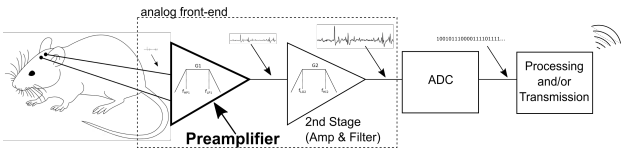

Fig. 1: Top-level schematic of the acquisition system.

[2] presents a neural preamplifier featuring low input noise, high CMRR, and current efficiency. The amplifier improves the performance of capacitive feedback neural amplifiers (i.e., [3]) by taking advantage of the high CMRR achievable in a DDA (Differential Difference Amplifier) without jeopardizing power consumption. In addition, this preamplifier introduced a technique for blocking the input dc voltage. However, [2] implemented this architecture in a 0.5 μm CMOS technology with a voltage supply of 3.3 V. A new version was introduced in [4], enabling a lower voltage supply of 1.2 V in a 130 nm CMOS technology. However, the current consumption turned out to be high (30 μA). In this work, we present a new generation of this architecture, targeting low voltage supply (1.8 V) and low current consumption while keeping a state-of-the-art performance in the other required features.

II. Architecture

In this work, we propose a variant of the architecture proposed in [2] and [4], aiming at low voltage supply (1.8 V), low current consumption, high CMRR, and low NEF. A fully differential version of the original architecture, employing complementary input differential pairs [5], is the main novelty of our proposal (see Fig. 2).

M1, M2, M3, and M4 (complementary input differential pairs) are the input stage of Gm1. The M5-M8 block, jointly with Gmf and C_F, implements an output feedback loop that establishes the high-pass characteristic and blocks the dc input. Gm2 and Gmf are symmetric OTAs (Operational Transconductance Amplifiers, see Fig. 2). The transconductance of Gm1, Gm2, and Gmf are G_{m1}, G_{m2}, and G_{mf}, respectively.

In small-signal operation M6-M7 and M5-M8 can be interpreted as asymmetric differential pairs where α defines the degree of asymmetry. $g_{m7} = \alpha g_{m6}$ and $g_{m8} = \alpha g_{m5}$, where g_{m5}, g_{m6}, g_{m7} and g_{m8} are the transconductance of M5, M6, M7 and M8 respectively. The effect of these transistors in the value of G_{m1} can be observed in Eq. 1.

$$G_{m1} = g_{m1}\frac{\alpha}{1+\alpha}, \tag{1}$$

where g_{m1} is the transconductance of the input transistors of Gm1 (M1, M2, M3, and M4). α is a key parameter that rules the trade-off between the capacity of blocking input dc voltage $V_{IN,dc}$, the high-pass frequency $f_{high-pass}$ accuracy, and the gain value G. We refer the interested reader to [2] for further details on the functioning of this part of the circuit.

Gm2 and Gmf are symmetric OTAs because it is a simple architecture (see Fig. 2), but other alternatives could be considered. Nevertheless, complementary differential pairs like those used in Gm1 are unsuitable for accommodating the input and output ranges of Gm2 and Gmf. Likewise, the savings on power consumption due to using complementary pairs in these blocks has a negligible impact. The transconductance of the input transistors of Gm2 is $g_{m2} = 2K_{G_{m2}}G_{m2}$, where $K_{G_{m2}}$ is the copy factor of the current mirrors of Gm2 (as indicated in Fig. 2). Correspondingly, the transconductance of the input transistors of Gmf is $g_{mf} = 2K_{G_{mf}}G_{mf}$, where $K_{G_{mf}}$ is the copy factor of the current mirrors of Gmf.

We use a standard common-mode feedback (CMFB) circuit [6] to sense the output common-mode level and accordingly adjust the bias current.

If $\alpha \gg 1$ is adopted, the transfer function of Gm1 is as follows (see Fig. 2):

$$i_{o1} \cong G_{m1}.v_{IN} + (g_{m5} + g_{m6}).v_{F1} \tag{2}$$

$$i_{o2} \cong G_{m1}.v_{IN} + (g_{m5} + g_{m6}).v_{F2} \tag{3}$$

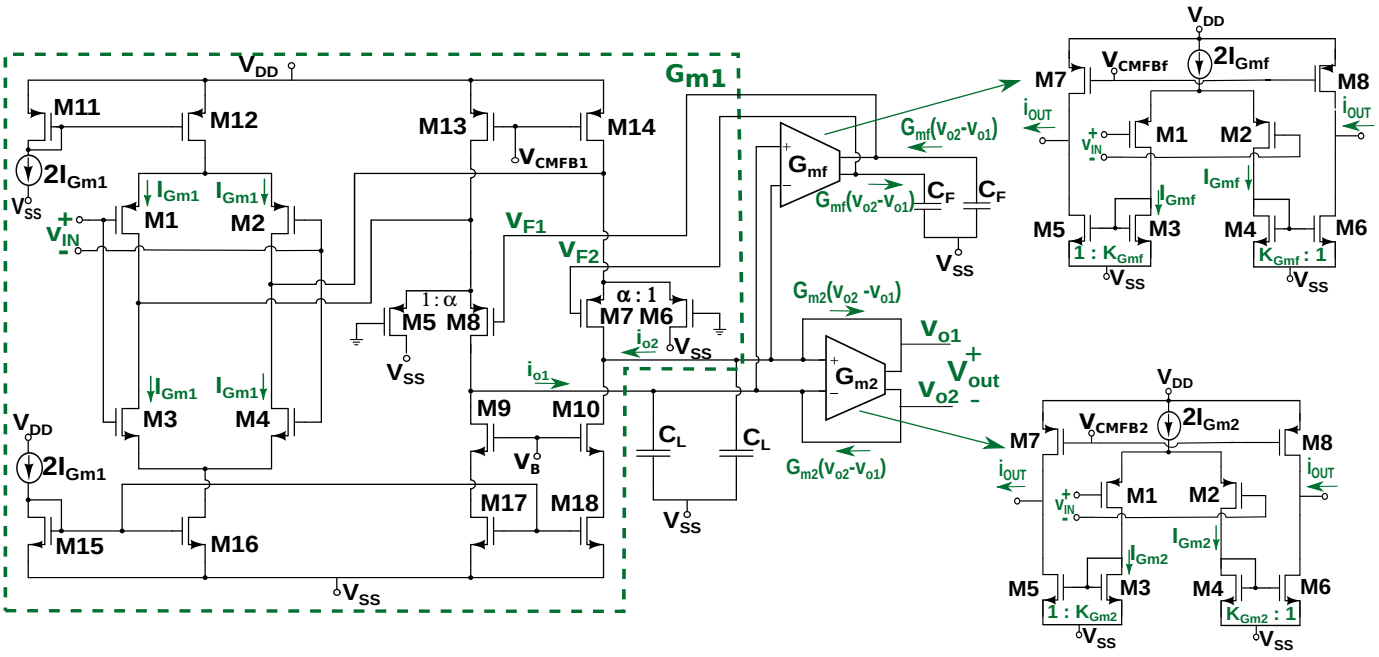

Fig. 2: Preamplifer architecture.

where i_{o1} and i_{o2} are the output currents of Gm1. The transfer function of the circuit depicted in Fig. 2 is:

$$\frac{v_{out}}{v_{in}}(s) = \frac{2\frac{G_{m1}}{C_L}s}{s^2 + 2\frac{G_{out}}{C_L}s + 2\frac{(g_{m5}+g_{m6})G_{mf}}{C_L C_f}} \tag{4}$$

where $G_{out} = G_{out1} + G_{m2}$. The following expressions are good approximations (assuming that poles are separated enough) for the bandpass gain G, given by Eq. 5, the high-pass frequency $f_{high-pass}$, given by Eq. 6, and the low-pass frequency $f_{low-pass}$ given by Eq. 7.

$$G = \frac{G_{m1}}{G_{out}} \tag{5}$$

$$f_{high-pass} = \frac{(g_{m5} + g_{m6})G_{mf}}{2\pi G_{out} C_F} \tag{6}$$

$$f_{low-pass} = \frac{G_{out}}{\pi C_L} \tag{7}$$

III. Implementation

The preamplifier was implemented in a 180 nm FD-SOI CMOS process. According to [2], α = 100 is adopted. Gm1 is the main contributor of noise. Therefore, to reduce thermal noise, the input differential pairs of Gm1 (M1, M2, M3 and M4) were biased in weak inversion [2]. The effect of Flicker noise was reduced by adjusting the size of these transistor (increasing the width W and the length L while keeping the W/L ratio constant, to keep the same inversion level). According to the EEG preamplifer specifications (the gain should be 40 dB, the high-pass frequency 0.1 Hz, and the low-pass frequency 1 kHz) and equations from Section II, the main parameters were determined.

Table I presents the main parameters of the preamplifier. In addition, C_L = 4 pF and C_F = 100 pF were set. On the other hand, V_{DD} = 0.9 V, V_{SS} = -0.9 V, and V_B = -0.4 V were selected.

TABLE I: Preamplifier main parameters.

	Gm1	Gm2	Gmf
$(g_m/I_D)_{InputPair}$	26 V^{-1}	14 V^{-1}	21 V^{-1}
$(g_m)_{InputPair}$	1.5 μS	115.7 nS	5.2 nS
G_m	1.47 μS	14.1 nS	8.8 pS
$(I_D)_{InputPair}$	60 nA	8 nA	0.25 nA
$(W/L)_{InputPair}$	pMOS 250/5	1/20	1/80
	nMOS 200/10	-	-
K_{G_m}	1	4	295
$g_{m5} + g_{m6}$	194 nS	-	-
$(W/L)_5$=$(W/L)_6$	3/15	-	-
$(W/L)_7$=$(W/L)_8$	300/15	-	-

IV. Results

Table II presents results of Monte Carlo simulations (1000 runs). PSRR+ is the positive power supply rejection ratio (V_{DD}), PSRR- refers to the negative power supply rejection ratio (V_{SS}), and THD is the Total Harmonic Distorsion. The simulations correspond to the typical value unless otherwise indicated.

Fig. 3 presents the amplifier frequency response.

TABLE II: Results.

	Result	Obs.
Voltage supply (V)	1.8	-
Gain (dB)	40.0	σ=0.4
$f_{high-pass}$ (Hz)	0.10	σ=0.02
$f_{low-pass}$ (kHz)	1.08	σ=0.04
Supply current (nA)	502	-
Power consumption (nW)	904	-
Input noise (μV_{rms})	3.2	-
NEF	2.7	-
CMRR @ 60 Hz (dB)	79.4	worst-value
Gain w/$V_{IN,dc}$ = 50 mV (dB)	34.5	-
v_{IN} @ THD = 1% (mVpp)	1.12	-
PSRR+ @ 60 Hz (dB)	54.3	worst-value
PSRR- @ 60 Hz (dB)	63.0	worst-value

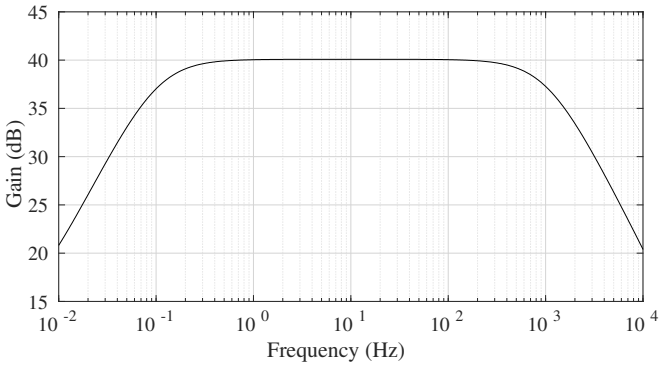

Fig. 3: Frequency response

A. Noise

Fig. 4 presents the Power Spectral Density (PSD) of the input-referred noise. Integration under the solid curve yields to a noise voltage of 3.2 μV_{rms}, where the integration bandwidth was [0.01 Hz-100 kHz].

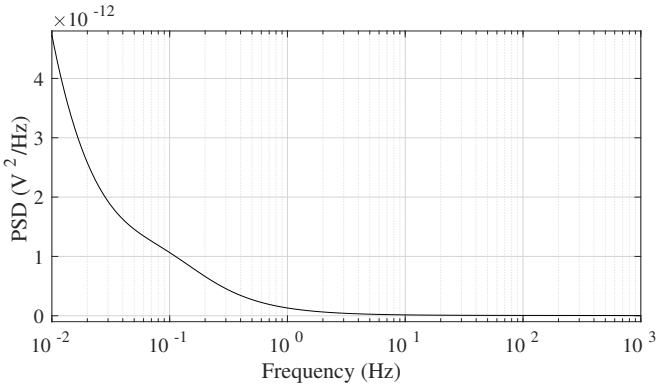

Fig. 4: Input-referred noise power spectral density

B. CMRR

Fig. 5 shows the CMRR Monte Carlo simulations results. The performance is excellent since below 10 kHz the worst-value is always greater than 70 dB, and the mean value is 93.6 dB with σ = 8.8 dB.

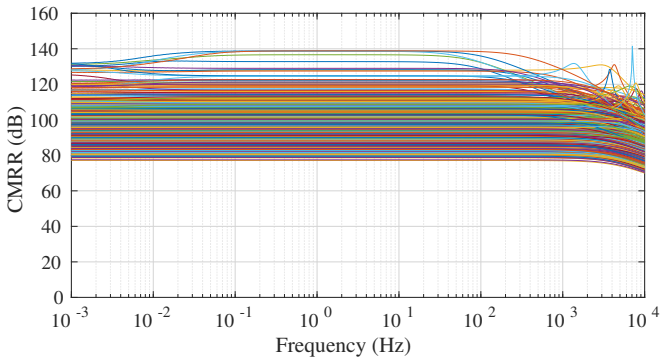

Fig. 5: CMRR

C. Power Consumption

The preamplifier exhibits a remarkable low power consumption of 0.9 μW. Fig. 6 shows its breakdown. As expected, Gm1 is the more demanding block, with more than 90 % (823 nW) of the total power consumption. The Gm1 input pairs consume 216 nW (24 %), the folded-cascoded block 227 nW (25 %), the CMFB block 128 nW (14 %), and auxiliary biasing circuits consume 252 nW (28 %). We did not optimize the power consumption of these biasing circuits so that the overall power consumption could be much reduced.

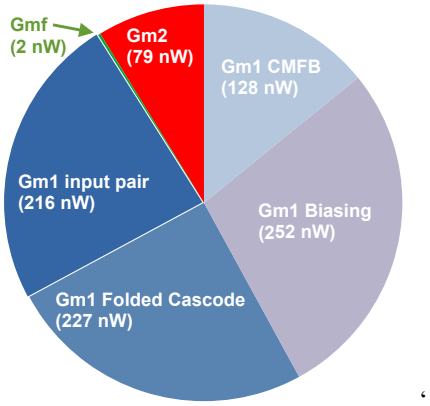

Fig. 6: Power consumption breakdown.

D. State-of-the-art comparison

Table III compares preamplifiers targeting electroencephalography (EEG) and neural applications (where AP stands for Action Potentials and LPF for Local Field Potentials). Our work is among those that report lower power consumption values, while the performance in the other features is outstanding.

V. Conclusions

A 1.8 V supply-voltage preamplifier, suitable for intracranial EEG applications, was designed on a 180 nm FD-SOI CMOS technology.

The results show that the power consumption (0.9 μW) and the current consumption (500 nA) are remarkable low. In addition, the input-referred noise is 3.2 μV_{rms}, the NEF

TABLE III: Comparison with prior work.

	JSSC '03 [3]	JSSC '16 [7]	EMBC '17 [8]	TBCAS '17 [9]	TCAS-I '18 [10]	TBCAS '18 [2]	BioCAS '19 [11]	TCAS-I '20 [12]	TCAS-I '21 [4]	TBCAS '21 [13]	This work*
Technology (μm)	1.5	0.065	0.18	0.35	0.18	0.5	0.18	0.18	0.13	0.18	0.18
V_{DD} (V)	5	1	1	3	1.2	3.3	1.8	1	1.2	1.8	1.8
Power consumption (μW)	80	3.3	2.2	9.6	9.24	28.1	2.36	0.8	35.8	13.7	0.9
Gain (dB)	39.5	52.1	70	46	58	49.2	57.5	40.4	39.3	39.3	40
$f_{low-pass}$ (kHz)	7.2	8.2	1	8.3	0.5	10.3	0.1	5	11.1	5	1
$f_{high-pass}$ (Hz)	25m	1	0.5	0.05	0.5	0.1	0.5	1	19.7	<0.1	0.1
Supply current (μA)	16	3.3	2.2	3.2	7.7	8.5	1.3	0.8	29.8	7.6	0.5
Input noise (μV_{rms})	2.2	4.1	1.2	3.86	1.3	1.9	0.7	4.1	1.3	3.36	3.2
Noise integration bandwidth (Hz)	0.5-50k	1-8.2k	0.5-1k	N/A	N/A	0.03 -25k	0.5-100	200-5k	10-100k	200-10k	0.01 -100k
NEF	4	3.2	2.4	2.8	6.2	2.1	2.8	2	2.5	4.8	2.7
CMRR (dB)	83	80	110	69	100	88	N/A	58	86	84	93.6
$CMRR_{worst-case}$ (dB)	42	46	N/A	N/A	N/A	84	N/A	N/A	69	77	79.4
THD=1% (mV_{pp})	17	1.4	N/A	N/A	>2	0.7	2.1	2.0	0.5	60	1.1
Application	EEG, AP LFP	LFP, AP	EEG	EEG, AP LFP	EEG	EEG, AP LFP	EEG	LFP, AP	LFP, AP	LFP, AP	EEG

Works marked with * presents simulation results

is 2.7, the CMRR is greater than 79.4 dB, the gain is 40 dB, the high-pass frequency is 0.1 Hz, and the low-pass frequency is 1 kHz. These results favorably compare with prior work.

Future work includes the fabrication and complete characterizations of the fabricated chips, including in-vivo validation of the architecture.

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