

# A Compact Lithium-Ion Battery Charger for Low-Power Applications

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**Abstract**—In this work, a linear-based battery charger is proposed, designed, fabricated in a 180 nm SOI process, and measured. The design is aimed to charge low-power wearable or implantable medical devices through a wireless power transfer (WPT) link at a transfer distance of several centimeters, where the available power is in the range of a few milliwatts. A novel self-turn-on/off circuit was implemented, preventing quiescent power consumption while the WPT link is inactive. The compact proposed circuit requires a remarkable low chip area of  $0.023 \text{ mm}^2$ . In measurements, using a 3.7 V (nominal) lithium-ion battery, a configurable charging current from  $500 \text{ } \mu\text{A}$  to 20 mA was achieved, while presenting a competitive efficiency with the state-of-the-art. The automatic transition between the constant current (CC) and constant voltage (CV) charging phases is shown in measurements.

**Index Terms**—Battery charger, lithium-ion (Li-ion) battery, area-efficient, low-power, wireless power transfer

## I. INTRODUCTION

Wireless power transfer (WPT) has proven to be an effective solution to recharge the battery of mobile devices, simplifying the recharge process and relaxing the trade-off between the battery size and the autonomy of the device. This is particularly useful in size-constrained applications such as wearable or implantable medical devices where a wired connection or battery replacement is not feasible. Inductive WPT is the most typically used link type, especially preferred for wearable and implantable medical devices [1]. A block diagram of an inductive WPT link is shown in Fig. 1. In these systems, an alternating current is imposed in the transmitter  $L_{\text{Tx}}-C_{\text{Tx}}$  resonant tank at the resonant frequency. Then, the induced voltage in the  $L_{\text{Rx}}-C_{\text{Rx}}$  resonant receiver is usually rectified and used to charge the battery of the mobile device. The design of the WPT link has been addressed in many previous works [2], [3] and it is out of the scope of this work which is focused on the battery charger design. Most of the commercially available WPT links for active implantable medical devices (AIMDs) require placing the charger over the patient skin, achieving a transfer distance of a few centimeters. In that charging scheme a charging current,  $I_{\text{bat}}$ , of hundreds of milliamperes can be achieved. However, the received power is not as high if the transmission distance is increased to several centimeters. A transmission distance in a range of several centimeters is required to act closer to the target organ

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This work was supported by ANII FMV 1 2017 1 136740 and CSIC Universidad de la República.

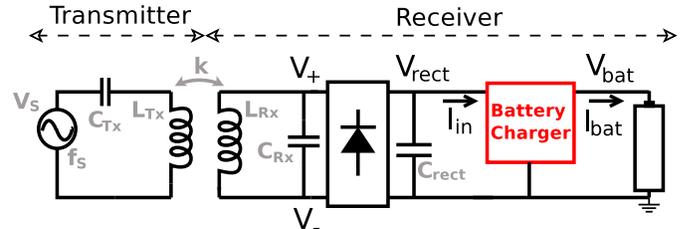


Fig. 1. Block diagram of an inductive WPT link. This work focuses on the battery charger design.

or nerve, or to implement a patient imperceptible charging scheme, e.g., to charge the wearable device or AIMD from behind the bed while the patient is sleeping [4]. In this charging scheme, only a few milliwatts are received [4], however, it is enough for applications such as hearing aid, analog cochlear processor, body-area monitoring, and the promising field of electroceuticals [5], [6].

In these low-power size-constrained applications, the charger has to be power-efficient while delivering a few milliamperes to the battery. Additionally, the charger must be area-efficient, to allow its integration jointly with the other required circuits such as the rectifier and others required by the application.

This paper presents a novel integrated 3.7 V (nominal) lithium-ion battery charger that requires minimal layout-area and achieves high efficiency while delivering a charging current in the milliamperes range. The charging current, during the constant current (CC) phase, can be controlled from  $.5 \text{ mA}$  to 20 mA, to adjust the battery charging rate to the power available through the WPT link. When no power is being received through the WPT link, a novel self-turn-on/off circuit disconnects the battery from the circuit, preventing bias power consumption, until the WPT link is active again, as explained in Section II. Therefore, the proposed battery charger is suitable for low-power size-constrained wireless chargers.

This paper is organized as follows. First in Section II the proposed circuit is introduced. This circuit was fabricated in a 180 nm Silicon On Insulator (SOI) technology from X-Fab Silicon Foundries, and the measurement results are presented in Section III including a comparison with the state-of-the-art. Finally, the main conclusions are drawn in Section IV.

## II. ARCHITECTURE AND CIRCUIT DESIGN

### A. Battery charger design

The battery chargers can be divided into switching-based and linear-based architectures. The linear (also known as low dropout, LDO) architectures are widely used due to their high accuracy, compact layout size, and low noise [7], [8]. Since the input current,  $I_{in}$ , and the output current,  $I_{bat}$ , are almost equal in a linear-based battery charger, the efficiency can be approximated as the ratio between its output and input voltages,

$$\eta = P_{out}/P_{in} = \frac{I_{bat}V_{bat}}{I_{in}V_{rect}} \approx \frac{V_{bat}}{V_{rect}}. \quad (1)$$

Therefore, the main drawback of this architecture is that the larger the voltage drop between  $V_{rect}$  and  $V_{bat}$  the lower the efficiency. On the other hand, the switching-based chargers achieve higher efficiencies but introduce switching noise and require a complex control circuit [7], [8].

One approach to reducing the power loss in the linear-based battery chargers is to control its input voltage, maintaining  $V_{rect}$  as close to  $V_{bat}$  as possible.

On one hand, this control can be implemented using a switching-based DC-DC converter placed between the rectifier and the linear-based battery charger, thus combining the advantages of these two methods [9]. This method to control  $V_{rect}$  makes the receiver circuits more complex which is not desired in this work where a compact circuit is pursued.

On the other hand, if the charging current,  $I_{bat}$ , is below the maximum battery charging current, the  $V_{rect}$  could be reduced by simply increasing  $I_{bat}$  and thus charging the battery faster, without requiring an extra complex circuit. This is the approach taken in this work, where the charging current can be configured in a wide range, from .5 mA to 20 mA, as shown later. Additionally, if the charging current is at the maximum battery charging rate,  $V_{rect}$  could be adjusted by modifying the transmitter output power [8]. Although this method requires back telemetry, this data link is usually required by the type of applications that this work is aimed for.

Although the  $V_{rect}$  regulation is out of the scope of this work, this is discussed to justify the selected charger architecture. For the target application, the linear-based architecture was selected due to its compact layout size and low ripple. The proposed circuit achieves a wide charging current range to allow the adjustment of the battery charging rate to the power available through the WPT link.

The proposed battery charger, shown in Fig. 2, is a compact and minimal version of the widely used linear-based chargers [8], [10], [11]. It is able to implement the well-known constant current (CC) and constant voltage (CV) charging phases, required to charge a lithium-ion battery. In this section the  $\overline{EN}$  signal is assumed at ground, thus M5 is on. The  $\overline{EN}$  signal generation is discussed in the next section II-B.

During the CC phase, the charging current is controlled by the control voltage  $V_{cont}$  (from off the chip). During this phase, M4 operates in triode region with low on resistance, and  $V_{cont}$  is copied to the R1 terminal by the OTA1 (virtual short), thus the current through the M1-M3-M4 branch,  $I_{mirror}$ , is  $V_{cont}/180 \text{ k}\Omega$ . The charging current,  $I_{bat}$ , is 1000 times

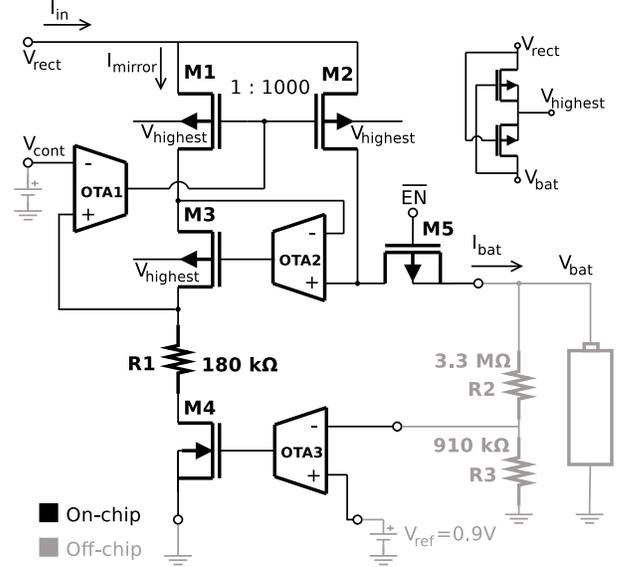


Fig. 2. Proposed linear-based battery charger.

higher than  $I_{mirror}$ , due to the M1-M2 mirror copy ratio. The OTA2 and M3 hold the M1 and M2 drains at the same voltage, reducing the current copy error. When the battery reaches its charge voltage (4.2 V in this case), the CV phase begins, where the charging current is gradually decreased. The CV phase is implemented by OTA3 and M4. When  $V_{bat}$  reaches the charging voltage (4.2 V) the inverting input of OTA3,  $V_{bat} \frac{R3}{R3+R2}$ , begins to surpass the non-inverting input,  $V_{ref}$ , thus the gate voltage of M4 begins to go down. Therefore, the on-resistance of M4 is increased, reducing  $I_{mirror}$  and thus  $I_{bat}$ , limiting  $V_{bat}$  to the charging voltage during the CV phase.

All the OTAs (operational transconductance amplifiers), are simply Miller OTAs, and are powered from  $V_{rect}$ . They were designed following the gm/ID methodology [12], minimizing layout area and power consumption while keeping the offset below 10 mV. The OTA1 and OTA3 have a PMOS input, while OTA2 has an NMOS input since its input voltage,  $V_{bat}$ , approaches the supply voltage during the CV phase.

Layout matching techniques were used to minimize the impact of mismatch and process variations. In the proposed architecture, MOS variations generate a fairly imperceptible impact compared to the variation of the R1 resistor in Fig. 2, which directly impacts the charging current. For instance, based on corner simulations, at  $V_{cont} = 360 \text{ mV}$  (target  $I_{bat} = 2 \text{ mA}$ ), the MOS variations generate less than  $20 \mu\text{A}$  shift, while the resistor variation could generate up to  $\pm 350 \mu\text{A}$  shift. The on chip generation of  $V_{cont}$  is part of future work. The R1 related spread can be mitigated through the inclusion of a replica of R1 in the circuit that generates  $V_{cont}$ .

### B. Self-turn-on/off circuit design

As explained in the previous subsection, all the OTAs used in the battery charger circuit are powered from the rectifier output node,  $V_{rect}$ . When no wireless power is being received,  $V_{rect}$  could drop below  $V_{bat}$ , causing a reverse current through the charger, from the battery back to the output node of the

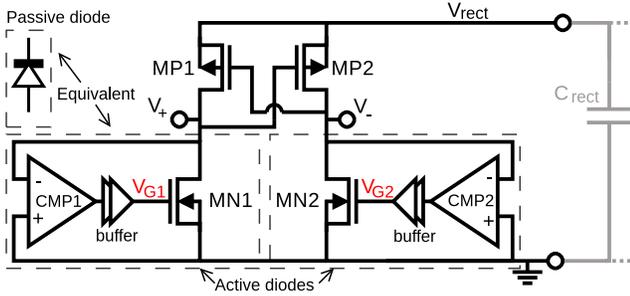


Fig. 3. PMOS cross-coupled active rectifier [17].

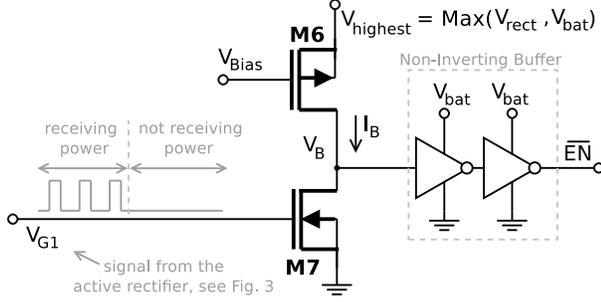


Fig. 4. Proposed self-turn-on/off circuit that generates the charger enable signal,  $\overline{EN}$ .

rectifier. If that happens, the battery will provide the bias power of all the circuits powered from  $V_{rect}$  while the wireless link is inactive. That quiescent power consumption from the battery is unnecessary, since the battery charger circuit could be powered off while the WPT link is inactive. Therefore, a self-turn-on/off circuit was proposed which generates the enable signal,  $\overline{EN}$ , turning on and off transistor M5, see Fig. 2, in order to disconnect the battery while the WPT link is inactive, thus preventing any quiescent consumption.

The proposed self-turn-on/off circuit takes advantage of the gate drive signals that are generated by the active rectifier. Instead of using diodes, an active rectifier uses MOS switches that are turned on and off by voltage comparators, behaving as a near-zero threshold voltage diode, reducing the forward voltage drop and thus increasing the power conversion efficiency of the rectifier [8], [9], [13]–[16]. In this work the PMOS cross-coupled active rectifier depicted in Fig. 3 was selected, which is widely used in the literature for this kind of application [8], [13]–[15], [17].

The design of the rectifier is out of the scope of this paper, but its architecture is introduced as the gate drive signals,  $V_{G1}$  and  $V_{G2}$  (Fig. 3), are used by the proposed self-turn-on/off circuit. The  $V_{G1}$  and  $V_{G2}$  signals only have pulses while the rectifier is delivering power to the output node [8], [13]–[15], which indicates that the inductive link is active. Therefore, the proposed self-turn-on/off circuit, shown in Fig. 4, uses one of these signals ( $V_{G1}$ ) to generate the enable signal,  $\overline{EN}$ , as explained next.

While power is being received, M7 (Fig. 4) is periodically turned on by the  $V_{G1}$  signal, at the WPT carrier frequency, discharging the  $V_B$  node to ground. When no power is being received,  $V_{G1}$  remains at low level, and the node  $V_B$  is charged by the bias current  $I_B$ , rising  $\overline{EN}$  and thus disconnecting the

TABLE I  
TRANSISTORS SIZE

	M1 <sup>A</sup>	M2 <sup>B</sup>	M3	M4	M5	M6	M7
W ( $\mu\text{m}$ )	5	500	20	20	200	.22	.22
L ( $\mu\text{m}$ )	5	.5	.5	1	.5	50	.5

A: 10 PMOS in series with  $L=500$  nm. B: 100 PMOS in parallel with  $W=5$   $\mu\text{m}$

battery from the charging circuit. Since the  $V_{Bias}$  of M6 is generated from  $V_{rect}$ , as all the bias,  $V_{Bias}$  will drop to ground after disconnecting the battery, increasing  $I_B$  and speeding up the end of the  $V_B$  charging process. Then, when the WPT link is active again,  $V_{rect}$  rises restoring the bias voltages, and the switching signal,  $V_{G1}$ , discharges  $V_B$  through M7, enabling the charger again. It is worth mentioning that the self-turn-on/off circuit does not consume quiescent power from the battery (except for leakage currents) while the WPT link is inactive since M7 remains off until the WPT link is restored.

The highest voltage of this circuit can be either the battery voltage,  $V_{bat}$ , or the rectifier output voltage,  $V_{rect}$ , depending on whether the WPT link is active. This highest voltage is usually required by the PMOS substrates and pad ring. To obtain the highest voltage between  $V_{rect}$  and  $V_{bat}$ , referred to as  $V_{highest}$ , the PMOS cross-coupled circuit shown in Fig. 2 was included, widely used for dynamic body voltage control [8].

The proposed charger was designed and fabricated jointly with the active rectifier in a 180 nm SOI technology from X-Fab, the transistors sizes are summarized in Table I. Measurement results are presented in the next section, proving the circuit performance and comparing it with the state-of-the-art.

### III. MEASUREMENT RESULTS

A micrograph of the fabricated chip is shown in Fig. 5. Since the top layer metals were not used, our circuit is hidden by the autofill, thus a layout picture was also included indicating the circuit size.

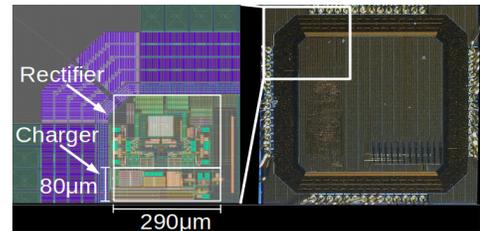


Fig. 5. Fabricated chip layout and micrograph, 180 nm SOI X-Fab technology.

To validate the circuit design, a  $9 \times 10 \times 3$  mm<sup>3</sup>, 3.7 V (nominal), battery from Guangzhou Markyn Battery Co., Ltd was charged. The measurement setup and a connection diagram are shown in Fig. 6. The charging current for this experiment was set to 2 mA ( $V_{cont} = 360$  mV). The selected battery has an effective measured capacity of 8 mAh, thus it is being charged at a 0.25C rate. This charging current is compatible with a WPT link charging a wearable or implantable device in the centimeter range [4], as discussed in the introduction.

The measured charging profile is presented in Fig. 7. The proposed circuit holds the desired constant charging current during the CC charging phase, and automatically switches to the CV phase when the battery reaches the charging voltage.

TABLE II  
PERFORMANCE COMPARISON

	[18]	[19]	[20]	[11]	[16]	[21]	This Work
Technology	0.35 $\mu\text{m}$	0.6 $\mu\text{m}$	180 nm	0.35 $\mu\text{m}$	180 nm	0.5 $\mu\text{m}$	180 nm
Charger Type	Digitally-controlled	LDO	LDO	LDO	Switched	LDO	LDO
Battery Capacity	3400 mA	n/a	n/a	80 mA	n/a	8 mAh	8 mAh
Charge Voltage	4.2 V	4.2 V	4.2 V	4.2 V	1.0-1.2 V	4.2 V	4.2 V
Charge Current at $V_{\text{rect}}$	600mA	1.5mA	1 - 6.8 mA	25 mA	$\approx 1.5 - 50$ mA	3 mA	0.5 - 20 mA
Peak Efficiency	n/a	95 %	98 %	94 %	AC input	4.3 V	4.3 - 5.5 V
Average Efficiency	79 %	n/a	n/a	88 %	84.7 %	89.7 %	89 % <sup>A</sup>
Max. Quiescent Current	n/a	n/a	< 151 nA	58 $\mu\text{A}$ <sup>B</sup>	n/a	n/a	< 1 $\mu\text{A}$ <sup>C</sup>
Chip Area	0.77 mm <sup>2</sup>	1.74 mm <sup>2</sup>	0.13 mm <sup>2</sup>	2.09 mm <sup>2</sup>	0.22 mm <sup>2</sup>	0.16 mm <sup>2</sup>	0.023 mm <sup>2</sup>

- A: at  $V_{\text{rect}} = 4.4$  V and  $I_{\text{bat}} = 2$  mA • B:  $I_{\text{mirror}}=25$   $\mu\text{A}$ ,  $I_{\text{bias}}=33$   $\mu\text{A}$  • C: plus  $I_{\text{mirror}} = I_{\text{bat}}/1000$ , but it is turned off while the WPT link is inactive.

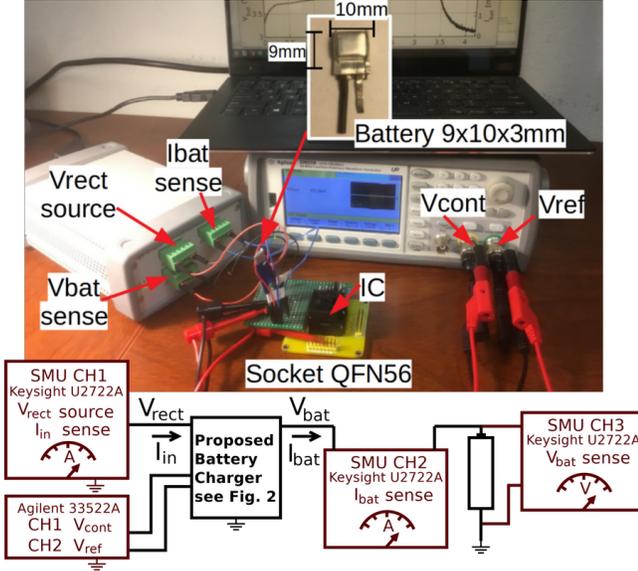


Fig. 6. Experimental setup: picture and block diagram.

During the CV, the battery voltage,  $V_{\text{bat}}$ , is tightly compared against the reference, reducing the charging current accordingly to hold a constant battery voltage. During that phase, slight variations in  $V_{\text{bat}}$  (tens of millivolts, not perceptible in Fig. 7) generate the observed fluctuations in the charger output current. The charger input current is only 3  $\mu\text{A}$  greater than the output current, as 2  $\mu\text{A}$  are consumed by the current mirror ( $I_{\text{mirror}} = I_{\text{bat}}/1000 = 2$   $\mu\text{A}$ ), and approximately 1  $\mu\text{A}$  is being consumed by the OTAs. Therefore, the charger efficiency (1), can be approximated by the ratio between the output and input voltages. During this experiment  $V_{\text{rect}}$  was fixed at 4.4 V, obtaining a measured maximum efficiency of 93 % and an average efficiency of 89 % during the whole charging process. The minimum required  $V_{\text{rect}}$  depends on the selected charging current and the battery voltage which ranges from  $\approx 3.3$  V to  $\approx 4.2$  V during the charging process. Figure 8 shows the charger output current during the CC phase (@  $V_{\text{bat}} = 3.7$  V) as a function of the control voltage for different values of  $V_{\text{rect}} = \{4.3, 4.5, 5.0, 5.5\}$  V. As can be seen, the circuit is able to deliver a charging current between 500  $\mu\text{A}$  and 20 mA. The greater the target charging current is, the higher  $V_{\text{rect}}$  should be to prevent an error between the target and effective charging current. The charger efficiency was not reported in Fig. 8 for the sake of simplicity, however, it can be estimated from (1)

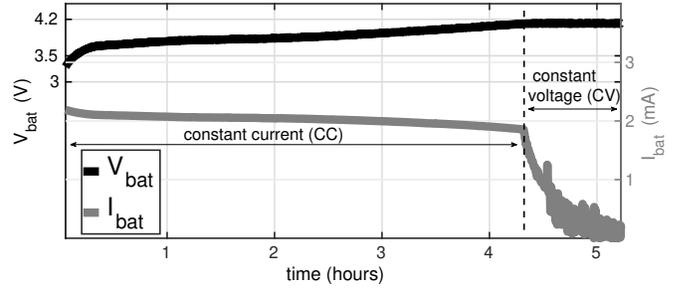


Fig. 7. Measurement results of the CC/CV charging profile of a battery with 8 mAh, 3.7 V (nominal), and 4.2 V (charging voltage). This experiment was at  $V_{\text{rect}} = 4.4$  V and  $V_{\text{cont}} = 360$  mV (in CC  $I_{\text{bat}} = V_{\text{cont}}/180 = 2$  mA).

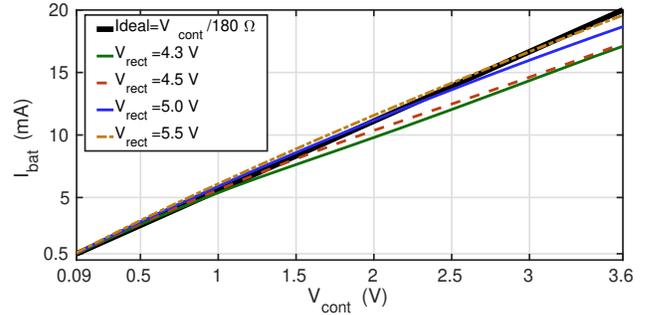


Fig. 8. Measured charging current,  $I_{\text{bat}}$ , as a function of the control voltage,  $V_{\text{cont}}$ , at  $V_{\text{bat}} = 3.7$  V. The ideal curve is compared with measured results for four values of  $V_{\text{rect}}$ .

as the  $1 \mu\text{A} + I_{\text{bat}}/1000$  quiescent consumption (OTAs+mirror) is negligible, thus  $I_{\text{in}} \approx I_{\text{bat}}$ .

The self-turn-on/off circuit was also experimentally validated by measuring the generated enable signal,  $\overline{EN}$ , at the beginning and end of the wireless charging process, Fig. 9. To do so, the rectifier and a test WPT link were included in the measurement setup. When the WPT starts, a voltage is induced in the receiver coil at nodes  $V_+$  and  $V_-$ , see figures 1 and 3. In Fig. 9, the measured  $V_+$  was included over the enable signal to indicate the WPT link status. As shown in Fig. 9a, at the beginning of the charging process the self-turn-on circuit responds very fast, switching the  $\overline{EN}$  signal in around 200 ns. As explained in Section II-B, during the self-turn-off, the bias current  $I_B$  has to charge the node  $V_B$ , see Fig. 4, which requires more time than the turn-on transition. Figure 9b shows the measured turn-off delay, which is 11.53  $\mu\text{s}$ . Since the

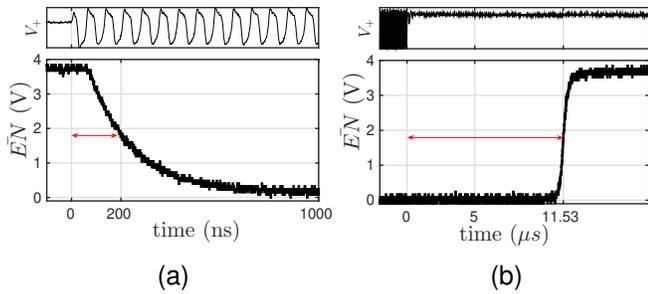


Fig. 9. Enable signal,  $\overline{EN}$ , at the beginning (a) and end (b) of the wireless charging process.

goal of the self-turn-on/off circuit is to prevent bias power consumption while the WPT link is inactive, this short delay ( $11.53 \mu\text{s}$ ) is not a problem from the energy savings point of view, and it prevents an undesired circuit turn-off in case of a short interruption in the WPT link.

To quantify the energy saving thanks to the self-turn-on/off circuit while the WPT link is inactive, the quiescent power consumption from the battery was measured connecting  $\overline{EN}$  to ground and disabling the self-turn-on/off circuit. If the battery is not disconnected while the WPT link is inactive,  $5.3 \mu\text{A}$  (measured) quiescent current is consumed. That consumption corresponds to: 1) the bias consumption of the battery charger's OTAs ( $\approx 1 \mu\text{A}$ ), 2) other on-chip circuits such as the bias voltage generator, rectifier comparators, and rectifier on/off delay compensation circuits ( $\approx 3.4 \mu\text{A}$ ), and 3) the off-chip voltage divider shown on Fig. 2 ( $\approx 879 \text{ nA}$ ). When the self-turn-on/off circuit is used, the on-chip quiescent consumption is eliminated and only the voltage divider consumption ( $\approx 879 \text{ nA}$ ) remains. It is worth mentioning that the same enable signal provided by the proposed circuit could be used to turn on/off other off-chip circuits such as the voltage divider.

The performance is compared with the state-of-the-art in Table II. As can be seen, the proposed circuit presents a competitive efficiency, is able to deliver a wide range of charging currents, and requires a remarkable low area, allowing its integration jointly with the other required circuits in a size-constrained application.

#### IV. CONCLUSION

An integrated lithium-ion battery charger was proposed, designed, and fabricated in a 180 nm SOI technology from X-Fab. The design was aimed to charge low-power wearable or implantable medical devices wirelessly in the centimeter range. A linear-based architecture was selected and a novel self-turn-on/off circuit was included, preventing quiescent power consumption from the battery while the WPT link is inactive. The compact and minimal design requires a remarkably low area of  $0.023 \text{ mm}^2$ . The measured efficiency is competitive with the state-of-the-art, and a wide charging current range from  $500 \mu\text{A}$  ( $\approx 1.85 \text{ mW}$ ) to  $20 \text{ mA}$  ( $\approx 74 \text{ mW}$ ) was obtained. Additionally, a commercial battery was charged, showing in measurements the CC and CV charging phases and their automatic transition.

#### REFERENCES

- [1] T. Sun, X. Xie, and Z. Wang, *Wireless power transfer for medical microsystems*. Springer, 2013.
- [2] P. Pérez-Nicoli, *Inductive Links for Wireless Power Transfer: Fundamental Concepts for Designing High-Efficiency Wireless Power Transfer Links*. Springer Nature, 2021.
- [3] M. Kiani and M. Ghovanloo, "The circuit theory behind coupled-mode magnetic resonance-based wireless power transmission," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 59, no. 9, pp. 2065–2074, 2012.
- [4] P. Pérez-Nicoli, M. Sivoletta, N. Gammarano, and F. Silveira, "Limits for increasing the WPT distance in AIMDs," in *2020 XXXIIIrd General Assembly and Scientific Symposium of the International Union of Radio Science*. IEEE, 2020, pp. 1–4.
- [5] A. P. Chandrakasan, N. Verma, and D. C. Daly, "Ultralow-power electronics for biomedical applications," *Annu. Rev. Biomed. Eng.*, vol. 10, pp. 247–274, 2008.
- [6] A. Majid, *Electroceuticals*. Springer, 2017.
- [7] S. Roy, A. Wasekul, S. Baidya, and F. H. Khan, "A comprehensive review on rectifiers, linear regulators and switched-mode power processing techniques for biomedical sensors and implants utilizing in-body energy harvesting and external power delivery," *IEEE Transactions on Power Electronics*, 2021.
- [8] C.-Y. Wu, S.-H. Wang, and L.-Y. Tang, "CMOS high-efficiency wireless battery charging system with global power control through backward data telemetry for implantable medical devices," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 67, no. 12, pp. 5624–5635, 2020.
- [9] Y.-C. Chu, N. S. Artan, D. Czarkowski, and H. J. Chao, "A new single-stage AC-DC converter for medical implant devices," in *2013 IEEE International Symposium on Circuits and Systems (ISCAS)*. IEEE, 2013, pp. 2948–2951.
- [10] *Monolithic Linear Lithium-Ion Battery Charger With Thermal Regulation*, LTC1733, Linear Technology, 2001.
- [11] K. Noh, M. Zhang, and E. Sánchez-Sinencio, "A unified amplifier-based CC-CV linear charger for energy-constrained low-power applications," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 66, no. 3, pp. 377–381, 2018.
- [12] F. Silveira, D. Flandre, and P. G. Jespers, "A gm/ID based methodology for the design of CMOS analog circuits and its application to the synthesis of a silicon-on-insulator micropower OTA," *IEEE journal of solid-state circuits*, vol. 31, no. 9, pp. 1314–1319, 1996.
- [13] L. Cheng, W.-H. Ki, Y. Lu, and T.-S. Yim, "Adaptive on/off delay-compensated active rectifiers for wireless power transfer systems," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 3, pp. 712–723, 2016.
- [14] C. Huang, T. Kawajiri, and H. Ishikuro, "A near-optimum 13.56 MHz CMOS active rectifier with circuit-delay real-time calibrations for high-current biomedical implants," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 8, pp. 1797–1809, 2016.
- [15] S. Pal and W.-H. Ki, "40.68 MHz digital on/off delay-compensated active rectifier for WPT of biomedical applications," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 67, no. 12, pp. 3307–3311, 2020.
- [16] S.-H. Lee, J.-S. Bang, K.-S. Yoon, H.-D. Gwon, S.-W. Kim, I.-K. Cho, S.-W. Hong, and G.-H. Cho, "Voltage-boosted current-mode wireless power receiver for directly charging a low-voltage battery in implantable medical systems," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 11, pp. 8860–8865, 2018.
- [17] P. Pérez-Nicoli, F. Veirano, and F. Silveira, "Comparator with self controlled delay for active rectifiers in inductive powering," in *2018 IEEE Wireless Power Transfer Conference (WPTC)*, 2018, pp. 1–4.
- [18] S.-Y. Lin and T.-H. Lin, "An area-efficient amplifier-less digitally-controlled li-ion battery charger in  $0.35 \mu\text{m}$  CMOS," in *2017 IEEE Asian Solid-State Circuits Conference (A-SSCC)*. IEEE, 2017, pp. 37–40.
- [19] P. Li and R. Bashirullah, "A wireless power interface for rechargeable battery operated medical implants," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 54, no. 10, pp. 912–916, 2007.
- [20] T. Ozaki, T. Hirose, H. Asano, N. Kuroki, and M. Numa, "Ultralow-quiescent-current and wide-load-range low-dropout linear regulator with self-biasing technique for micropower battery management," *Japanese Journal of Applied Physics*, vol. 56, no. 4S, p. 04CF11, 2017.
- [21] B. Do Valle, C. T. Wentz, and R. Sarpeshkar, "An area and power-efficient analog li-ion battery charger circuit," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 5, no. 2, pp. 131–137, 2011.