Minimum Supply Voltage of 2.45 GHz LC Oscillator in 28 nm FD-SOI Process

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***Abstract*—The minimum supply voltage limit is studied in the case of a 2.45 GHz LC cross-coupled oscillator, in a 28 nm FD-SOI technology. An approach with simple equations aided with look up tables is used to obtain a theoretical prediction of the minimum voltage and current required for operation. The look up tables are loaded with all the transistor parameters of interest, which are extracted by means of DC simulations. The prediction is in good agreement with the simulation results, as long as the transition frequency of the transistors is at least 10 times the oscillation frequency. A feasible supply voltage for this circuit topology, oscillation frequency and technology is shown to be 37 mV. Depending on the back-plane voltage value and the inductor selected, the supply voltage reduction is limited by either the parasitic capacitances or the intrinsic gain of the transistors. Equations are provided to aid the designer in the selection of all of the design parameters to achieve the lowest possible supply voltage and lowest possible current.**

***Index Terms*—Ultra-Low Voltage, Low-Power Electronics, RF, FD-SOI**

I. Introduction

Supplying energy to a device may entail very restrictive voltage and power constraints. Thermal or electrochemical harvesting devices provide very low voltages of the order of $100\,\mathrm{mV}$ or even lower [1]–[3]. Furthermore, if the operation of circuits at those supply voltage levels is feasible this makes possible important reductions in consumed power and energy.

Here we target a cross-coupled LC oscillator that operates at $2.45\,\mathrm{GHz}$, the center frequency of the $2.4\,\mathrm{GHz}$ Industrial, Scientific and Medical (ISM) radio band. This radio band is one of the most used RF frequency bands worldwide, as protocols like Wi-Fi, Bluetooth and IEEE 802.15.4 work in that band.

The oscillator is simulated in a $28\,\mathrm{nm}$ FD-SOI process. As the nanometer processes are complex to model, we use an approach based on analytic calculations and lookup tables (LUTs) [4], [5]. Thus, the complexity, in particular the short channel effects, are dealt with by using different LUTs depending on the target transistor size.

The oscillators in the range of GHz with lowest supply voltage operate from supplies as low as 0.35 to $0.41\,\mathrm{V}$ [6]–[8]. Here, the minimum supply voltage limit is studied, showing that it can be much further reduced and explaining what are the constraints to do so. As a result, guidelines are provided to achieve the lowest supply voltage possible, as well as an accurate estimation of the minimum current consumption required.

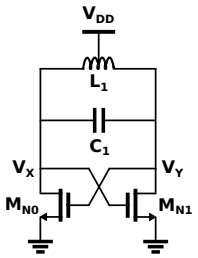

Fig. 1. Circuit schematic of an LC cross-coupled oscillator.

II. Study of the minimum operating voltage limit

The minimum supply voltage to enable oscillation is studied herein in the case of an LC cross-coupled oscillator. Figure 1 shows the circuit schematic of such oscillator. Each transistor introduces $180°$ shift, so two transistors suffice for oscillation [9].

This voltage biased topology is more suitable for ultra low voltage operation than a current biased topology, since the transistors in the tail current source would not saturate. In addition, the voltage biased topology is useful in the ultra low voltage context, since the circuit is only connected to the supply voltage, V_{DD}, through the inductor. Therefore, full advantage is taken from the DC voltage by supplying it directly to the transistors and having an output that may swing well above V_{DD} [10].

The inductor L_1 and the capacitor C_1 can be considered as two separate inductors $L_1/2$ and two separate capacitors $2C_1$ in series respectively. In both cases, the middle node is connected to virtual signal ground due to the circuit's symmetry. The oscillation angular frequency is $\omega_{osc} = 1/\sqrt{L_1 C_1}$. At the oscillation frequency, the open-loop gain is

$$A_{ol}\left(j\omega_{osc}\right) = \left(\frac{g_m}{\frac{2}{R_P} + g_o}\right)^2, \tag{1}$$

where R_P is the inductor L_1 parallel resistance at the oscillation frequency and g_m and g_o are the transconductance and the output conductance of either transistor, respectively. Both are calculated around the DC operating point $V_X = V_Y = V_{DD}$. The Barkhausen oscillation condition reduces to

$$g_m \geq \frac{2}{R_P} + g_o. \tag{2}$$

The oscillation condition does not depend explicitly on the supply voltage, but through the parameters g_m and g_o which depend on the bias voltage.

(2) simplifies to a condition on the drain current

$$I_D \geq \frac{\frac{2}{R_P}}{\frac{g_m}{I_D} - \frac{g_o}{I_D}}, \tag{3}$$

where g_m/I_D and g_o/I_D are looked up in a table. This lookup table (LUT) must be filled in advance by means of DC simulations of a unitary transistor.

A. Design of the transistors

The lvtnfet_rf devices are the nMOS transistors of choice, since these have a lower threshold voltage than the standard nfet and are characterized for RF operation.

To minimize the capacitance contribution, the minimum channel length $L = 30\,\mathrm{nm}$ is used (following some of the suggestions in Section 8.8 of [9]).

Both transistors are implemented with N fingers of width $W_u = 206\,\mathrm{nm}$. Thus, the total width is $W = N \times W_u$. This allows the designer to extract the LUT only in the case of a transistor of $L = 30\,\mathrm{nm}$ and $W_u = 206\,\mathrm{nm}$. Then the designer can obtain in a simple way the parameters of a transistor with N fingers, by means of multiplying by N.

Thus, the values in the LUT are loaded for $L = 30\,\mathrm{nm}$, $W_u = 206\,\mathrm{nm}$ and the values of V_{DD} and back plane voltage V_{BP} of interest, provided that in DC $V_{GS} = V_{DS} = V_{DD}$.

As a consequence,

$$I_D = N \times I_{D\,u}, \tag{4}$$

where $I_{D\,u}$ is the drain current through a single finger. From (3) and (4), it follows that there is a minimum number of fingers N required for oscillation at $2.45\,\mathrm{GHz}$, given by

$$N_{min} = \left(\frac{1}{I_{D\,u}}\right)\left(\frac{\frac{2}{R_P}}{\frac{g_m}{I_D} - \frac{g_o}{I_D}}\right). \tag{5}$$

Note that $N \geq 0$ if $g_m/I_D > g_o/I_D$. Then, $g_m/g_o > 1$, which sets a lower boundary for the intrinsic gain of the transistor.

B. Inductor choice

The inductor that achieves the lowest losses at the operating frequency must be used to reduce the power consumption of the oscillator. This is because the active devices of the oscillator must compensate for the losses of the LC tank and because the inductor is the most lossy part of the tank in integrated technologies.

There are four kinds of inductors available in the library. The achievable inductance values using the single turn coils are in the range from $0.091\,\mathrm{nH}$ to $1.2\,\mathrm{nH}$, while using the multi turn coils the achievable values are in the range from $0.61\,\mathrm{nH}$ to $7.76\,\mathrm{nH}$. These two kinds (single and multi turn coils) have their differential and non-differential version. Here the multi turn coils are chosen, to use higher values of inductors that achieve a higher quality factor Q. The differential coils are chosen to keep the circuit symmetric.

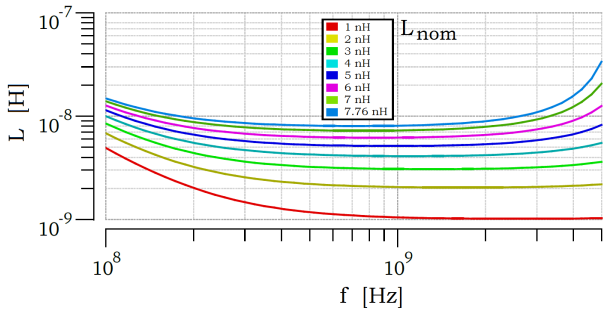

Fig. 2. Inductance value L_1 as a function of frequency of a given inductor in the library with $11\,\mu\mathrm{m}$ coil width.

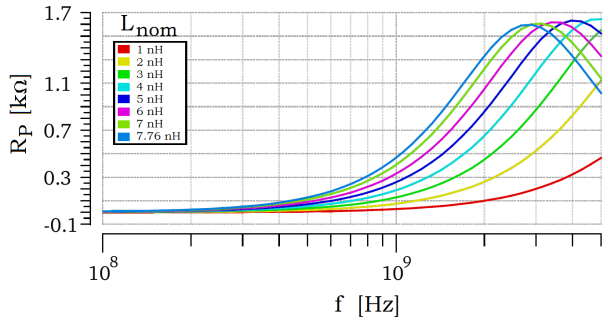

Fig. 3. Parasitic parallel resistor R_P as a function of frequency of a given inductor of the library with $11\,\mu\mathrm{m}$ coil width.

The parameters of the inductors in the library were extracted for several values of the intended nominal inductance. The equivalent parallel resistance is extracted as $R_P = 1/\operatorname{Re}(Y_{L_1})$, the inductance value is extracted as $L_1 = -1/(2\pi f \operatorname{Im}(Y_{L_1}))$ and $Q = R_P/(2\pi f L_1)$. The results are plotted in Figs. 2 to 4, as a function of frequency.

The coil width used in these simulations is $11\,\mu\mathrm{m}$. Moreover, the dependence of the coil parameters on its width is negligible, according to simulations (omitted here).

According to (3), the highest R_P the lowest the minimum I_D. The maximum value of R_P diminishes with frequency, as seen in Fig. 3. Therefore, the $L_{nom} = 7.76\,\mathrm{nH}$ nominal inductor is selected because it has the lowest losses at $2.45\,\mathrm{GHz}$, which correspond to the highest $R_P = 1.6\,\mathrm{k\Omega}$ and

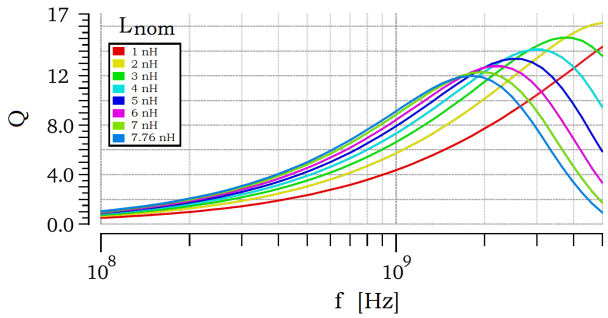

Fig. 4. Quality factor Q as a function of frequency of a given inductor of the library with $11\,\mu\mathrm{m}$ coil width.

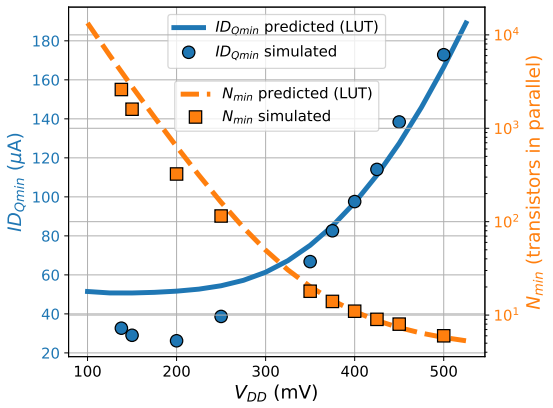

Fig. 5. The minimum current and number of transistors in parallel for oscillation at 2.45 GHz as a function of V_{DD} for $V_{BP} = 0\,\text{V}$. Simulation results and results predicted by (3) and (5) and the LUT.

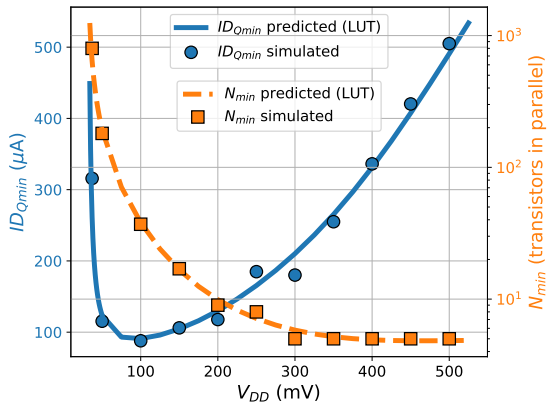

Fig. 6. The minimum current and number of transistors in parallel for oscillation at 2.45 GHz as a function of V_{DD} for $V_{BP} = 3\,\text{V}$. Simulation results and results predicted by (3) and (5) and the LUT.

$L_1 = 9.63\,\text{nH}$. Note that the 7.76 nH nominal inductor is not the highest Q inductor, according to Fig. 4.

III. Methodology

Given V_{DD} and V_{BP}, the minimum current to enable oscillation can be obtained by means of following (3) together with the LUT (g_m/I_D and g_o/I_D).

The oscillator simulated includes the 7.76 nH nominal inductor selected in Section II-B, an ideal capacitor C_1 to match the oscillation frequency to 2.45 GHz and two identical parallel arrangements of N transistors of $L = 30\,\text{nm}$ and $W_u = 206\,\text{nm}$.

For each value of V_{DD} and V_{BP} of interest, N and C_1 are modified to obtain, through periodic steady-state (PSS) simulations, the minimum N for oscillation at 2.45 GHz. Thus, obtaining the minimum I_D.

Finally, the simulation results of I_D are compared to the boundary predicted by (3) together with the LUT.

IV. Results

The current through the transistors I_D and the number of fingers N, are compared to those predicted by (3) and (5), respectively, and the LUT. The results are shown in Fig. 5 for $V_{BP} = 0\,\text{V}$ and in Fig. 6 for $V_{BP} = 3\,\text{V}$.

On the one hand, the simulation results for $V_{BP} = 3\,\text{V}$ are well predicted for all the values of V_{DD}.

On the other hand, the results for $V_{BP} = 0\,\text{V}$ show that the prediction is good for $V_{DD} \geq 275\,\text{mV}$ and it worsens as V_{DD} decreases. In order to understand up to what extent is it possible to make these predictions, the transition frequency f_T of the transistors is included in the LUT. Figure 7 shows how f_T depends on V_{BP} and V_{DD}.

If f_T is too small, the simple small signal model used to make the predictions would not be accurate at the 2.45 GHz operating frequency. As a rule of thumb, f_T should be at least one decade above the operating frequency, thus $f_T > 24.5\,\text{GHz}$ [11]. This means that, the results are likely to be accurate for $V_{DD} \geq 275\,\text{mV}$ if $V_{BP} = 0\,\text{V}$ and for

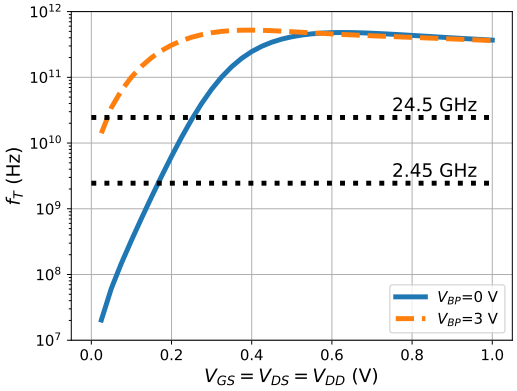

Fig. 7. Simulation results of the transition frequency f_T of a transistor of $L = 30\,\text{nm}$ and $W = 206\,\text{nm}$ as a function of $V_{GS} = V_{DS} = V_{DD}$ for different values of V_{BP}.

$V_{DD} \geq 50\,\text{mV}$ if $V_{BP} = 3\,\text{V}$. This is consistent with the results shown in Figs. 5 and 6.

In (3), we have $I_D \geq 0$ if $g_m/I_D > g_o/I_D$. This is equivalent to $g_m/g_o > 1$, bounding the intrinsic gain of the transistor. Figure 8 shows the dependence on V_{DD} of g_m/I_D and g_m/g_o for $V_{BP} = 0\,\text{V}$ and $V_{BP} = 3\,\text{V}$. Note that $g_m/g_o > 1$ for $V_{DD} \geq 25\,\text{mV}$ if $V_{BP} = 0\,\text{V}$ and for $V_{DD} \geq 30.7\,\text{mV}$ if $V_{BP} = 3\,\text{V}$.

For values of V_{DD} for which $g_m/g_o > 1$, there is an N large enough to satisfy (5). However, increasing N increases the parasitic capacitances of the transistors. This is a problem if the equivalent parasitic capacitance is greater than C_{tot}, where

$$C_{tot} = \frac{1}{(2\pi f_{osc})^2 L_1}, \tag{6}$$

because in this case the desired oscillation frequency cannot be tuned by means of adjusting C_1. Thus,

$$C_1 = C_{tot} - N\left(\frac{C_{gs}+C_{gb}+C_{sd}+C_{bd}}{2} + 2C_{gd}\right) \geq 0, \tag{7}$$

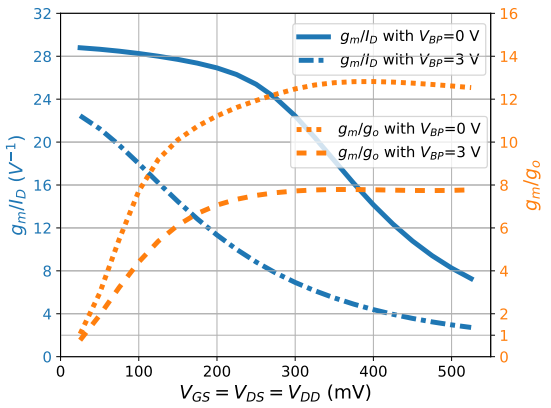

Fig. 8. g_m/I_D and g_m/g_o as a function of V_{DD} for $V_{BP} = 0\,\mathrm{V}$ and $V_{BP} = 3\,\mathrm{V}$, extracted from the LUT.

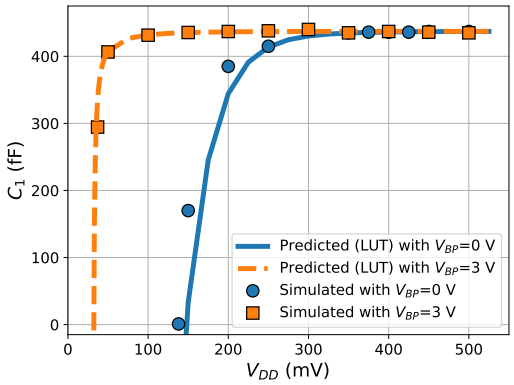

Fig. 9. Simulated necessary capacitor C_1 for oscillation at 2.45 GHz as a function of V_{DD} for $V_{BP} = 0\,\mathrm{V}$ and $V_{BP} = 3\,\mathrm{V}$.

where C_{ij} are the capacitances of a unitary transistor loaded from the LUT.

Figure 9 shows the capacitor C_1 needed to tune the oscillation frequency to 2.45 GHz. The values of C_1 found through (7) and the LUT, are compared to the simulation results of the oscillator, for $V_{BP} = 0\,\mathrm{V}$ and $V_{BP} = 3\,\mathrm{V}$, obtaining an excellent agreement. The capacitor $C_1 = 0\,\mathrm{F}$ for $V_{DD} = 150\,\mathrm{mV}$ if $V_{BP} = 0\,\mathrm{V}$, and for $V_{DD} = 35\,\mathrm{mV}$ for $V_{BP} = 3\,\mathrm{V}$.

Table I shows the simulation results for the minimum V_{DD} obtained.

In the case of $V_{BP} = 0\,\mathrm{V}$, the most restrictive condition on V_{DD} is that of the parasitic capacitances of the transistors, since the minimum V_{DD} is obtained for $C_1 = 0\,\mathrm{F}$, while the intrinsic gain is still high since $g_m/I_D = 9.70 \times g_o/I_D$. Further, slight, improvement in the minimum supply voltage could be achieved by replacing the inductor L_1 with a smaller one (lower L_1 at the oscillation frequency), relaxing the most restricting constraint (parasitic capacitance) at expense of a small decrease in R_P and a small increase in the minimum I_D.

In the case of $V_{BP} = 3\,\mathrm{V}$, the intrinsic gain is the most restrictive condition on lowering V_{DD}, since $g_m/I_D = 1.25 \times g_o/I_D$ for the minimum V_{DD} and there is still headroom for C_1 to properly tune the frequency.

TABLE I
SIMULATION RESULTS OF THE OSCILLATOR FOR THE MINIMUM SUPPLY VOLTAGE V_{DD}.

V_{DD} (mV)	V_{BP} (V)	N	I_{D_Q} (µA)	g_m/I_D (V^{-1})	g_o/I_D (V^{-1})	C_1 (fF)
138	0	2600	32.67	27.85	2.87	0
37	3	800	315.8	21.97	17.58	294.5

V. Conclusion

There are two limitations for lowering V_{DD}: the parasitic capacitances of the transistors must be small enough to attain the target frequency of 2.45 GHz and the intrinsic gain of the transistors must be greater than 1.

The minimum current predicted is in good agreement with the simulation results, as long as the transition frequency of the transistors f_T is at least 10 times the oscillation frequency.

A 2.45 GHz cross-coupled LC oscillator is feasible at $V_{DD} = 138\,\mathrm{mV}$ for $V_{BP} = 0\,\mathrm{V}$ and $V_{DD} = 37\,\mathrm{mV}$ for $V_{BP} = 3\,\mathrm{V}$ in 28 nm FD-SOI.

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