

AN ELECTRONICALLY ASSISTED BINARY INDUCTIVE VOLTAGE DIVIDER

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Abstract

A high precision Binary Inductive Voltage Divider (BIVD) was developed. The main application field is at low frequencies (50 Hz to 1 kHz) with input voltages up to 240 V (4.8 V/Hz). It has eight stages, reaching uncertainties of few parts in 10^9 at the ratio 256:1. The device can be self calibrated, without the need of any external reference.

Introduction

BIVDs have many advantages on decade dividers [1]. A computer can easily control them, they require fewer numbers of switches than decade dividers, and self calibration of each stage is possible. If separate stages are used, as proposed in this paper, stray capacitances can be compensated with a simple auxiliary variable capacitor connected in each stage. On the other hand, this kind of dividers has the problem of the load of each stage on the previous one, due to the non-negligible output impedances and relative low input impedances. In this paper an electronic solution is proposed to reduce this effect. The main application of this research was for the input divider of our reference wattmeter to scale from 240 V to the level of 1 V [2], using the ratio 256/1. However, the stages connection system allows to reach any binary combination.

Description

The proposed system has eight totally separated binary stages, where each one has a 2:1 main divider, IVD_m, and an auxiliary device for eliminating the load effect of the following stage. The IVD_m are very small (60 mm × 25 mm) and have 2×1680 turns with a resistance of 2×74 Ω. Fig. 1 shows a schematic circuit for the stages 1 to 4 (near to the input), and Fig. 2 for the stages 5 to 8. The follower configuration of the OpAmp reduces the output impedance to values lower than 1 mΩ. To reduce the gain error of the amplifier, the common point of the power supply sources V_a is connected to a voltage equal to the output voltage V_o . In this way, the amplifier always sees null output voltage (and then, null input voltage), regardless of the real input voltage. Then, the gain errors are practically eliminated. The maximum output voltage of stage five is 7.5 V, so that IC2 (Fig. 2) can manage it with conventional power sources of ±15 V. On the other

hand, an auxiliary divider 2:1, IVD_a, was used in stages 1 to 4 (Fig. 1) for that function because they have higher working voltages.

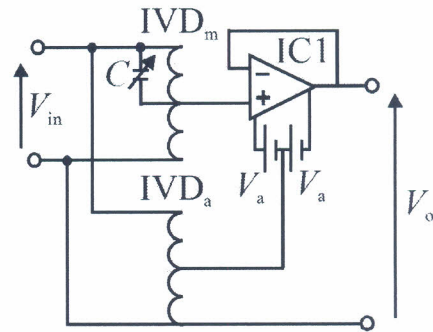


Fig. 1. Schematic circuit for the first four stages of the BIVD.

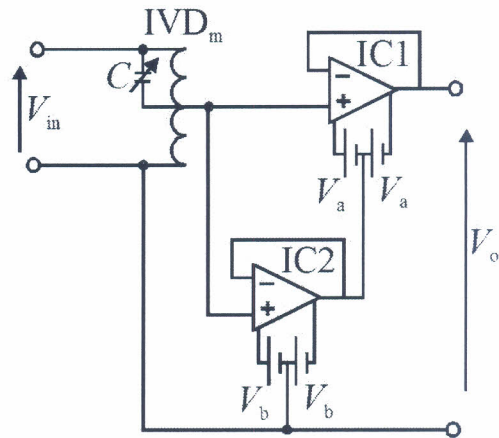


Fig. 2. Schematic circuit for the stages 5 to 8 of the BIVD.

Calibration

Each stage can be self calibrated using any other stage as an auxiliary divider. It is necessary to make two comparisons, inverting the connections of the auxiliary divider. The average values of these ratio and phase displacement errors correspond only to the error of the divider under test, whichever it is the error of the auxiliary divider. The null detector is formed by an amplifier, a band-pass filter and a digital oscilloscope. Using a large number of averages, and the rms and phase

angle calculation facilities, the ratio and phase shift errors of each stage can be calculated. The external trigger of the oscilloscope is driven by the input voltage of the IVD under test, through an opto-isolated coupler. This assures a stable trigger.

Influence factors

Varying the input voltage of the first 4 stages between 10 V and 120 V, the variation of the real and imaginary parts of the error is less than 8×10^{-8} and 3×10^{-8} of their average value, respectively; and even more, the influence of this uncertainty source can be further reduced calibrating each IVD at its real working voltage. The error curves are smooth and predictable.

Another influence factor is related to external magnetic fields. All stages have partial magnetic shields. The efficiency of these shields, regarding to the fields generated by another stages, was measured turning on and off the voltage of adjacent IVDs, to the one under test. The observed changes were under 1×10^{-8} in ratio errors and 6×10^{-8} in phase displacement. The influence of other external fields can be neglected placing the device far from those magnetic field sources.

The errors also depend on frequency. To reduce this variation, an adjustable capacitor C is placed between the central point of the winding and one extreme. In this way, the winding stray capacitances can be compensated. This problem increases at high frequency. The prototype was tested between 50 Hz and 1 kHz, and error variations in the order of 2×10^{-6} in the real part, and 5×10^{-7} in the imaginary one were founded for all stages. Anyway, performing the self calibration at the working frequency, this uncertainty contribution can be greatly reduced.

The load of one stage on the previous one produces additional errors. They depend on the output and input impedances, and the connection impedances. The output impedance is lower than $1 \text{ m}\Omega$ due to the OpAmp IC1. For connecting stages, cooper bars are used. Their impedances are around $0.5 \text{ m}\Omega$. On the other hand, the values of the input impedances vary between $80 \text{ k}\Omega$ and $140 \text{ k}\Omega$, depending on the stage, its voltage and frequency. Then, the errors caused by load effect, are in the order of 2×10^{-8} , for each step.

Conclusions

An eight stages binary inductive divider was presented. It is intended for low frequency applications (50 Hz to 1 kHz). One of the main error sources, the load of one stage on the previous, was greatly reduced with a simple active device. Other uncertainty sources can be limited using the self calibration process at the working conditions. Total ratio and phase shift uncertainties of few parts in 10^7 were

obtained at 50 Hz, at the ratio 256/1, equivalent to one part in 10^9 of the input.

Acknowledgments

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