Low-voltage low-noise high-CMRR biopotential integrated preamplifier

Carolina Cabrera, *Student Member, IEEE*, Renzo Caballero, *Student Member, IEEE*, María C. Costa-Rauschert, Conrado Rossi-Aicardi, *Member, IEEE*, Julián Oreggioni, *Senior Member, IEEE*

***Abstract*—This work presents a novel amplifier architecture which is the input stage of an analog front end targeting the acquisition of biological signals with low voltage supply (1.2 V), low noise, high Common Mode Rejection Ratio (CMRR) and high current efficiency. A prototype, designed and fabricated in a 130 nm CMOS technology, was characterized by simulations and measurements. Our preamplifier presents one of the lowest noise levels reported up-to-date (over the considered bandwidth) while presenting a very competitive performance in other important features. Results from measurements show a bandwidth from 20 Hz to 11 kHz, a CMRR higher than 70 dB, an equivalent input-referred noise as low as 1.3 μV_{rms}. The Noise Efficiency Factor (NEF) at 2.5 and Power Efficiency Factor (PEF) at 7.5 are remarkable results.**

***Index Terms*—Analog integrated circuits, low-power, neural amplifier, differential difference amplifier, bandpass filter, sub-threshold design, high CMRR**

I. Introduction

In recent decades, the increasing demand for medical equipment capable of health monitoring, diagnosis aid, patient recovery and follow-up, has led to the development of a significant number of portable and implantable medical devices. In particular, technological advances have allowed the miniaturization of electrocardiogram (ECG), electromyogram (EMG), electroencephalogram (EEG), and neural activity (like Local Field Potentials, LPF, or Action Potentials, AP) recording devices. These devices must be small in size and have low power consumption. In this regard, CMOS technology has played a fundamental role in the miniaturization process over time because it has increased its functionalities and processing capabilities, while reducing both size and power consumption. Clear examples of these advances, among others, are the Insertable Cardiac Monitor [1] or biopotential recording devices that acquire and process neural signals for the most diverse purposes: medical, prosthetics [2] [3], research [4] [5], and even entertainment [6].

A preamplifier is usually the input stage of biopotential recording devices (see Fig 1). It must amplify signals in the range of interest for the application, and filter unwanted signals while maintaining the highest possible signal to noise ratio.

This work was partially funded by CSIC (Comisión Sectorial de Investigación Científica, Uruguay), ANII (Agencia Nacional de Investigación e Innovación, Uruguay) and CAP (Comisión Académica de Posgrado, Uruguay).

C. Cabrera, C. Rossi-Aicardi, and J. Oreggioni are with Instituto de Ingeniería Eléctrica, Universidad de la República, Montevideo, Uruguay (e-mail: ccabrera@fing.edu.uy, cra@fing.edu.uy, juliano@fing.edu.uy).

R. Caballero, and M. C. Costa-Rauschert were with Instituto de Ingeniería Eléctrica, Universidad de la República, Montevideo, Uruguay.

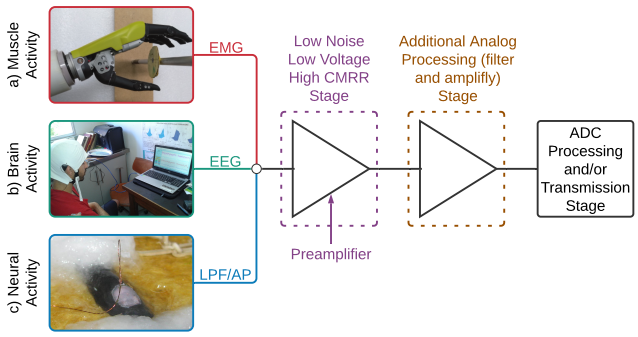

Fig. 1. Typical use of a preamplifier as the input stage of a biopotential recording device: a) Osseointegrated neural prosthesis [3], b) Wireless EEG System [4], and c) Weakly electric fish recording [5].

Besides, the dc signals caused by the contact potential between the electrodes and the skin must be filtered out. In [5], a neural preamplifier featuring low input noise, high Common Mode Rejection Ratio (CMRR), and high current-efficiency (low Noise Efficiency Factor, NEF [7]) was presented. The amplifier improves the performance with respect to capacitive feedback neural amplifiers, such as the one presented in [8], by taking advantage of the high CMRR achievable in a standard DDA (Differential Difference Amplifier) structure without jeopardizing power consumption. In addition, the gain and bandpass cut-off frequencies are fixed by means of parameters that are, respectively, accurate (i.e. ratios of transconductances) or can be easily and automatically tuned (i.e. ratios of transconductance over capacitances) [9], achieving high-accuracy and low power consumption [10]. Moreover, the preamplifier proposed in [5] introduced a novel technique for blocking the dc input voltage.

However, the number of stacked transistors makes the topology in [5] not suitable for low supply voltages, required in technologies with smaller geometrical features. Designing a preamplifier for those technologies has many advantages. For instance, it can be built in on the same chip together with complex digital signal processing circuitry. This work presents a novel topology that implements the same general idea in [5], albeit enabling a nominal supply voltage of just 1.2 V (compared to 3.3 V in [5]), thus allowing to design, fabricate and test the new preamplifier topology on a 130 nm CMOS technology.

This paper significantly expands the work presented in [11] by introducing a detailed description of the architecture, a fully experimental characterization of the fabricated chips, together

with a more comprehensive comparison with other designs in the literature. Furthermore, a deep analysis of the main effects of the technique for blocking the dc input voltage on the gain, high-pass frequency, and other important parameters of the preamplifier are presented.

The preamplifier was designed to the following general specifications, suitable for applications that simultaneously require high CMRR, low noise, and low NEF or low PEF (Power Efficiency Factor [12]), like the ones presented in Fig. 1 (EMG or neural signals from cuff electrodes in an osseointegrated neural prosthesis, or weakly electric fish neural recordings):

- Voltage supply: $V_{DD} \leq 1.2$ V
- Input equivalent noise $\leq 2\ \mu V_{rms}$
- CMRR $\geq$ 70 dB
- Gain: G = 40 dB
- High-pass frequency: f_{HP} = 20 Hz
- Low-pass frequency: f_{LP} = 10 kHz
- Input linear range = 2 mV_{pp} with a THD (Total Harmonic Distorsion) $\leq$ 5%

The rest of this paper is organized as follows: Section II describes the proposed architecture in detail while Section III presents the implementation according to the specifications above. Section IV shows the results of comprehensive measurements on the fabricated prototype and, Section V compares our work with the state-of-the-art. Finally, Section VI presents concluding remarks.

II. Architecture

Starting from the general idea in [5], we present a new topology needed for the reduced 1.2 V supply voltage, a condition for fabrication in 130 nm. The novel topology is shown in Fig. 2. The main novelty of our proposal consists in replacing the NMOS asymmetric differential pair of [5] for a PMOS one placed on the other branch of Gm1 (M6 and M7 in Fig. 2). In this way, it is possible to reduce the supply voltage, because Gm1 has fewer transistors stacked in the output branch. Moreover, this solution enhances symmetry between positive and negative dc input voltages, as both asymmetric pairs (M6-M7 and M5-M8) are built with MOSFETs of the same type.

Gm1[1] is an OTA (Operational Transconductance Amplifier) with a differential input (v_{IN}) and a single ended input (v_F). The Gm1 core is formed by M1, M2, M3 and M4 and its transconductance is G_{m1}. The single ended input v_F is connected to a local feedback loop circuit, implemented by M5-M8 together with Gmf and C_F, that establishes the high-pass characteristic and blocks the dc input.

In small-signal operation M6-M7 and M5-M8 can be thought of as asymmetric differential pairs where α (see 2) defines the degree of asymmetry. So, $g_{m7} = \alpha g_{m6}$ and $g_{m8} = \alpha g_{m5}$, where g_{m5}, g_{m6}, g_{m7}, and g_{m8} are the transconductances of M5, M6, M7, and M8 respectively. The

[1]OTA notation: Gmi refers to the block, G_{mi} (italic) is the transconductance of the block and g_{mi} (italic lowercase) is the transistor transconductance.

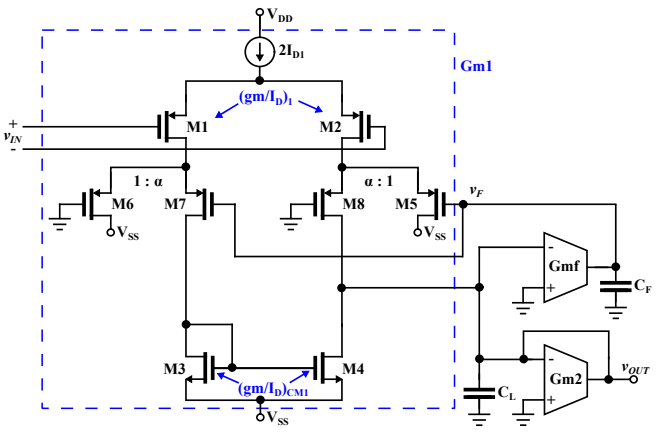

Fig. 2. Proposed preamplifier architecture.

effect of these transistors in the value of G_{m1} can be observed in Eq. 1,

$$G_{m1} = g_{m1}\frac{\alpha}{1+\alpha} \tag{1}$$

where g_{m1} is the transconductance of the input transistors of Gm1 (M1 and M2).

The key parameter α rules the trade-off between dc input voltage ($V_{IN,dc}$) blocking capacity, accuracy of the high-pass frequency (f_{HP}), noise, and the overall amplifier gain (G). An in-depth analysis of the influence of α on these characteristics of the preamplifier is presented in the following sections.

Gm2 and Gmf are implemented as symmetrical OTAs whose respective transconductances are G_{m2} and G_{mf} (see Fig. 3 and Fig. 4). The transconductance of the input transistors in Gm2 is $g_{m2} = K_{G_{m2}} G_{m2}$, where $K_{G_{m2}}$ is the copy factor of the current mirrors in Gm2. In the same way, we introduce $K_{G_{mf}}$ such that $g_{mf} = K_{G_{mf}} G_{mf}$ and g_{mf} is the transconductance of the input transistors in Gmf. We use symmetrical OTAs because it is a simple architecture, but other alternatives can be considered as well. However, non-symmetrical OTAs similar to the one used in Gm1, are not suitable to accommodate the required input and output ranges of Gm2 and Gmf. Furthermore, the savings on power consumption associated with using non-symmetrical OTAs in these blocks would have had little impact.

The input linear range of Gm2 was improved through the linearization technique in [13] consisting in adding two MOS transistors that produce source degeneration.

A. Asymmetric differential pair

M7 and M8 are implemented as α transistors identical to M6 and M5 respectively, connected in parallel as shown in Fig. 5. We will refer to the transconductance of the asymmetric differential pair as G_{mADP},

Given that the transconductance to dc drain current ratio of M5, M6, M7, and M8 are the same (referred to as $(g_m/I_D)_{ADP}$), it can be shown that the transconductance of the asymmetric differential pair G_{mADP} is given by Eq. 2.

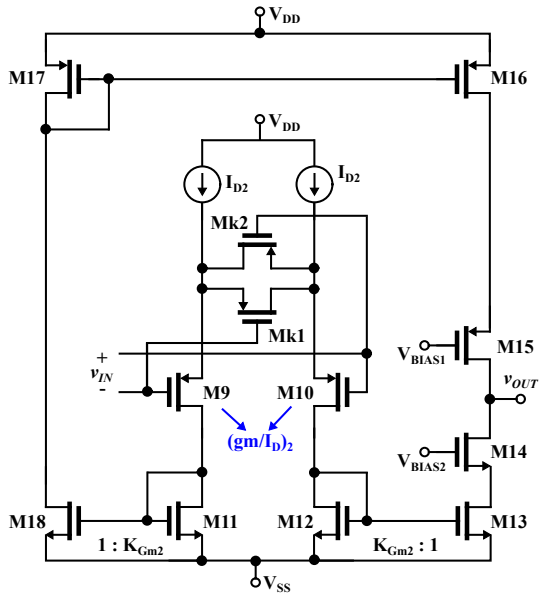

Fig. 3. Implementation of Gm2 at transistor level.

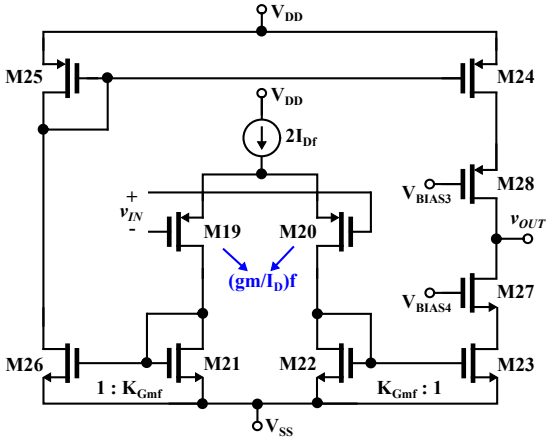

Fig. 4. Implementation of Gmf at transistor level.

$$G_{mADP} = g_{m\ ref}\frac{4\alpha}{(1+\alpha)^2} \tag{2}$$

where $g_{m\ ref}$ is the transconductance of a symmetric differential pair (α = 1),

$$g_{m\ ref} = \frac{I_B}{2}\left(\frac{g_m}{I_D}\right)_{ADP} \tag{3}$$

and I_B is the tail current of the differential pair.

Fig. 6 shows how the transconductance of the asymmetric differential pair varies as a function of α. Note that it is maximal when $\alpha = 1$.

The output conductance of the asymmetric differential pair (the conductance looking to the drain of M8) is given by Eq. 4.

$$G_{out_{ADP}} = g_{DS_8}\frac{1}{1+\alpha} \tag{4}$$

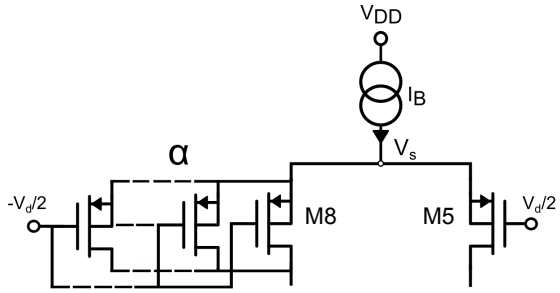

Fig. 5. Asymmetric differential pair.

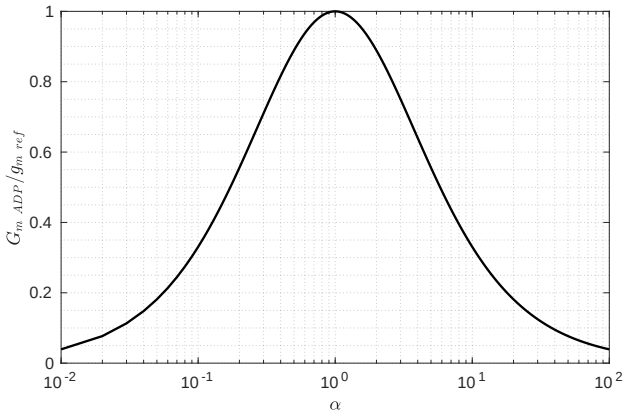

Fig. 6. Standardized asymmetric differential pair transconductance

where g_{DS_8} is the small-signal output conductance of M8. Therefore, the output conductance of Gm1 (G_{out_1}) will be given by Eq. 5.

$$G_{out_1} = g_{DS_4} + g_{DS_8}\frac{1}{1+\alpha} \tag{5}$$

where g_{DS_4} is the small-signal output conductance of M4. It should be noted that the output conductance of Gm1 depends on α.

B. Transfer function

The transfer function of Gm1 is as follows (see Fig. 2):

$$i_{Gm1} \cong G_{m1}.v_{IN} + G_{mADP}.v_F \tag{6}$$

where i_{Gm1} is the output current of Gm1.

The transfer function of the circuit depicted in Fig. 2 is:

$$\frac{v_{out}}{v_{in}}(s) = \frac{\frac{G_{m1}}{C_L}s}{s^2 + \frac{G_{out}}{C_L}s + \frac{G_{mADP}G_{mf}}{C_L C_F}} \tag{7}$$

where

$$G_{out} = G_{out1} + G_{m2} \tag{8}$$

When poles are separated enough, the following expressions are good approximations for the bandpass gain and the frequencies of the poles:

$$G = \frac{G_{m1}}{G_{out}} \tag{9}$$

$$f_{HP} = \frac{G_{mADP} G_{mf}}{2\pi G_{out} C_F} \tag{10}$$

$$f_{LP} = \frac{G_{out}}{2\pi C_L} \tag{11}$$

C. High-pass / dc input blocking circuit

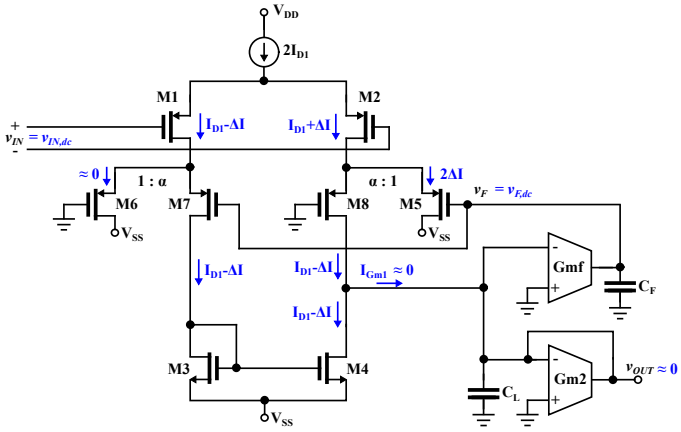

Fig. 7. Block diagram of the proposed architecture. The steady state condition of the dc input blocking mechanism is highlighted, this implies that the current through M8 equals the one by M7 and $I_{Gm1} \approx 0$.

Considering dc operation, when both inputs are at the same voltage, the currents through M1 and M2 are equal ($I_{D1} = I_{D2}$). Any dc input signal $V_{IN,dc}$ will generate a current ΔI through M1 and M2 (see Fig. 7). In an OTA standard structure (without M5, M6, M7, and M8), the current through M1 (I_{D1}) will be copied to the output by the current mirror formed by M3 and M4. Then, if M5, M6, M7 and M8 are not present, the excess current caused by $V_{IN,dc}$ will exit the circuit at the output node ($I_{Gm1} = 2\Delta I$).

Therefore, when the dc input signal causes the current through M8 to rise[2] ($I_{D8} = I_{D1} + \Delta I$), I_{Gm1} will also rise, and v_{OUT} will rise as well (Gm2 acts as a resistor to ground). Because of this, Gmf will decrease its output current and v_F will fall. Then, the current that M5 drains will increase and M6 will cut off. The equilibrium will be reached when $I_{D7} = I_{D8}$, and consequently when $I_{Gm1} = 0$. This steady state condition (marked in blue in Fig. 7) holds in a simplified case where Gmf-C_F provides ideal integration with infinite dc gain. In a practical case, the finite dc gain and offset of Gmf will result in a small remaining output dc offset.

It is interesting to note that any mismatch in the transistors of Gm1 that would generate a ΔI current, will also be minimized by the feedback loop through Gmf. One side-effect of this technique is that in ac operation M5 and M6 will drain signal current, as is further analyzed in Section II-E.

D. Noise

As the total noise is dominated by the first stage (Gm1), thermal noise input-referred power spectral density S_{ni}^{total} for the circuit shown in Fig. 2 is very well approximated by:

[2]An analog reasoning can be carried out if it is considered that the current through M7 rises ($I_{D7} = I_{D1} + \Delta I$).

$$S_{ni}^{total} \cong \frac{2nkT}{g_{m1}} \gamma_{EQ} \tag{12}$$

where n is the slope factor, k is the Boltzmann constant, T is the absolute temperature, and γ_{EQ} is:

$$\gamma_{EQ} = \gamma_{WI} + \gamma_{SI} \frac{\alpha+1}{\alpha} \frac{(g_m/I_D)_{CM1}}{(g_m/I_D)_1} + \\ + \gamma_{WI} \frac{1}{\alpha+1} \frac{(g_m/I_D)_{ADP}}{(g_m/I_D)_1} \tag{13}$$

where $(g_m/I_D)_1$, $(g_m/I_D)_{ADP}$, and $(g_m/I_D)_{CM1}$ are respectively the transconductance to dc drain current ratios of the input transistors of Gm1 (M1 and M2), the asymmetric differential pair (M5, M6, M7, and M8) and the current mirror transistors of Gm1 (M3 and M4), where CM stands for "Current Mirror". $\gamma_{WI} = 2$ and $\gamma_{SI} = 8/3$ are the excess noise factors in weak and strong inversion, respectively.

According to Eq. 13, to reduce thermal noise, the input differential pair of Gm1 (M1 and M2) is better biased in weak inversion (high value of $(g_m/I_D)_1$), and the current mirror (M3 and M4) in strong inversion (low value of $(g_m/I_D)_{CM}$).

For the same reason, M5, M6, M7, and M8 should be biased in strong inversion. However, they were biased in weak inversion (high value of $(g_m/I_D)_{ADP}$) to obtain a low V_{DSsat}, which is necessary to meet the requirements of low voltage supply.

Fig. 8 plots γ_{EQ} as a function of α, where $(g_m/I_D)_1$ = 26 V^{-1}, $(g_m/I_D)_{ADP}$ = 26 V^{-1}, and $(g_m/I_D)_{CM1}$ = 7 V^{-1}. γ_{EQ} was normalized with respect to γ_{EQ} with α = 1 ($\gamma_{EQ_0} = \gamma_{EQ@\alpha=1}$).

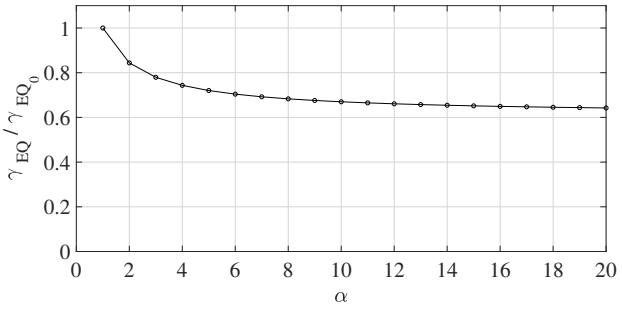

Fig. 8. Normalized γ_{EQ} factor as a function of α.

According to Eqs. 12 and 13, large values of α minimize noise. However, Fig. 8 shows that is not necessary to use very high values of α to have a good performance in terms of noise. For example, for α = 4 a reduction of 26 % of noise is achieved ($\gamma_{EQ}/\gamma_{EQ_0}$ = 0.74) while the asymptotic value ($\alpha > 250$) gives a 39 % of noise reduction ($\gamma_{EQ}/\gamma_{EQ_0}$ = 0.61).

The effect of flicker noise can be highly reduced by increasing the width (W) and length (L) of M1 and M2 while keeping constant the W/L ratio so that the inversion level, and consequently the g_m/I_D ratio, is not modified.

E. Variations in Gm1 due to the dc input voltage blocking technique

The dc input blocking capacity will be evaluated through the normalized variation of the dc current imbalance that is generated between M1 and M2 by a dc input voltage V_{inDC}:

$$\Delta I_{DC} = \frac{I_1 - I_2}{4I_{D1}} \tag{14}$$

where $2I_{D1}$ is the bias current of Gm1. The graphs are normalized with respect to their balanced state: $G_0 = G_{@\Delta I_{DC}=0}$, and $f_{HP_0} = f_{HP@\Delta I_{DC}=0}$.

The results presented in this section were numerically calculated using the ACM [14] model for M5, M6, M7, and M8.

1) Gain: The gain depends on G_{m1} and G_{out1}. Both are affected by the degree of asymmetry α. According to Eq. 1 there is a gain attenuation due to the asymmetric differential pairs. Fig. 9 shows how the asymmetric differential pairs modify the gain, as a function of α and ΔI_{DC}. Fig. 10 presents a cross section of Fig. 9 for some particular values of α.

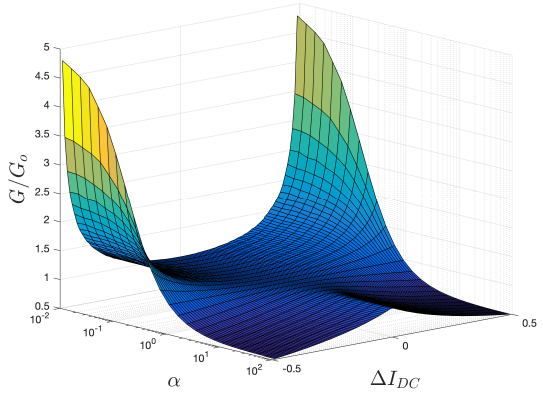

Fig. 9. Variation of the normalized gain G as a function of α and ΔI_{DC}

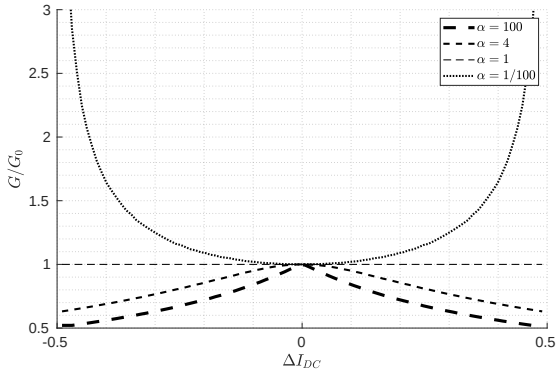

Fig. 10. Cross section of Fig. 9. Variation of normalized G as a function of ΔI_{DC} for $\alpha = \{0.01, 1, 4, 100\}$

Fig. 10 shows that large values of α introduce a significant reduction on the gain in presence of dc input signals. Also, an optimum value of α is registered for α = 1. Fig. 10 also shows the behavior of the circuit for α = 4.

2) High-pass frequency: In the transient of the dc input voltage blocking, the operation point of the asymmetric differential pairs will be changing until $I_{D7} = I_{D8}$. This will result in a variation of the transconductance of the asymmetric differential pairs G_{mADP} (which is a function of α). In addition, Eq. 10 shows that the preamplifier high-pass frequency depends on G_{mADP}. Fig. 11 shows the variation of f_{HP} considering different values of α and ΔI_{DC}. Fig. 12 presents a cross section of Fig. 11 for some particular values of α.

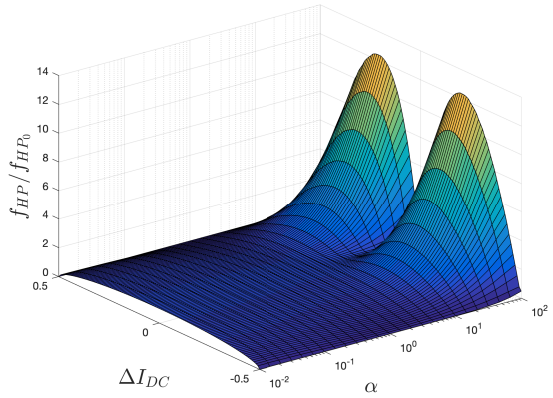

Fig. 11. Variation of normalized f_{HP} as a function of α and ΔI_{DC}

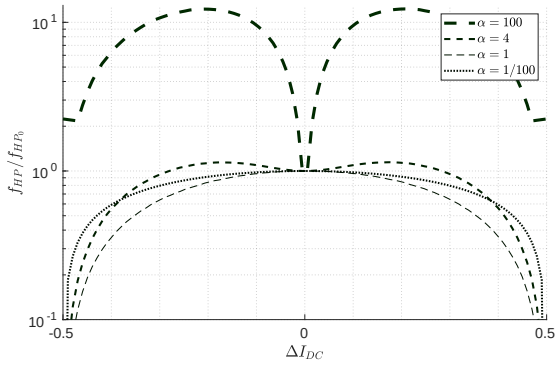

Fig. 12. Cross section of Fig. 11. Variation of normalized f_{HP} as a function of ΔI_{DC} for $\alpha = \{0.01, 1, 4, 100\}$

According to Fig. 12, large values of α introduce a significant variation on the f_{HP} when blocking dc input signals. On the other hand, when α = 1, a variation of 10 % on the f_{HP} ($0.9 \leq |f_{HP}/f_{HP_0}| \leq 1.1$) only occurs when $|\Delta I_{DC}| \simeq 0.15$. Finally, it is observed that there is an optimum value around α = 4, where the variation of 10 % occurs for $|\Delta I_{DC}|$ as large as 0.30.

F. Selection of α

In the preceding sections it became evident that several parameters depend on the degree of asymmetry α. This subsection analyzes the involved tradeoffs.

For α = 1 the circuit can block high levels of dc input signals without introducing gain variation through different dc input voltages (Section II-E1). However, the differential pairs

M5-M8 and M6-M7 will be symmetrical and half of the gain of Gm1 will be lost (low gain-efficiency, see Eq. 1).

For large values of α (i. e. $\alpha \geq 10$), the loss of gain due to the asymmetric differential pairs is negligible (high gain-efficiency, see Eq. 1) and the noise is minimum (Section II-D). But, in this case, the capability of blocking high levels of dc input signals will be reduced (Section II-E1). Also, large values of α introduce a significant variation on the high-pass frequency (Section II-E2).

As shown in Section II-D, it is not necessary to have very high values of α to have a reasonable performance in terms of noise. For example, for α = 4 a significant noise reduction is achieved. A similar situation occurs with the loss of gain (Eq. 1).

Finally, in Section II-E2 it was shown that, to reduce the variation of f_{HP} due to large dc input signals, there is an optimum value of α around 4.

Therefore, we choose α = 4 as a reasonable trade-off between gain-efficiency, noise, precision on f_{HP}, and dc input blocking capability.

III. Implementation

The preamplifier was implemented in a 130 nm standard CMOS process.

Following the considerations about noise in Section II-D, the mirror in Gm1 (M3-M4) was biased in strong inversion while the input differential pair (M1-M2) and the asymmetric pairs (M5-M8) were biased in weak inversion. Using the specifications presented in Section I, and equations from Section II-B, the preamplifier main parameters were determined (see Table I).

Cascode transistors were added in Gm1 (only to the M3-M4 mirror, referred to as MC1), Gm2 (M14-M15), and Gmf (M27-M28), to increase their output resistance and improve the overall performance of the circuit.

TABLE I
PREAMPLIFIER MAIN PARAMETERS (POST-LAYOUT SIMULATIONS).

	Gm1	Gm2	Gmf
$(g_m/I_D)_{InputPair}$	26 V^{-1}	5 V^{-1}	18 V^{-1}
$(g_m)_{InputPair}$	338 μS	600 nS	27 nS
G_m	270 μS	1.8 μS	300 pS
$(I_D)_{InputPair}$	13 μA	120 nA	1.5 nA
$(W/L)_{InputPair}$	550/2	4/8	1/164
K_{G_m}	1	1/3	90
$(g_m/I_D)_{CM}$	7 V^{-1}	-	-
G_{mADP}	100 μS	-	-

The voltage supplies (V_{DD} and V_{SS}) are determined by Gm1, as Gm2 and Gmf are more relaxed in terms of stacked transistors. The conditions given by Eqs. 15, 16, and 17, must be met.

$$V_{BIAS,MC1} - V_{GS,MC1} > V_{SS} + V_{DSsat,M4} \tag{15}$$

so that the transistors in the mirror M3-M4 are in saturation.

$$V_{SG,M8} - V_{SDsat,M8} + \\ - (V_{BIAS,MC1} - V_{GS,MC1} + V_{DSsat,MC1}) > V_{OUT,pp} \tag{16}$$

leaves the needed headroom for the output.

$$V_{SG,M8} + V_{SDsat,2} + V_{sat,CS1} < V_{DD} \tag{17}$$

must be met for keeping M2 and the Gm1 bias current source (CS1) in saturation.

TABLE II
GM1 OPERATION POINT (SIMULATED).

Component	V_{GS} (mV)	V_{DSsat} (mV)
M1, M2	211	115
M3, M4	374	219
M5, M6	225	115
M7, M8	229	115
MC1	179	120
Gm1 bias current source (CS1)	489	226

Using data from a dc simulation of Gm1 (shown in Table II) and leaving room for an output voltage range ($V_{OUT,pp}$) of 200 mV_{pp}, we chose V_{SS} = −0.5 V and $V_{BIAS,MC1}$ = −0.1 V which comply with Eqs. 15, 16, and 17. Then, the positive supply is V_{DD} = 0.7 V as determined from the nominal supply voltage (1.2 V) of the technology. The minimum supply voltage for this circuit is limited by Eq. 17, so $V_{DD} > 570$ mV and $V_{DD} - V_{SS} > 1.07$ V.

The dc gate voltage of M7 and M8 and the reference values of Gm2 and Gmf were set to 0 V, so that the output is referred to this voltage, hereinafter referred to as "ground". The common-mode voltage of the gates of M1 and M2, referred to as V_{REF}, was initially set around 200 mV although there is some latitude around this value.

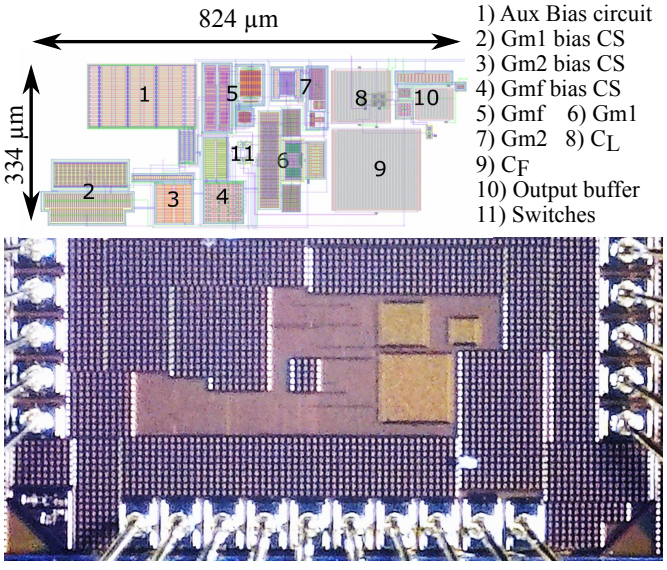

Fig. 13. Overview of the preamplifiers layout (above) with a micro-photograph of the manufactured chip (below). CS stands for "Current Source".

The capacitors were implemented by leveraging the Dual MIM Cap type available in the technology as it offers the best capacitance per area. The value of C_F, which directly affects the low-frequency pole, was chosen in advance as C_F = 100 pF limited by its approximate area of 150 μm x 150 μm considered to be the maximum acceptable to be spent on the capacitor. The design flow determined C_L = 48 pF. The connection of external capacitors was foreseen to provide the possibility of configuring the preamplifier bandwidth to different values.

Fig. 13 shows the layout and a microphotograph of the fabricated chip. Circuit blocks cannot be seen clearly in the photo due to metal fill structures. Nonetheless, the main blocks of the circuit are marked on the layout.

The fabricated amplifier occupies 0.275 mm^2. The area was not optimized, while the core of the amplifier occupies 0.103 mm^2 (including capacitors), auxiliary circuits (including biasing and test circuits) occupy 0.172 mm^2. The area of the auxiliary circuits could be much reduced. The distribution of the area is as follows: A_{Gm1} = 0.027 mm^2 (26 %), A_{Gmf} = 0.015 mm^2 (15 %), A_{Gm2} = 0.017 mm^2 (16 %), A_{C_F} = 0.030 mm^2 (29 %) and A_{C_L} = 0.014 mm^2 (14 %).

Table III presents results of Monte Carlo (MC) post-layout simulations (500 runs) using PSP model. PSRR+ is the positive power supply rejection ratio (V_{DD}) and PSRR- refers to the negative power supply rejection ratio (V_{SS}).

TABLE III
SIMULATION RESULTS.

	Specs	Result	Obs.
Voltage supply (V)	$\leq$1.2	1.2	-
Input noise (μV_{rms})	2.5	2.2	-
Noise integration bandwidth (Hz)		10 - 100k	
CMRR @ 1 kHz (dB)	$\geq$70	75	worst-value
Supply current (μA)	-	29.7	-
G (dB)	40	40.2	σ=0.2
f_{HP} (Hz)	20	19.5	σ=0.8
f_{LP} (kHz)	10	10.0	σ=0.4
Gain w/$V_{IN,dc}$ = 50 mV (dB)	-	35.5	-
Gain w/$V_{IN,dc}$ = 100 mV (dB)	-	27.5	-
THD w/V_{in} = 2 mV$_{pp}$	$\leq$5%	2.3%	-
PSRR+ (dB)	-	79	worst-value
PSRR- (dB)	-	53	worst-value

IV. EXPERIMENTAL RESULTS

Laboratory characterization was performed on six samples using a custom designed board.

A. Current consumption

Table IV compares the total current consumption of the chip and the contribution of the main blocks (Gm1, Gm2, and Gmf) with simulation results.

TABLE IV
CURRENT CONSUMPTION MEASUREMENTS.

	Sim	Ch1	Ch2	Ch3	Ch4	Ch5	Ch6
Gm1 (μA)	27.3	27.7	27.4	27.3	27.6	28.1	28.6
Gm2 (μA)	2.3	2.2	2.3	2.4	2.3	2.3	2.2
Gmf (μA)	0.12	0.12	0.12	0.12	0.12	0.13	0.12
Total (μA)	29.7	30.0	29.8	29.8	30.0	30.5	30.9

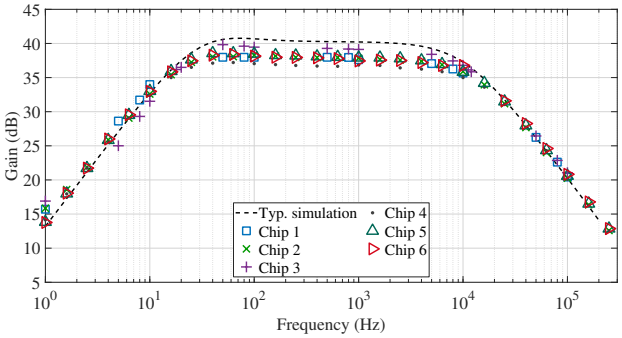

Fig. 14. Preamplifier frequency response.

B. Frequency response

Fig. 14 presents the frequency response of the six measured chips and the comparison with the simulation (typical value).

Table V shows the measured gain at 600 Hz, high-pass frequency and low-pass frequency for the six chips. The frequency response was measured using an input signal of 1 mV$_{pp}$. Measured gain is quite close to the simulated value. Pole frequencies are also close, although some dispersion in the measured values is observed. This is not detrimental as the bandwidth of the whole system is usually set in the following stage (Fig. 1).

TABLE V
FREQUENCY RESPONSE CHARACTERISTICS

	Sim	Ch1	Ch2	Ch3	Ch4	Ch5	Ch6
G (dB)	40.2	38.0	37.9	39.3	36.7	38.0	37.8
f_{HP} (Hz)	19.9	13.7	15.2	19.7	12.5	14.8	14.2
f_{LP} (kHz)	10.0	11.5	12.6	11.1	15.5	12.5	14.5

C. Noise

Noise laboratory characterization on six samples was performed. The noise power spectral density (PSD) was measured using an Agilent 4395A Spectrum Analyzer. Fig. 15 presents the noise results for two samples. Integration under the solid curve yields an input-referred noise voltage of 1.28 μV_{rms} for Chip 1 and 1.42 μV_{rms} for Chip 6, where the integration bandwidth was [10 Hz-100 kHz].

Table VI presents the input-referred noise voltage in μV_{rms} and the NEF for all measured chips and the typical simulation. The power efficiency factor PEF (equal to NEF$^2 \times V_{DD}$, [12]) is also presented. In all cases the integration bandwidth was [10 Hz-100 kHz]. Results of input-referred noise voltage and NEF are excellent for all measured chips.

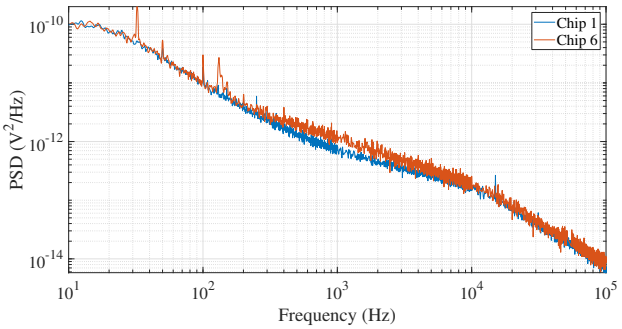

Fig. 15. Input-referred noise power spectral density

TABLE VI
NOISE PERFORMANCE.

	Ch1	Ch2	Ch3	Ch4	Ch5	Ch6
Input noise (μV_{rms})	1.28	1.44	1.27	1.57	1.37	1.42
NEF	2.5	2.7	2.5	2.7	2.6	2.5
PEF	7.5	8.7	7.5	8.7	8.1	7.5

D. Common Mode Rejection Ratio

Fig. 16 shows the CMRR of the six measured chips for a frequency range from 1 Hz to 200 kHz. The performance in terms of CMRR is very good: below 10 kHz it is almost always greater than 70 dB. At this frequency it starts to fall, but at 60 kHz it is still greater than 60 dB. In addition, at 50 Hz the measured value is 86 dB for Chip 3, 69 dB for Chip 2 (worst-case) and 90 dB for Chip 6 (best-case).

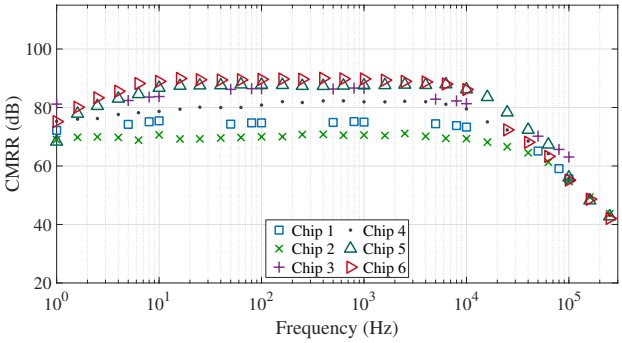

Fig. 16. CMRR measured for the six chips.

E. Power Supply Rejection Ratio

Figs. 17 and 18 respectively show the PSRR+ and PSRR- of 6 chips for a frequency range from 1 Hz to 200 kHz. These measurements were performed using V_{REF} = 170 mV. The measured PSRR+ at 50 Hz is 67 dB for Chip 3 (best case), and 65 dB for Chip 6 (worst case). On the other hand, the measured PSRR- at 50 Hz is 45 dB for Chip 3 (best case), and 43 dB for Chip 4 (worst case).

F. Total Harmonic Distortion

Table VII shows the linearity performance by means of the total harmonic distortion (THD) of Chip 6. These measurements were performed with the 4395 Agilent Spectrum Analyzer, using an input signal of 600 Hz and V_{REF} = 250 mV.

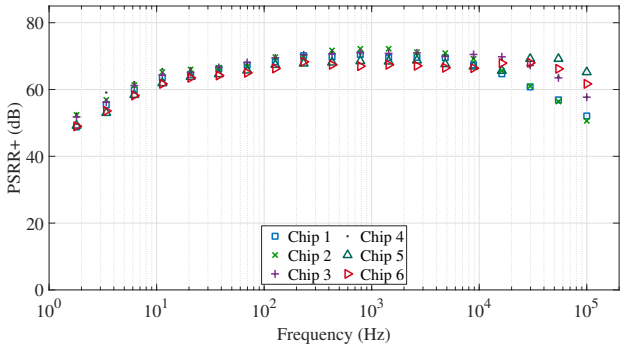

Fig. 17. PSRR+ measured for the six chips.

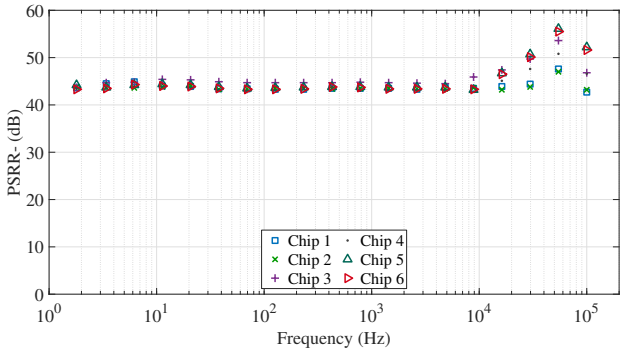

Fig. 18. PSRR- measured for the six chips.

The achieved THD is adequate to deal with the targeted input signals (amplitudes of hundreds of micro-volts).

TABLE VII
TOTAL HARMONIC DISTORTION (THD) FOR CHIP 6

V_{in}	THD
0.5 mV_{pp}	1.0 %
0.7 mV_{pp}	1.3 %
1.0 mV_{pp}	2.2 %
2.2 mV_{pp}	5.0 %
2.3 mV_{pp}	5.2 %

G. Input Common-Mode Range

The amplifier input common-mode range ICMR is 162 mV (within a 1.2 V power supply). This value of ICMR assures a loss of gain lower than 0.5 dB and a CMRR higher than 70 dB (see Fig. 19). This ICMR is enough to accommodate typical common-mode signals. Fig. 19 shows that, to guarantee a loss of gain lower than 0.5 dB and a CMRR higher than 70 dB, the amplifier inputs need to be biased to a common-mode potential (V_{REF}) in the range from 135 mV to 297 mV. These measurements were performed in the band-pass of the preamplifier at 1 kHz.

H. Output offset

The preamplifier output offset was measured as the difference between the voltage V_{OUT} with respect to ground, with the preamplifier inputs shorted to V_{REF} = 170 mV to

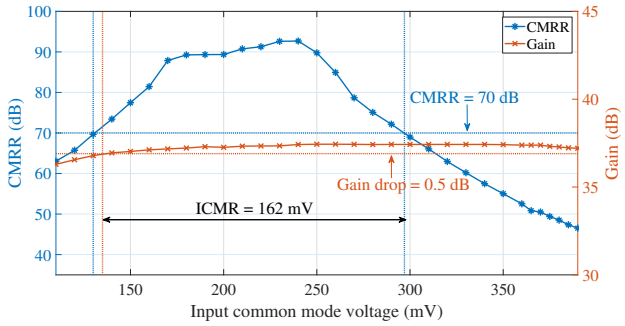

Fig. 19. Chip 6 measurement of input common-mode range (ICMR). Gain (orange) and CMRR (blue) measurements for different dc input common-mode voltages (referred to ground).

ensure proper operation. The measurements are presented in Table VIII:

TABLE VIII
OUTPUT OFFSET MEASUREMENTS

	Ch1	Ch2	Ch3	Ch4	Ch5	Ch6
Output Offset (mV)	3.5	-16.7	-6.7	13.4	-1.6	13.2

I. Gain variation with dc input signals

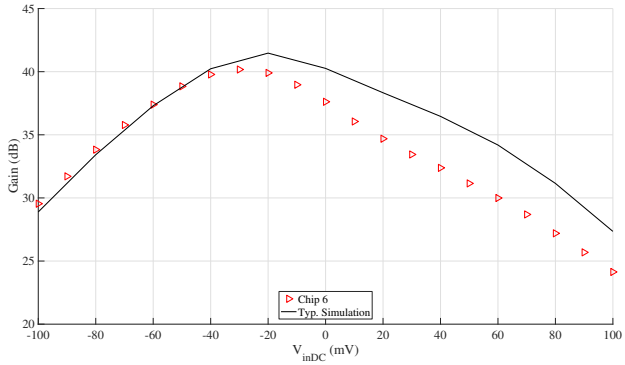

Fig. 20. Variations of the gain with a dc input voltage (V_{inDC}) for Chip 6.

Fig. 20 shows the gain at 600 Hz when the circuit is blocking a range of dc input voltages from -100 mV to 100 mV. The measured gain presents a shift of approximately 10 mV towards negative imbalances with respect to the simulated one.

J. Frequency response with external capacitors

Fig. 21 shows the frequency response of Chip 6. Between 20 Hz and 11 kHz internal capacitors are used (C_L = 48 pF and C_F = 100 pF), while for the band from 0.1 Hz to 250 Hz external capacitors with nominal values C_L = 2 nF and C_F = 22 nF are used. A minimal variation in the band-pass gain is observed along a wide bandwidth: 0.1 Hz and 11 kHz.

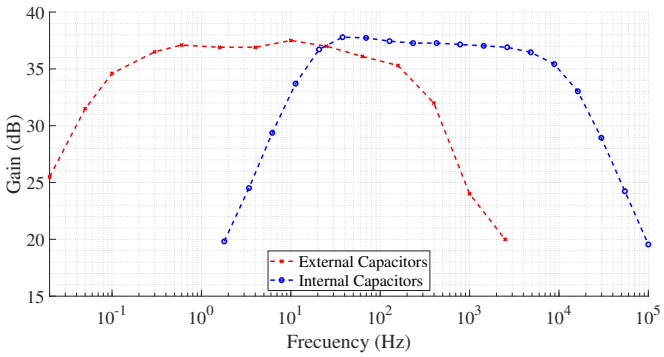

Fig. 21. Preamplifier frequency response for chip 6. The bandwidth can be programmed between 0.1 Hz and 11 kHz.

V. COMPARISON WITH STATE-OF-THE-ART

Table IX shows a comparison with the state of the art. Our preamplifier presents one of the lowest noise levels reported up-to-date (over the considered bandwidth) while presenting a very competitive performance in other important features, like CMRR or NEF. On the other hand, the overall preamplifier linearity input range, which is limited by the input differential pair linearity range (M1 and M2), is low but adequate to deal with the targeted input signals (amplitudes of hundreds of micro-volts).

VI. CONCLUSIONS

This work introduces a novel neural amplifier architecture which was fabricated and extensively measured.

A low voltage biopotential preamplifier, suitable for use in implantable or wearable devices, was designed and fabricated on a 130 nm CMOS technology. Results from simulations and measurements show its remarkable low input-referred noise, low supply voltage (1.2 V), high CMRR, and state-of-the-art NEF. These results favorably compare with prior work.

Results from measurements show that the CMRR is greater than 70 dB, the equivalent input noise can be as low as 1.3 μV_{rms}, the NEF 2.5, and the PEF 7.5.

The preamplifier has a configurable bandwidth, where f_{HP} can range from 0.1 Hz to 19.7 Hz, and f_{LP} from 250 Hz to 11.1 kHz.

Future work includes an in-vivo validation of the architecture.

ACKNOWLEDGMENT

The authors would like to thank Prof. Fernando Silveira from Universidad de la Repblica for his insightful advice and useful discussions, and Dr. Angel Caputi of IIBCE (Instituto de Investigaciones Biológicas Clemente Estable, Uruguay) for his guidance on requirements and his biological/medical insights. The authors are also very grateful to Gonzalo Carozo and Pablo Aguirre for their contribution in the first stage of this work. Finally, the authors thank Marion Hoffer and Fiorella Haim for proofreading this manuscript.

TABLE IX
COMPARISON WITH PRIOR WORK.

	JSSC '03 [8]	JETCAS '11 [15]	TBCAS '12 [16]	TCAS-I '13 [17]	TCAS-I '13 [18]	JSSC '16 [19]	TCAS-I '18 [20]	EMBC '19 [21]	TCAS-I '20 [22]	TBCAS '18 [5]	This Work
Technology (μm)	1.5	0.35	0.13	0.18	0.18	0.065	0.18	0.5	0.18	0.5	0.13
V_{DD} (V)	5.0	3.3	1.2	1.0	1.8	1.0	1.2	3.3	1.0	3.3	1.2
Gain (dB)	39.5	46.0	47.5	40.0	60	52.1	58	47	40.4	49.5	39.3
f_{LP} (kHz)	7.2	10.0	6.9	5.1	9	8.2	0.5	7.5	5.0	9.8	11.1
f_{HP} (Hz)	25m	200	167	0.38	0.3	1.0	0.5	1.0	1.0	13.0	19.7
Supply current (μA)	16.0	22.4	1.6	0.8	6.1	3.3	7.7	16.1	0.8	8.5	29.8
Power consumption (μW)	80.0	73.9	1.9	0.8	11.0	3.3	9.2	53.1	0.8	28.1	35.8
Input noise (μV_{rms})	2.2	2.9	3.8	4.0	5.0	4.1	1.3	1.8	4.1	1.9	1.3
Noise integration bandwidth (Hz)	0.5-50k	N/A	1-100k	1-8k	1-8k	1-8.2k	N/A	N/A	200-5k	0.03-25k	10-100k
NEF	4.0	6.6	2.3	1.9	4.6	3.2	6.2	3.2	2.0	2.1	2.5
PEF	80	144	6.1	3.7	38	10.2	46	34	4.0	14.6	7.5
CMRR (dB)	83	110	83	60	48	80	100	101	58	87	86
PSRR (dB)	85	110	70	70	55	78	N/A	N/A	54	74	67
Area (mm^2)	0.16	0.15	0.05	0.04	0.07	0.04	N/A	N/A	0.19	0.34	0.10
THD=1% (mV_{pp})	17	$>$20	3.1	N/A	1	1.4	$>$2	N/A	2.0	0.7	0.5

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Carolina Cabrera (S'18) received the B.Sc. degree in Electrical Engineering from Universidad de la República, Uruguay, in 2019. She is currently working as Research and Teaching Assistant at the Instituto de Ingeniería Eléctrica, Universidad de la República, where she is pursuing the M.Sc. degree in Electrical Engineering, focusing on low-noise and low-power analog circuit design, especially for biomedical applications. Her current research interests include low-power and low-noise analog circuit design, wireless embedded systems, and signal processing with reduced resources.

Renzo Caballero received the B.Sc. degree in Electrical Engineering from Universidad de la República, Uruguay, in 2016, and the M.Sc. degree in Applied Mathematics and Computer Science from King Abdullah University of Science and Technology (KAUST), KSA, in 2019. He is currently in a Ph.D. position under the supervision of Professor Eric Feron at KAUST. His current research focuses on self-replicating robots, but he also is interested in microelectronic design, synthesis of 2D materials, stochastic optimal control, and robust control.

María Cecilia Costa Rauschert received the B.Sc. degree in Electrical Engineering from Universidad de la República, Uruguay, in 2016, and M.Sc. degree in Advanced Microelectronic Systems from University of Bristol, UK, in 2019. She is currently part of the Silicon Team at Graphcore, UK. Her main areas of work in the electronics industry include embedded systems for biomedical applications, analog design of sensors, and digital design for AI applications.

Conrado Rossi-Aicardi (M'88) received the Electronics Engineering and Ph.D. in Electrical Engineering degrees from Universidad de la República, Montevideo, Uruguay in 1988 and 2013, respectively. Since 1984 he has held several teaching positions at the same university, where he is currently a part-time Associate Professor. From 1988 to 1995 he was involved in consulting for industrial and commercial automation. In 1991 he co-founded the Microelectronics Group at Universidad de la República where he has been part of several academic and industrial R&D projects to date. From 2007 to 2016 he was a founding partner at NanoWattICs, Montevideo, Uruguay. He is currently Design Center Manager at the Uruguay Design Center of Allegro MicroSystems. His research interests are related to low power analog and mixed signal IC design, in particular ultra low power temperature sensors, voltage references and biasing circuits.

Julián Oreggioni (M'06 SM'18) received the B.Sc., M.Sc., and Ph.D. degrees in Electrical Engineering from Universidad de la República, Uruguay, in 2006, 2013, and 2018 respectively. He is currently Assistant Professor with the Instituto de Ingeniería Eléctrica, Universidad de la República (Montevideo, Uruguay). He has more than ten years of experience in the electronics industry (M2M, e-commerce, vending machines, agrotech, and medical devices). He holds several patents, and is co-author of many technical articles. His main research interests include the design of ultra-low-power analog integrated circuit and systems, and low-power embedded systems, for biomedical and agrotech applications.