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Very Large Time Constant G_m-C Filters.

Alfredo Arnaud Maceira

Tesis presentada para la obtención del título de Doctor en Ingeniería, en el área de Microelectrónica.

Tutor: **Dr.Carlos Galup Montoro**
Universidade Federal de Santa Catarina (UFSC), Florianópolis - Brazil.

Tribunal: Dr.José Silva Martínez - (*Texas A&M University*)
Dr.Fernando Silveira - (*IIE - Fac.Ingeniería UROU*)
Dr.Ricardo Marotti - (*IF - Fac.Ingeniería UROU*)
Ing.Julio Arzuaga - (*C.C.C. del Uruguay S.A.*)
Prof. Rafael Canetti - (*IIE - Fac.Ingeniería UROU*)

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Filtros G_m-C de muy altas constantes de tiempo.

Resumen:

En esta tesis se presenta un conjunto de herramientas para el diseño de circuitos integrados que implementan filtros transconductor-capacitor (G_m-C), de muy altas constantes de tiempo, con bajo ruido, y consumo de corriente por debajo del micro-Ampere. Como ejemplo de aplicación se toma un amplificador-pasabanda 2º orden, de ganancia 400 en la banda de 0.5 a 7Hz, que realiza el acondicionamiento de señal de un acelerómetro piezoeléctrico a ser empleado en un marcapasos implantable. El principal desafío es realizar en dicho filtro de tiempo continuo, muy altas constantes de tiempo sin usar componentes externos. La técnica elegida para alcanzar tal objetivo es la división serie-paralelo de corriente en transconductores (OTAs) simétricos estándar. Estos circuitos demostraron ser una excelente solución en cuanto al área ocupada, su consumo, ruido, linealidad, y en particular offset. Se diseñaron, fabricaron, y midieron, OTAs hasta 33pS -equivalente a una resistencia de 30GΩ-, con hasta 1V de rango de lineal, y offset a la entrada de algunos mV, utilizando una tecnología CMOS de 0.8 micras de largo mínimo de canal. La aplicación requiere la asociación serie-paralelo de un gran número de transistores, y polarización con corrientes de hasta pico-Amperes, lo que constituye una situación poco frecuente en circuitos integrados analógicos. En este marco el diseñador debe elegir los modelos de transistor con sumo cuidado. Un aspecto central de esta tesis es también, el estudio y presentación de modelos adecuados de ruido y offset, que no resultan obvios al principio.

En los primeros dos capítulos se realiza una introducción y se revisa, utilizando el modelo ACM, diferentes características del transistor MOS en función del nivel de inversión.

En el capítulo 3 revisa la pertinencia y consistencia frente a la asociación serie-paralelo, de los modelos usuales de ruido de flicker o 1/f, y térmico. Luego se presenta, incluyendo medidas, un nuevo modelo físico, consistente, simple, y válido en todas las regiones de operación del transistor MOS, para el ruido de flicker. Como corolario a este estudio se presenta un nuevo modelo para estimar el desapareo entre transistores, en función no solo de la geometría, pero también de la polarización. Se demuestra la correlación, debido a su origen físico análogo, entre el ruido de flicker y el offset por desapareo que puede ser visto como un ruido en DC.

En el capítulo 4 se presenta el diseño de OTAs con rango de linealidad extendido, y muy baja transconductancia, utilizando división serie-paralelo de corriente. Se presentan herramientas precisas para la estimación de offset y ruido y se demuestra la utilidad de la técnica para reducir el offset en espejos de corriente. Se presenta el diseño y medida de diversos OTAs.

En el capítulo 5, las herramientas desarrolladas, y los OTAs presentados, son empleados en el diseño del filtro descripto para un acelerómetro piezoeléctrico. Se establece una metodología general para el diseño de filtros G_m-C con características similares. El filtro se fabricó y midió, operando en forma satisfactoria, con un consumo total de 230nA y hasta los

2V de tensión de alimentación, con ruido y offset a la entrada de tan solo 2-4μV_{rms}, y 18μV respectivamente.

El desarrollo de un nuevo modelo de ruido 1/f para el transistor MOS, el estudio de la influencia del offset frente a la asociación serie-paralelo y su aplicación en OTAs, la metodología de diseño empleada, la demostración del uso de técnicas novedosas en una aplicación como la elegida que tiene relevancia tecnológica e interés académico; esperamos que todo ello constituya una contribución valiosa para la comunidad científica en microelectrónica y un conjunto de herramientas de utilidad para el diseño de circuitos.

Very Large Time Constant G_m-C Filters.

Abstract:

In this study a set of tools for the design of fully integrated transconductor-capacitor (G_m-C) filters, with very large time constants and current consumption under one micro-Ampere are presented. The selected application is a 2nd order bandpass-filter-amplifier, with a gain of 400 from 0.5 to 7Hz, carrying out the signal conditioning of a piezoelectric accelerometer which is part of an implantable cardiac pacemaker. The main challenge is to achieve very large time constants, without using any discrete external component. The chosen circuit technique to fulfill the requirement is series-parallel current division applied to standard symmetrical transconductors (OTAs). These circuits have demonstrated to be an excellent solution regarding their occupied area, power consumption, noise, linearity, and particularly offset. OTAs as low as 33pS -equivalent to a 30GΩ resistor-, with up to 1V linear range, and input referred offset of a few mV, were designed, fabricated in a standard 0.8 micron CMOS technology, and tested.

The application requires the series-parallel association of a large number of transistors, and the use of bias currents as low as a few pico-Amperes, which is not very common in analog integrated circuits. In this case the designer should employ maximum care in the selection of the transistor models to be used. A central aspect of this thesis was also to evaluate and develop noise and offset estimation models which was not obvious in the very beginning of the research.

In the first two chapters an introduction to the target application is presented, and several MOS transistor characteristics in terms of the inversion coefficient -using the ACM transistor model- are evaluated.

In chapter 3 it is discussed whether the usual flicker and thermal noise models are consistent regarding series-parallel association, and adequately represent the expected noise behavior under different bias conditions. A consistent, physics-based, one-equation-all-regions model for flicker noise in the MOS transistor is then presented. Several noise measurements are included demonstrating that the new model accurately fits widely different bias situations. A new model for mismatch offset in MOS transistors is presented, as a corollary of the flicker noise analysis. Finally, the correlation between flicker noise and mismatch offset, that can be seen as a DC noise, is shown.

In chapter 4, the design of OTAs with an extended linear range, and very low transconductance, using series-parallel current division is presented. Precise tools are introduced for the estimation of noise and mismatch offset in series-parallel current mirrors, that are shown to help in the reduction of inaccuracies in the copy of currents with a large copy factor. The design and measurement of several OTA examples are presented.

In chapter 5, the developed tools, and the OTAs shown, are employed in the design of the above mentioned filter for the piezoelectric accelerometer. A general methodology for the design of G_m-C filters with similar characteristics is established. The filter was fabricated

and tested, successfully operating with a total power consumption of 233nA, up to a 2V power supply, with an input noise and mismatch offset of 2-4μV_{rms}, and 18μV respectively.

To summarize the main results obtained were: The development of a new flicker noise model, the study of the effect of mismatch regarding series-parallel association, a new design methodology for OTAs and G_m-C filters. It is our hope that this constitutes a helpful set of tools for the circuit designer.

Agradecimientos

Esta tesis es el resultado de más de tres años de trabajo el cual no hubiera sido posible sin la ayuda que he recibido de muchas personas e institutciones. Quiero transmitirles mi más sincero agradecimiento.

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Very Large Time Constant G_m-C Filters

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Chapter 5 - A Fully Integrated 0.5-7Hz, 40db/dec, CMOS Bandpass Amplifier.

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Chapter 1:

Introduction.

Modern trends in electronics require more and more portable applications, where it is mandatory to reduce energy consumption [1,2]. This group of applications includes implantable medical devices which microelectronics technology is steadily contributing to develop. Low power consumption is crucial in the case of pacemakers - the most widespread active implant - , where batteries need to last for years [3,4]. On the other hand, circuits must be extremely reliable since they may be life supporting devices for the patient. Other sources of energy have proved impractical in most cases [3], and since the replacement of batteries requires a surgical -though simple- procedure, the need arises for minimizing power consumption to extend device lifetime. A cardiac pacemaker is nowadays a complex electronic circuit performing several sensing, control, and stimulation functions [3-5] to reestablish a normal rhythm to a diseased heart. In addition, modern pacemakers have the ability to communicate with external units to monitor the patient, and program or supervise the pacemaker. The realization of complex but reliable circuits restricted to a few micro-Amperes of current consumption, is a major quest for the pacemaker manufacturer that normally incorporates custom integrated circuits for the task, not only due to power consumption, but also to reduce to a minimum the size of the device to be implanted in a human patient.

1.1 BACKGROUND, MOTIVATION AND GOALS.

The Microelectronics Group (GME) [6] at the Instituto de Ingeniería Eléctrica - Universidad de la República (IIE - UROU) is dedicated to the research and development of application specific integrated circuits (ASICs), with emphasis on analog and mixed mode "full custom" design in CMOS technology. Low voltage and micropower applications for implantable medical devices is the main research area. In recent years the GME has designed under an industry contract, an ASIC containing most analog functions for a modern cardiac pacemaker [7,8]. This integrated circuit (IC) or just *chip* has been fabricated in small quantities, qualified, and adopted in the latest pacemaker models [9] from Centro de Construcción de Cardioestimuladores del Uruguay (C.C.C.), a Uruguayan manufacturer and design center of medical devices. The designed circuit integrates cardiac sensing channels, cardiac stimulus, battery sensing, telemetry, and also (physical) activity sensing which is the motivation behind this study [4,5,10].

Activity sensing is a measurement of the physical activity, used in the so-called adaptive pacemakers, which regulate the heart stimulation rate according to the requirements of the patient [3]. For example the heart should beat at a much higher frequency while running than while sleeping; during strenuous exercise the heart rate can increase 250% over its

resting rate. If there is insufficient cardiac output, an active patient may become fatigued while doing exercise and may not be able to continue. Thus, rate adaptation will increase the quality of life in near half the pacemaker holders whose heart cannot self-establish its rate [3].

A rate adaptive pacemaker should measure in some way the rate requirements of the patient particularly in cases of exertion. A simple but robust solution is the use of an accelerometer registering body movement. Because it is non-invasive (the sensing device is placed inside the pacemaker without a direct contact with the human body), this is the preferred technique incorporated in most rate adaptive pacemakers either complimented with another sensed parameter like ventilation rate, venous O_2 saturation, or impedance measurement among others [3]. This study deals with the implementation of an activity sensing circuit based on a commercial discrete accelerometer (the transducer should not be integrated in the same die with the circuit). The objective of the activity sensing signal conditioning circuit, is to obtain an output proportional to the average amplitude of the mechanical movement of the patient. The process requires amplification, filtering, and amplitude estimation of the accelerometer output. This task which appears simple, becomes difficult when dealing with usual pacemaker power consumption restrictions. Because physical activity movements are of very low frequency, the passive components -capacitors, resistors- for a traditional filter become too large to incorporate them into an integrated circuit [11]. A major challenge regarding this circuit is to reduce external components to a minimum, integrating all of them into a single chip.

It is common to classify accelerometers according to their measurement principle: piezoelectric, piezocapacitive and piezoresistive accelerometers [12,13,14], but the classification is not complete and there are other kinds of transducers (i.e. thermal accelerometer[15]). For implantable devices, an accelerometer should be reduced in size and consume very low power. Piezoelectric accelerometers fulfill these requirements and have been successfully incorporated in pacemakers, but their cost is elevated. Piezoresistive accelerometers based on a micromachined Wheatston bridge that respond to acceleration [13], result in attractive option due to their performance and cost. But the low resistance of the bridge, usually in the kΩ range, limits their use in implantable devices due to a prohibitive power consumption when the bridge is biased with a moderate voltage. A possible solution is to sample&hold the signal in the bridge, turning off the sensor during hold time [16]. The solution worked successfully [10], and was the first approach to the activity sensing block in the pacemaker ASIC for C.C.C.. However, owing to difficulties with sensor size and packaging, the circuit was finally adapted to use a piezoelectric sensor. This adapted circuit is the one currently being employed in C.C.C. pacemakers [9]. It performs a bandpass-filtering-amplification at very low frequency (0.5-7Hz) of the sensor signal, and average amplitude estimation, both implemented in continuous-time; the power consumption is 10μW, while its input referred noise is just $18\mu V_{rms}$. However, the actual activity sensing circuitry uses apart from the sensor, more that 10 external components including resistors, capacitors. Since it is desirable to minimize board size and fabrication process, it was important to carry out a case study with the activity sensing circuit and:

1st: *To design a continuous-time activity sensing integrated circuit, ideally with no external components with the exception of the sensor device.*

and:

2nd: *Specifically incorporate the piezoelectric sensor.*

3rd: *Reduce power consumption and increase sensitivity, in comparison to previous designs.*

To implement sub-Hz filters without external components it was necessary to develop very special circuit techniques The high sensitivity required the use of low noise techniques; a power consumption in the μA order and a low power supply voltage were also necessary.

1.2 Thesis contents.

In this study a set of tools for the design of fully integrated transconductor-capacitor (G_m-C) filters [17], with very large time constants, and current consumption under one micro-Ampere are presented. The case study is the signal conditioning circuit for the accelerometer, but particular emphasis is placed on the development of general design methodologies at all levels. The selected circuit technique for transconductors is series-parallel current division applied to standard symmetrical OTAs [18,19] because these circuits have proved to be an excellent solution regarding their occupied area, power consumption, noise, linearity, and particularly offset. A 2nd order bandpass filter amplifier for a piezoelectric accelerometer, in the band from 0.5 - 7Hz with no external components, was successfully designed and tested. The equivalent of a several GΩ resistor was integrated while the largest capacitor used was 250pF.

OTAs in the pS range were designed, requiring an elevated number of series-parallel associated transistors and biasing currents as low as a few pico-Amperes. Although at the beginning was clear that there exist available transistor DC models allowing the accurate representation of series-parallel association of transistors, it was not clear which of the available noise, and mismatch, models were appropriate. A central aspect of this thesis is to evaluate and present adequate noise and offset models.

Next, we present an outline of the contents of each chapter of the thesis.

Chapter 1 - Introduction.
In this chapter, an introduction to the case study -physical activity sensing circuit for rate adaptive pacemakers- is presented. The specifications are defined and the main challenges are highlighted. Although the selection of G_m-C filters is the starting point, other applicable options for the same target circuit are also briefly examined. The major difficulties and benefits in each case are noted. A brief survey of known circuits for the implementation of large time constants G_m-C filters is then presented including capacitance scaling, and several architectures for obtaining linear OTAs with a very low transconductance.

Chapter 2 - Some basic aspects of the MOS transistor: DC-AC models, offset, linearity.
The goal of the second chapter is to introduce the reader to several MOS transistor characteristics. They are revised using the ACM transistor model [20,21,22]. The use of the ACM model allows easy writing of different transistor parameters like node capacitance, or small signal parameters, in terms of the inversion coefficient. In particular, a simple

equation that links the inversion coefficient with the linear range of a differential pair is derived. These relationships will help later in the establishment of a circuit design methodology.

Chapter 3 - Consistent noise models for analysis and design of CMOS circuits.

Chapter 3 begins with a definition of series-parallel association consistency of noise models. It is then investigated whether the usual flicker and thermal noise models are consistent regarding series-parallel association of transistors, and adequately represent the expected noise behavior at different bias conditions. A new consistent, physics-based, one-equation-all-regions model for flicker noise in the MOS transistor is then presented. Several noise measurements are included demonstrating that the new model accurately fits widely different bias situations. Thermal noise is also examined, and the corner frequency f_c is introduced. The bias dependence of f_c is obtained. Flicker and thermal noise models are written in terms of the inversion level coefficient, conciliating the accuracy and consistency of a physics-based approach with the simplicity necessary in design. A design example is then shown using the previously introduced low-noise set of design tools. Finally, a new model for mismatch offset estimation in MOS transistors, as a function not only of the geometry but also of the bias point, is presented as a corollary of the flicker noise analysis. The correlation -due to their analogous physical origin- between flicker noise, that can be seen as a DC noise, and mismatch offset, is demonstrated.

Chapter 4 - Design of OTAs with very small transconductance and extended linear range, using series-parallel current division.

Chapter 4 begins with a revision of series-parallel association properties of MOS transistors. Current mirrors utilizing series-parallel association of transistors are examined particularly regarding mismatch. Precise expressions for mismatch offset and noise are derived. Measurements demonstrating the reduction of mismatch offset due to the use of series-parallel association of transistors in current copiers with a large copy factor are presented. The technique may be applied in several analog circuit blocks like current sources, or transconductors. OTAs using series-parallel current dividers are presented as well as a design methodology for this family of circuits; expressions for total noise, input offset, dynamic range, are also discussed. Finally, several designed, fabricated, and tested OTAs are presented. These OTAs range from 33pS to 28nS, with a linear range from ±150 to ±500mV.

Chapter 5 - A fully integrated 0.5-7hz, 40db/dec, CMOS bandpass amplifier.

The fifth chapter is aiming at designing very low frequency G_m-C filters using series-parallel current division OTAs. A widely general design methodology is established. The detailed design, and test result, for a G≅400 gain, 0.5-7Hz bandpass amplifier is presented, while the design and simulation of a rectifier and 3-second time average are shown. Both bandpass filter-amplifier, and rectifier-time averaging, constitute the activity sensing system described in chapter 1. A final comparison between the performance of this and other filters for implantable medical applications is presented.

Chapter 6 - Conclusions.

In this chapter, a brief resume of conclusions, main contributions, and future research prospects related to this study are presented. A list of related publications at the present is also enumerated.

1.2 CASE STUDY: PHYSICAL ACTIVITY SENSING CIRCUIT.

The range of accelerations, appearing at chest level due to normal human exercise, ranges approximately from $0.007g_{peak}$ to $0.34g_{peak}$. The frequency band of interest is 0.5Hz to 7Hz [5], which corresponds to figures reported in [3] for several studies on acceleration for various activities for the human body. Owing to the force of gravity, physical activity acceleration signals may be immersed in a much higher DC offset up at least ±1g that should be removed. The specified signal chain for the circuit is presented in Fig.1.1. First there is a 2nd order bandpass filter amplifier stage, with a given fixed gain. Second order lowpass and highpass characteristics are required but a fine-tuning in the transfer function is not necessary due to the nature of the application. It is then necessary to estimate the average signal amplitude in the last 3 seconds which is obtained with a rectifier, and a 3-second time averaging.

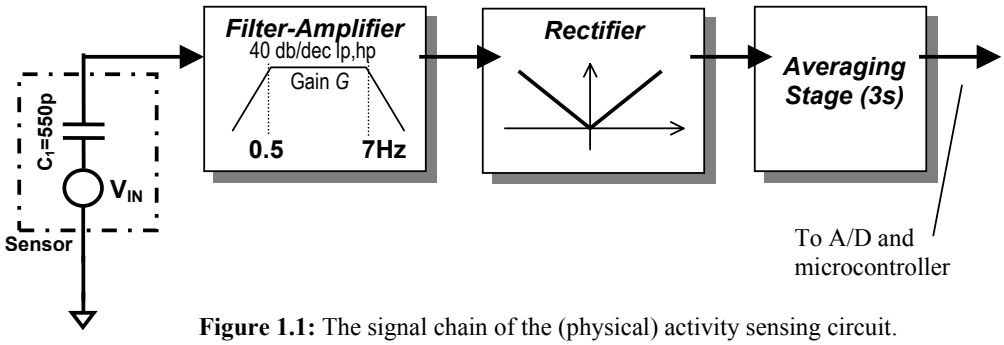

Figure 1.1: The signal chain of the (physical) activity sensing circuit.

The remaining constraint is supply voltage. A 2.8V (nominal) Lithium-Iodine battery normally powers modern pacemakers. Battery voltage decays with time and the pacemaker should be fully operational up to a 2V power supply to guarantee a reasonable time from the low battery condition detection, to pacemaker substitution.[3,7]. The activity sensing circuit must operate up to this voltage with a power consumption budget restricted to less than 3μA [5,7,10].

The critical block in the signal chain is the bandpass filter-amplifier. The reason is that at the rectifier and time averaging stage, low noise is no more critical, and the transfer function is simpler. Throughout this work the focus will be on the bandpass amplifier, and the complete design and test measurements for this stage are presented in chapter 5. Moreover, a very simple rectifier and time averaging design will also be presented in chapter 5, using some of the circuit blocks employed in the bandpass amplifier.

1.2.1 - The sensing element.

Although several kinds of sensors exist -as noted above- for sensing acceleration, we will limit the analysis to the piezoelectric one. A piezoelectric accelerometer is formed by a special material that is sensitive to bending, generating a given amount of charge on its surface depending on the mechanical stress. Two electrodes are connected on the surface of the sensing element, usually a thin slice, to measure the charge. As the sensor is accelerated, a mechanical stress is applied according to Newton's law. Provided there is an adequate

Specification	Min.	Typ.	Max.
Charge Sensitivity [pC/g]	1.4	1.9	2.4
Capacitance		550 pF	
Transverse response			5%
Resistance (25ºC)	10GΩ		
Resistance (150ºC)	100MΩ		
Mechanic Resonance Freq.		9kHz	

Table 1.1: Relevant sensor characteristics.

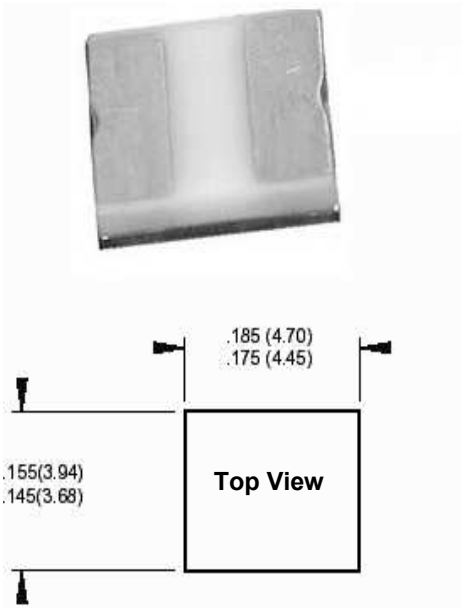

Figure 1.2: Sensor photograph and dimensions in inches(mm).

transducer design, the induced charge is proportional to acceleration. The usual configuration for the sensing element is some kind of cantilever with a privileged axis that allows bending, thus it is capable of measuring acceleration only in that direction. Traditionally, 3 axis accelerometers are built with 3 single sensing elements. Because the sensing material is an isolator, the transducer acts as a capacitor. From the circuit perspective, the measurement can be either seen as a charge generator or as a voltage source in series with a capacitor, as in Fig.1.1 [24].

The selected accelerometer is a PICO12M1A from ENDEVCO [23]. It is a miniature single axis piezoelectric accelerometer. It was selected because C.C.C. had experience in its usage, but also a dedicated search for a better option was carried out without success. In Fig.1.2 a photograph of the sensor, and in Table 1.1 a detailed specification are shown. The specified charge sensitivity and capacitance of the sensor are 1.5pC/g, and 550pF respectively, which is equivalent to a 3.5mV/g sensitivity in the connection scheme of Fig.1.1. At the frequencies of interest in this work, the accelerometer response is approximately flat but it has a mechanical resonance at 9kHz and the response decreases quickly for higher frequencies.

1.2.2 - System Specifications.

With the previous description of the system and the sensor, it is possible to obtain almost all circuit specifications. However, nothing has yet been said about the bandpass amplifier gain *G*, because in principle it is not fixed by the biometric application requirements. In effect, note in Fig.1.1 that *G* may be reduced to one half if the accuracy of the A/D converter is doubled. Now it will be shown that the specifications on value of the bandpass gain, are related to its output offset.

If there is no input signal, at the output of the system in Fig.1.1, an offset voltage is observed corresponding to the output offset voltage of the bandpass filter-amplifier (if rectifier and 3s average are ideally without offset). We expect to detect the minimum signal of 0.007g. For easy detection, the peak amplitude of the signal cannot be less than the offset. On the other hand, for zero offset, the average of a rectified sine wave with amplitude A is $2A/\pi$, regardeless the frequency value. In the plot of Fig.1.3 it is shown how the output of the circuit in Fig.1.1 varies depending on the bandpass output offset voltage, using as a test signal a sine wave of unity amplitude at the bandpass output[1]. We should provide the bandpass-amplifier with enough gain, so that the amplitude caused by the minimum 0.007g ($24\mu V_{peak}$ with a typical sensor) acceleration is high enough in comparison to offset, to recognize it at the output of the averaging circuit. Roughly estimating a 5mV offset in a continuous time offset cancellation loop, and examining Fig.1.3, a gain G=400 is selected so the minimum signal is twice the offset at the output of the bandpass filter[2]. Of course, a more complex offset cancellation circuitry can be used if the detection of very low input signals is critical. But in principle the gain is fixed at 400 which also gives a reasonable $480mV_{peak}$ output value for the maximum typical acceleration to be measured (see table 1.2).

In Table 1.2, a resume of specifications for the circuit is presented. Noise specifications correspond to a in-band rms value equal to the rms voltage produced by the minimum acceleration input to be detected (typ.- $24\mu V_{peak}$).

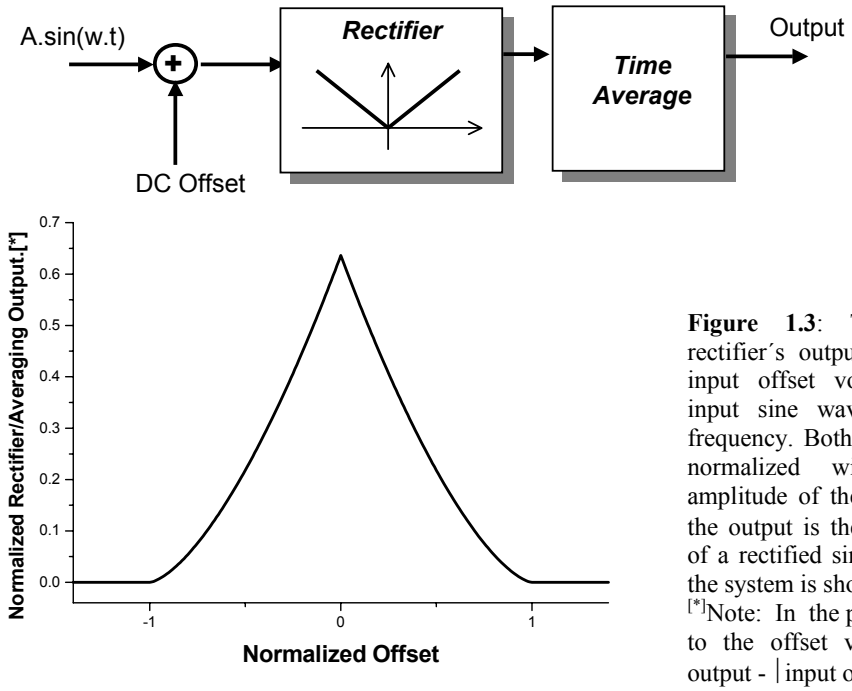

Figure 1.3: Time average of a rectifier´s output as a function of its input offset voltage, considering an input sine wave signal of arbitrary frequency. Both offset, and output, are normalized with respect to the amplitude of the input. At zero offset, the output is the expected $2/\pi$ average of a rectified sine wave. A scheme of the system is shown on the top.
[*]Note: In the plot the output is refered to the offset voltaje (output=average output - |input offset|)[1]

[1] Because on steady state what we measure is offset, and we want to distiguish between steady state and the minimum acceleration output, the absolute value of offset has been substracted in Fig.1.3.
[2] It will be shown in chapter 4, that 5mV is in accordance also with the measured input referred offset of the OTAs that will be employed for offset cancellation in the circuit.

Specification	Requirement
Supply Voltage	2.8 - 2.0 V
Acceleration Range	0.007 - 0.34 g_{peak}
Input Voltage Range	(24 μV_{peak} - 1.2 mV_{peak}) $\pm$ 3.5mV DCoffset (1)
	18 μV_{peak} - 1.5 mV_{peak} (2)
Power Consumption	< 3μA
Frequency Response	Band-pass 0.5-7Hz second order low-pass and high-pass. (3)
Input Referred Noise	< 12μV_{rms} (3)
Input Referred Offset	< 13μV (3)
Total Gain	400 (3)
Others	No external components
	Relaxed tolerance in gain and poles position

(1) Typical values (2) Worst case depending on the charge sensitivity of the sensor (Table 1.1).
(3) Applies only for band-pass filter amplifier section of the circuit.

Table 1.2: Specifications summary for rate adapting sensing circuit.

1.2.3 Challenges.

For implantable applications, a piezoelectric transducer is an ideal choice because:
- It has no power consumption of its own, only that of the signal conditioning circuitry.
- It can be found in very small packages for OEM applications.
- It has an adequate sensitivity.

But the signal conditioning circuit presents several challenges:
-At the minimum frequency of interest, the 550pF sensor capacitance represents a 580MΩ impedance so the sensor can be represented as a voltage source with an enormous series impedance. Also note in Fig.1.1 that the upper node of the accelerometer is floating unless the measuring circuit provides some kind of virtual ground. So the sensor cannot be simply connected to an infinite input impedance amplifier.
-Due to the prescence of the force of gravity there is, at the input of the amplifier, a small signal immersed in a much higher DC offset (or more precisely voltage steps) that must be removed at the first stage of the amplifier to avoid saturation.
-The circuit must operate at low voltage, with extremely low power consumption, it must be low-noise, and with a reduced offset at the input.
-All these restrictions must be overcome without the use of external passive components.

Since fully integrated continuous time filters in the sub-Hz range are a modern research topic, the last point is expected to be the hardest challenge because novel techniques must be combined with low-noise and micro-power restrictions.

There are also two further difficulties to highlight:
-The use of novel techniques requires adequate transistor modeling. Although in principle reliable DC transistor models exist, but the appropriate noise and offset transistor models are not available. An in-depth survey and research study on this topic is presented later in the thesis.
-Although a pacemaker is a self-contained circuit in a titanium case very close to an ideal Faraday jail, capacitive or inductive coupled noise may strongly affect the sensor output due to its enormous output impedance. Noise may be coupled, for example, into the pacemaker through the stimulation leads acting as an antenna, or internal switching noise may be coupled to the sensor.

It is important to remark that, fortunately, activity sensing with the accuracy necessary in a rate adaptive pacemaker does not require a precise position of the poles in the bandpass filter nor a precise gain, so constrains are relaxed in this sense. No tuning is required if the dispersion due to technology parameters of the filter response is not exaggerated. Also size is not an important restriction. For example, capacitors up to a few hundred pF are allowed.

1.3 DIFFERENT CIRCUIT OPTIONS.

In this section a brief discussion on the different possibilities at system and circuit level for the target circuit is presented, focusing on the bandpass filter amplifier that is the critical section of the signal chain in Fig.1.1.

To start, in the picture of Fig.1.4 a discrete circuit, similar to the first of a two-stage bandpass amplifier used in a commercial pacemaker is shown. The circuit uses also a piezoelectric accelerometer. The transfer function of the circuit is:

$$H_1(\omega) = \frac{V_{Out}}{V_{IN}} = \frac{j\omega R_2 C_1}{\left[j\omega R_2 C_1 + (1 + j\omega R_2 C_2).(1 + j\omega R_1 C_1)\right]} \cdot \frac{\left[R_4(1 + j\omega R_3 C_3) + R_3\right]}{R_4(1 + j\omega R_3 C_3)} \quad (1.1a)$$

$$H_1(\omega) \approx \frac{R_3}{R_4} \cdot \frac{j\omega R_2 C_1}{\left[1 + j\omega\left((R_2 + R_1)C_1 + R_2 C_2\right) - \omega^2 R_1 C_1 R_2 C_2\right]} \cdot \frac{(1 + j\omega R_4 C_3)}{(1 + j\omega R_3 C_3)} \quad (1.1b)$$

Equation (1.1b) is a bandpass transfer function with a maximum gain approximately equal to 4.5 at 2.6Hz. Even with an R_3/R_4 ratio of 100, the reduced gain of the stage comes from the voltage divider formed by $Z_1=R_1+1/sC_1$ and $Z_2=R_2\|1/sC_2$ that gives $e^+ << V_{IN}$. Since C_1 at the frequency of interest represent an enormous impedance, the input voltage is reduced unless an R_2 resistor in the GΩ range -which is unpractical- is used. R_2 cannot be removed because it provides the necessary DC bias to node e^+, which would then be floating.

The circuit in Fig.1.4 is a well-known solution for piezoelectric sensors [24]. Despite the voltage division being not-efficient, it has been successfully employed in rate adaptive pacemakers, using the target accelerometer. However, it seems impossible to integrate such a circuit into a chip because capacitors in the nF range, and resistors in the MΩ range, will occupy an unrealistic silicon area. The design of a fully integrated circuit performing the same task as the one in Fig.1.1, requires a different circuit architecture. In this study we

explored for the Gm-C filter techniques (a continuous-time family of circuits), but at this point is necessary to present a brief survey of other options as well as a discussion on known Gm-C filters with very large time constants.

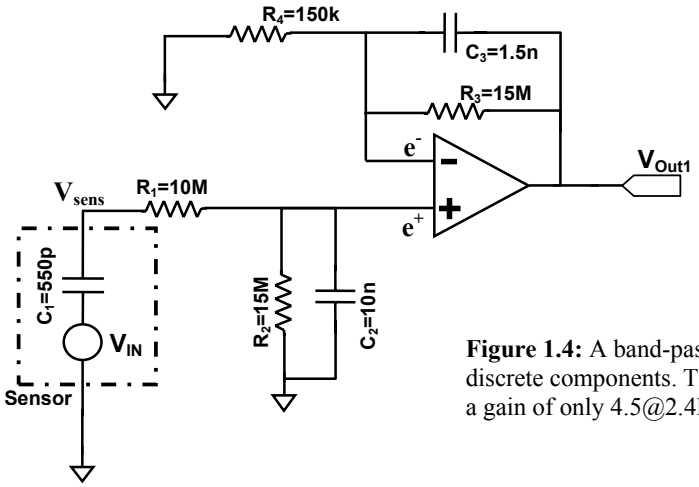

Figure 1.4: A band-pass filter amplifier using discrete components. This amplifier provides a gain of only 4.5@2.4Hz.

1.3.1 - Discrete-Time and Continuous-Time filters.

A digital filter performs its task operating with quantized samples of the input signal that are obtained with some kind of A/D converter. On the other hand, an analog filter, discrete or continuous-time, processes the signal itself, without a quantizer. The difference between a continuous-time (i.e.G_m-C), and a sampled-signal (i.e. switched capacitor [25,26,27,28], or switched current [29]) analog filter, is that the former processes the whole continuous time signal while the latter performs calculations using discrete-time analog samples and state variables.

A first option to implement the signal chain in Fig.1.1 may be to digitalize the signal of the accelerometer, and then filter, rectify, and average it in the digital domain. Although it is not possible to affirm that this solution is not suitable, it was nonetheless discarded. An A/D converter is a mixed-signal circuit that requires signal adaptation, and low noise operation with, in this case, micropower current consumption. Additionally, sensor DC bias is necessary as well as some kind of anti-aliasing filter. Summarizing, the A/D requirements are as complex as those in Table 1.2, and it seems that the total circuit including the A/D and digital filter, would become very complex, with more power consumption and a large circuit area. Even supposing that at least an A/D converter is required as depicted in Fig.1.1, a dedicated A/D converter for the accelerometer signal prcocessing is not necessary. The A/D converter of Fig.1.1 (and in fact is the solution currently being employed in the comercial pacemaker chip of [7],[8]) can multiplex the output of several analog blocks included in a pacemaker and it can cosume a relatively high current because is turned on once each 3 seconds for a very short time.

The second possibility is some kind of discrete-time filter that allows the implementation of large time constants just by using a low frequency sampling rate; which is their main advantage in the case under study. The switched capacitor technique seems to be particularly suitable since it has been successfully used in very low frequency applications for implantable devices (i.e.[27]). It is also a well-known technique that allows the implementation of low-noise circuits with reduced power consumption. The disadvantages of this technique are the need to avoid signal aliasing, and the difficulty in providing adequate biasing to the sensor without employing an extremely complex circuit. Note for example that although the sensor capacitance C_1 at the input may be used for the charge transfer in a switched capacitor filter, it is not clear how to connect it for charge-discharge at the different phases in a switched circuit, and probably some kind of analog continuous-time circuit will be required.

Continuous-time filters are the third option. Because no exact tuning is required the filter can be implemented with a reduced number of circuit elements, and minimum power consumption. The major challenge with this technique is to integrate very large time constants into a standard CMOS technology. The two traditional families of continuous time filters are Mosfet-Capacitor (Mosfet-C) filters, and Transconductor-Capacitor(Gm-C) filters.

G_m-C was the preferred circuit technique because it seems able to provide an extremely simple solution and is thus more likely to consume less area and power. However, designing the circuit either with discrete-time and continuous-time filters seems possible. In fact, a switched capacitor signal conditioning circuit with the above described transfer function has been previously designed for a piezoresistive accelerometer [30] with an adequate area and power consumption.

1.3.2 - MOSFET-C filters.

In Mosfet-C filters, MOS transistors operating in the linear region substitute resistors of a traditional active filter [31,32]. The technique has become widely popular due to its simplicity, because differential structures are easy to implement, and also because the circuits are very easy to tune just by changing the gate voltage of MOS resistors. In Fig.1.5(a) a basic MOSFET-C integrator is shown, with a time constant $\tau = R_{ch}C_{\text{int}}$, where R_{ch} is the channel resistance of the MOS operating in the linear region, controlled by the voltage V_{ctrl}. Simple modification of the basic cell allows the construction of efficient differential structures [31,32]. However, channel resistors are limited to a few MΩ which is not enough to implement filters in the sub-Hz range as needed. As far as we know there are no special techniques to increase the resistance of MOS transistors in the linear region, up to GΩs or hundreds of MΩs, while preserving an adequate linear range. MOS only current dividers (MOCDs) [33] offer a possible option to overcome the problem, and have been previously used in the design of continuous-time filters [34]. In Fig.1.5(b) a possible MOCD integrator that takes advantage of current division in the MOS ladder for a very slow charge the capacitor C_{int} is shown. The time constant of the circuit in Fig.1.5(b) is multiplied by 8 using the same capacitor, transistor, and control voltage of Fig.1.5(a). By using an 8-step MOCD, the current division factor is 256 and so on. But the structure as shown is very sensitive to offset in the operational amplifier because there is a resistance approximately equal to $2R_{ch}$ seen between both inputs of the amplifier e^+, e^-. Because the node e^- is not an ideal virtual ground, this resistance also takes current from the capacitor. For a reduced

number of steps in the MOCD the effect is negligible, but for the division factors required in our application the effect is unacceptably high as was observed in simulations.

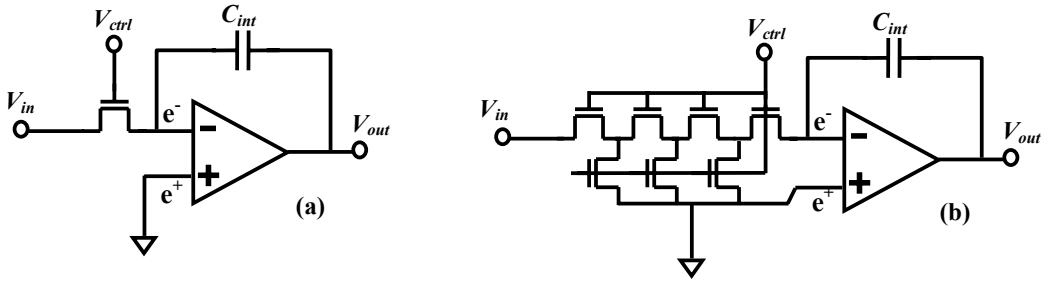

Figure 1.5: (a) A basic MOSFET-C integrator (b) a possible MOCD-C integrator to implement a very large time constant.

1.3.3 - G_m-C filters.

G_m-C filters rely on transconductors (named also OTAs or active voltage to current converters) and capacitors to obtain the desired transfer function of a filter [17]. In Fig.1.6 a basic G_m-C lowpass filter is shown with a transfer function:

$$H(\omega) = \frac{G_{m1}}{G_{m2}} \cdot \frac{1}{\left[1 + j\omega \frac{C}{G_{m2}}\right]} \tag{1.2}$$

Since in G_m-C filters the positions of the poles are given by C/G_m ratios, the main problem is to obtain time constants large enough for the needs of a 0.5-7Hz bandpass amplifier. Integrated capacitors when limited to a reasonable area are in the order of a few hundred pF, while transconductances usually range up to a few tens of nS. Thus, the cutoff frequency in Fig.1.6 is in the best case, around 100Hz unless special circuit techniques are employed.

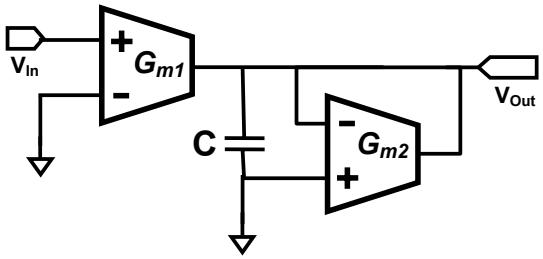

Figure 1.6: A basic G_m-C low-pass filter.

In Fig.1.7, a classical symmetrical OTA is shown. Voltage to current conversion is carried out in the input differential pair M_1 while the other transistors just copy the current to the output. A typical transfer function -output current vs. input differential voltage- is shown in Fig.1.8 for M_1 transistors sized W/L=100µm/10µm with 4nA bias current each. Although M_1 can be

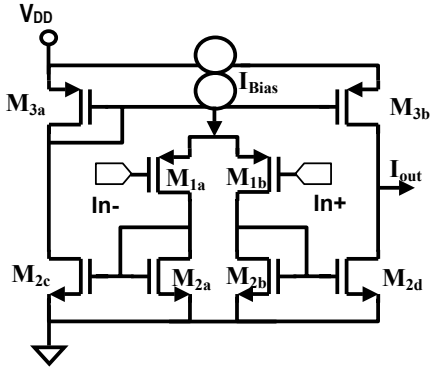

Figure 1.7: An standard symmetrical single ended OTA.

biased with an extremely low current [35], thus obtaining an extremely low transonductance, the problem is the poor linearity. Effectively, as the bias current is lowered M_1 enters the weak inversion region and the range of operation of the OTA is reduced to 60-70mV at the input; for greater input voltages the OTA is no longer linear and there is a considerable distortion in the circuit. It is possible to resume the problem of the large time constants G_m-C filters as follows: to increase its linear range while preserving low noise, low offset, and a reduced area and power consumption. Different circuit techniques have been shown to improve OTAs in this way, some of them are presented and classified in the following section.

1.4 - VERY LOW FREQUENCY G_m-C FILTERS SURVEY.

Several studies have reported the implementation of transconductors and very low frequency Gm-C filters, mostly for biomedical applications [36-47]. Techniques are widely different but it is possible to initially divide them into those that implement very low transconductance OTAs, and those that simulate large capacitors.

Different circuit techniques have been employed in the past to implement very low transconductance OTAs, with an extended linear range. In [48] a brief tutorial focused in linearization techniques for OTAs is presented, while in [36] an interesting comparative study of different linearized OTAs in the nS range is shown.

Although the working principle and circuit topology of very low transconductance OTAs is different in all cases, a rough classification may include:

-Those techniques that modify the differential pair to operate the MOS transistor with a different configuration performing the voltage-to-current conversion in such a way to reduce the transconductance of the pair itself, and increase its linear range.
-Those techniques that use current cancellation, or current division to divide the OTA transconductance by a desired factor (do not increase input linear range).
-Voltage division techniques for the extension of the linear range.

Of course, techniques can be combined. A brief discussion of each follows.

In Fig.1.9, three different modifications of a differential pair that may substitute that in Fig.1.7 to increase the linearity while reducing the transconductance, are shown. Source degeneration in Fig.1.9(a) is a well-known technique to increase linearity by means of a resistor between sources of input transistors, which are now biased with independent current sources. In Fig.1.8 the effect of this linearization, using a 20MΩ resistor, is shown. The linear range has been greatly enhanced, however, the resistor value is too large for an integrated circuit. A better solution is the active source degeneration of Fig.1.9(b) where the resistor has been substituted with a MOS transistor operating in the linear region [46-48]. An improved version of this circuit is proposed in [49] using 2 linearization transistors[3]. The architectures may be made more complex to extend the linear range. For example, Sharpeshkar et al. in reference [37], present the linearized pair of Fig.1.9(c) combining gate

[3] The topology, that will be examined later in chapter 4, is shown on Fig.4.10.

degeneration, bulk driven transistors, and the so called *bump transistor* technique, to achieve a transconductor of 10nS with a linear range of ±1.7V consuming less than 1μW. Among others, the list of examples includes also floating gate transistors, bulk driven transistors [36], etc. However, modified-differential pairs are limited to a few nS in their transconductace. Further reduction of the transconductance requires the use of current division/cancellation schemes. Another aspect to observe regarding G_m-C filters is that complex transistor configurations may result in an excessive mismatch offset or noise. For example, the offset when calculated, is several times greater in the circuit in Fig.1.9(c) than in a standard differential pair using the same input transistor.

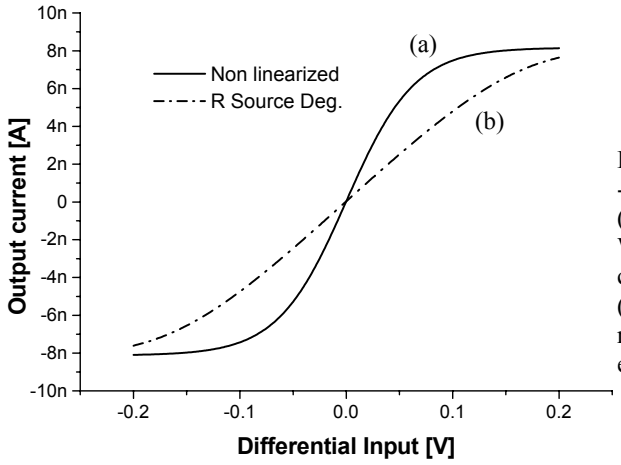

Figure 1.8: The simulated output transference - output current vs. input voltage - in:
(a) a standard symmetrical OTA with WL=100/10 input transistors and 8nA bias current.
(b) source degenerated pair with a 20MΩ resistor (Fig.1.9(a)), bias currents are 4nA each.

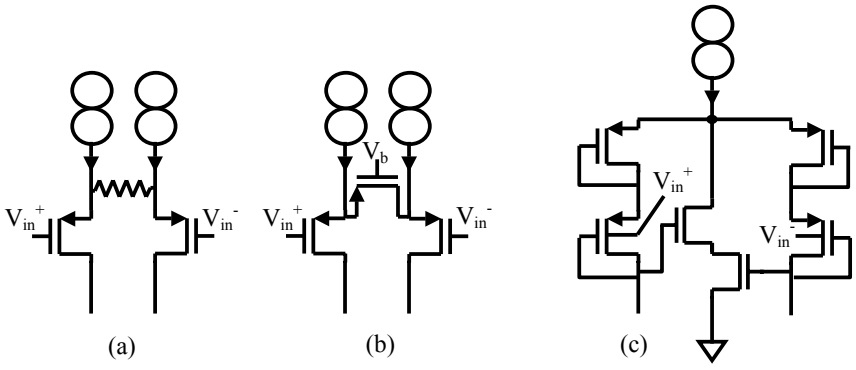

Figure 1.9: (a) a source degenerated differential pair using a resistor, (b) active source degeneration with a transistor, (c) bulk-driven, gate degenerated pair with NMOS 'bump' transistors from reference [37].

A modified differential input pair is, in most cases, sufficient to design an OTA with good linearity and reduced transconductance. This is not the case for the target application that requires OTAs of several pS. Such transconductors should combine also current division or current cancellation.

The basic current division technique consists of substituting $M_{2a,b}$ transistors in Fig.1.7, with a transistor wider than $M_{2c,d}$. Classical *N*:1 factor NMOS current mirrors are implemented with *N* transistors in parallel copying to a single one as in Fig.1.10. The major drawback of this circuit is the enormous area if for example a 1000:1 copy factor is needed, but other drawback is the elevated input referred mismatch offset and flicker noise -as will be discussed at the beginning of chapter 4-. A simple modification to this circuit is series-parallel current division [18,19] as shown in Fig.1.11. There, 3 transistors are series-parallel connected in a standard OTA in order to divide its transconductance by 9. If for example, 8 series-parallel transistors are used instead of only 3, the division factor is 64, and so on. In reference [18] a 2120 division factor is used to obtain a 150pS OTA using a scheme close to that in Fig.1.11; a 500ms time constant integrator is also shown. As far as we know, this is the only reference where series-parallel current division is applied to Gm-C filters.

A current cancellation scheme is shown in Fig.1.12 [38]. In this circuit the OTA small signal transconductance is given by $G_m = \frac{N-1}{N+1} g_{m1}$, where N is the ratio between the transconductance g_{m1} of M_1 and g_{m2} of M_2. The major limitation of this circuit is its sensitivity to offset and noise which, normally limits the range of N to 0.5-0.9 [38]. Offset and noise originate from the elevated currents that are subtracted in the output branch. It should be pointed here, that current division or current cancellation does not increase the linear range of an OTA, it just reduces its transconductance by a given factor *N*.

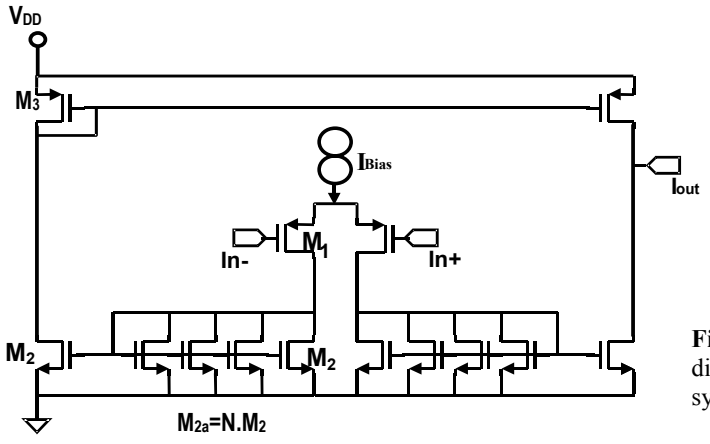

Figure 1.10: Classic 1/N division scheme in a symmetrical OTA.

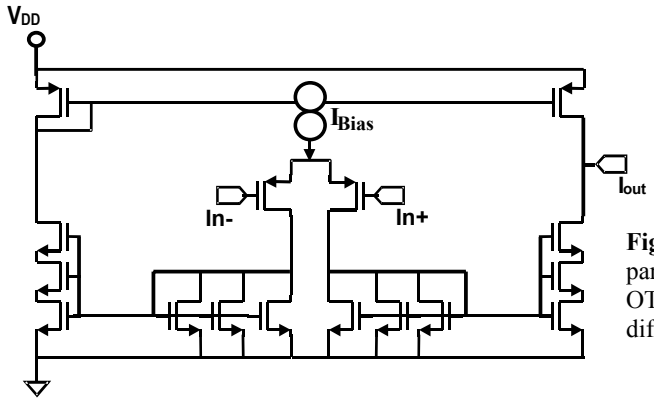

Figure 1.11: A 1/9 series-parallel current division OTA with a standard differential input pair.

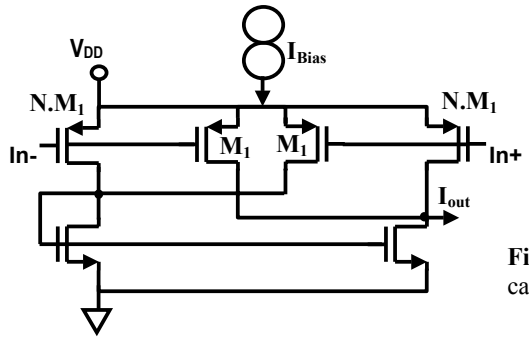

Figure 1.12: Current cancellation technique

The last OTA reduction technique is simple voltage attenuation at the input for example by means of a resistive divider. In this way the transconductance is divided, and the linear range multiplied. A capacitive [41] or active voltage attenuation can be used for reduced power consumption. Although the technique can be successfully employed in the design of a filter in the Hz range [41], it seems unwise for our case study where a considerable gain, reduced noise, and offset are required. The reason is because the technique uses attenuation at the input, and therefore degrades the signal to noise (offset) ratio of the transconductor.

Finally impedance scaling should be considered. It is a well known technique that allows the multiplication or division of a given impedance, either resistive or capacitive [39]. In Fig.1.13, a basic capacitor multiplication circuit is shown. Regardless of the way in which such a circuit is implemented, the input current is: $i_{in} = [j\omega C(1+N)]v_{in}$ so the capacitor is multiplied by a factor (1+N). Scaled capacitors may be employed even in switched capacitor filters for the reduction of capacitance spread [39], and may help to reduce noise [44]. In [39] there is a review of several impedance scaler circuits for capacitors and resistors in CMOS technology. Although the technique seems to be helpful for the design of low frequency filters, offset and noise increase depending on the scaler topology. Also, for very low frequency applications, scaled capacitors are limited and should be complimented with low transconductance OTAs [43].

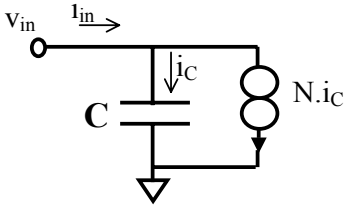

Figure 1.13: Simplified scheme for a capacitor scaler.

By using one or several of the above mentioned techniques, efficient low frequency G_m-C filters can be obtained. In reference [43], Solís-Bustos et al, present a sixth order 2.4Hz low-pass filter that combines current division-cancellation and source degeneration in OTAs, with capacitance scaling. The circuit occupies a total area of $1mm^2$ in a 0.8µm technology, with an integrated input noise of $50\mu V_{rms}$, and a power consumption of 10µW with a 3V power supply. Veervalli et al in [40] present a 0.8Hz bandpass filter also using capacitance scaling, and a low transconductance OTA. This circuit also features tunable center frequency, consumes 28µW power, and has $210\mu V_{rms}$ input noise. Salthouse and Sarpeshkar in [41] use a capacitive attenuation technique to obtain a 100-200 Hz bandpass filter, consuming only 230nW but with an input referred noise of $780\mu V_{rms}$. Silva-Martínez, and Salcedo-Suñer in [38] present a 10Hz , 3^{rd} order lowpass filter, with only $15\mu V_{rms}$ input noise, and 10µW power consumption.

From the latter discussion, it is not possible to select a priori a given G_m-C filter topology for the specifications in Table 1.2. A noise and/or power consumption reduction is required in comparison to surveyed filters in the Hz range, while there is not enough information regarding offset. Although some of the above revised circuit techniques can probably be adapted to the specifications with a very careful design, after a brief analysis we finally opted for the employment of the series-parallel current division technique in OTAs, either with a standard input differential pair, or an active linearized one [49]. This is because this circuit is extremely simple, and thus, is more likely not to compromise noise, offset, or power consumption. In spite of the fact that the integrator using the technique in [18] shows an elevated power consumption and input offset, a first approach to the circuit allowed us to conclude that noise, offset, circuit area, and power consumption, can be limited to acceptable boundaries.

1.5 CONCLUSIONS.

The target application has been presented. It is a 0.5-7Hz 2^{nd} order bandpass-amplifier, rectifier, and time averaging circuit for a piezoelectric accelerometer, which is part of an implantable pacemaker. The application is very restricted regarding power consumption, noise and offset. Continuous-time techniques have been selected, and the major circuit challenge is to employ no discrete components outside the IC with the exception of the sensor itself.

Circuit specifications were defined, and sensor characteristics have been presented. A brief discussion on different circuit options for the system has been presented.

Chapter 2:

Some Basic Aspects of the MOS Transistor: DC-AC models, Mismatch, Linearity.

A MOS transistor is a four terminal semiconductor electronic device constituted by a silicon substrate (body or B), two highly doped silicon regions named source (S) and drain (D), and the gate (G), which is an insulated conductive layer deposited over the region that separates source and drain, named the channel. A voltage applied to the gate controls the current flow between source and drain while the body is usually connected to a fixed reference voltage. Depending on node voltages, the transistor may work in different regions, i.e. the linear region where it behaves like a voltage-controlled resistor, and saturation where it behaves like a current source. Additionally each region may occur at different inversion levels: strong, moderate, and weak [50]. The electrical model of the MOS transistor, is a set of equations that link voltages and currents in the device, and other state variables such as charges.

A fundamental step in the design process for an electrical circuit is simulation, where a computer solves a large set of equations representing the circuit topology and the electrical models of the different circuit elements. Transistor models are not required only for computer simulation, but also for an adequate exploration of the design space (either computer aided, or by hand calculation). An adequate parameter sweep cannot be performed using a complex model. During the design process of an integrated circuit, the designer selects the circuit topology and the size and bias point for the transistors. This process may be iterative and to arrive at a good solution, an adequate design methodology should be selected. It is possible to define a design methodology as a design space exploration, based on a given transistor model, that helps in finding an optimal or adequate solution for a given circuit architecture. Although analog circuits are always tuned with the aid of a SPICE-like program (circuit simulator), the design normally begins with a symbolic analysis carried out by the designer.

MOSFET models for analog integrated circuit design should consist of simple, continuous, accurate, single piece expressions, valid over the entire inversion regime of operation. These models should verify fundamental properties, such as charge conservation and the MOS source-to-drain intrinsic symmetry [20]. Moreover, they have to be technologically independent and correctly represent not only the weak and strong inversion regions, but also the moderate inversion region, where the MOSFET often operates. From the designer perspective, models should provide simple expressions with only a few parameters to adjust, which accurately predict transistor operation. They should also be easily handled by circuit simulators employing easy to handle variables, such as currents or charges in transistor nodes. Several models [50] have been developed for MOS transistors. The BSIM[52] model has been widely employed by circuit designers [51], among other reasons, because

integrated circuits manufacturers normally provide BSIM parameters for circuit simulators. BSIM is fully compatible with CADENCE and MENTOR, and Spice which are the standard CAD tools for most of the companies. The major drawback of BSIM is its elevated number of parameters.

During this study three different models were employed at different design stages for SPICE simulation: BSIM3v3[52], EKV[53], and ACM[20-22]. A full performance comparison will not be presented, but briefly, EKV and ACM were preferred since they preserve the series-parallel association properties of transistors. Series-parallel association of transistors is a key technique in the target design of this thesis. In particular, the ACM model was employed for almost all theoretical developments as well as hand calculations at the design stage. It was demonstrated to be an extremely powerful tool to setup a design methodology, from circuit to transistor level. The ACM model was also introduced without major problems in MATLAB[54,55] routines for design optimization. For the above reasons, this chapter starts with a review of the ACM model and principal equations, including DC and small signal parameters for low and medium frequency analysis.

In many analog circuits, MOS transistor noise and mismatch are relevant, and the designer therefore requires adequate mismatch and noise models. A simple model of transistor mismatch is presented in section 2.3, and an improved mismatch model will be described in annex C. Mismatch and noise are also key aspects to be considered in the circuits of chapters 4, 5. Noise transistor models will be extensively discussed in chapter 3.

Finally, as an example of the use of the ACM model, a very simple formula for the linear range of a CMOS differential pair is deduced in terms of the inversion coefficient of the transistor in section 2.4.

Although in this chapter several fundamental characteristics of the MOS transistor are reviewed, the purpose is just to highlight basic aspects for later use, without intending to demonstrate or deeply examine them. In this and the following chapters, an adequate knowledge of MOS transistor physics and its behavior at the different operating regions are assumed. A wide list of classic and modern references that may be consulted for a deep understanding of the different topics is included.

2.1 THE ALL-REGIONS ONE-EQUATION MODEL.

The fundamental approximation of the ACM model is the linear dependence of the inversion charge density Q_I' on the surface potential ϕ_S, which encompasses the weak, moderate, and strong inversion regions:

$$dQ_I' = \left(C_b' + C_{ox}'\right)d\phi_S = nC_{ox}'d\phi_S, \tag{2.1}$$

where n is the slope factor, slightly dependent on the gate voltage, and C_b', C_{ox}' are the depletion and oxide capacitance per unit area, respectively. The drain current in a long-channel transistor is calculated with the aid of (2.1) and the charge-sheet approximation [50]:

$$I_D = \frac{\mu W}{nC'_{ox}}\left(-Q'_I + nC'_{ox}\phi_t\right)\frac{dQ'_I}{dx} \tag{2.2}$$

where x is a coordinate along the channel, μ is the effective mobility, W is the transistor width, and ϕ_t is the thermal voltage. The other specificity of the ACM model is the use of the unified charge control model (UCCM) [56,57] to link the carrier charge density with the applied voltages:

$$V_P - V_x = \phi_t\left[\frac{Q'_I}{Q'_{IP}} - 1 + \ln\left(\frac{Q'_I}{Q'_{IP}}\right)\right] \tag{2.3}$$

where $Q'_{IP} \approx -nC'_{ox}\phi_t$ is the channel charge density at pinch-off, $V_P \cong (V_{GB}-V_T)/n$ is the pinch-off voltage, and V_x, V_T, V_{GB}, are, respectively, the channel potential at distance x, transistor's threshold voltage, and bulk referred gate voltage. As shown in [21] the use of (2.2) in conjunction with UCCM (2.3) gives

$$I_D = -\mu\frac{W}{dx}Q'_I dV_x \ . \tag{2.4}$$

Consequently, the ACM model is fully consistent with the quasi-Fermi potential formulation for the drain current [50]. Substituting (2.1) into (2.2) and integrating along the channel it is possible to write:

$$I_D = \frac{\mu nC'_{ox}\phi_t^2}{2}\cdot\frac{W}{L}\left[\left(\left(\frac{Q'_{IS}}{nC'_{ox}\phi_t}\right)^2 - \frac{2Q'_{IS}}{nC'_{ox}\phi_t}\right) - \left(\left(\frac{Q'_{ID}}{nC'_{ox}\phi_t}\right)^2 - \frac{2Q'_{ID}}{nC'_{ox}\phi_t}\right)\right] \tag{2.5}$$

L is the channel length, while $Q'_{IS(D)}$ are the channel charge densities at source(drain) dependent on V_G, $V_{S(D)}$. Note at this point that the drain current can be expressed as a combination of a forward I_F and a reverse current I_R:

$$I_D = I_F - I_R, \qquad I_{F(R)} = I\left(V_G, V_{S(D)}\right) \tag{2.6}$$

Expression (2.5) can be rewritten in the form:

$$-\frac{Q'_{IS(D)}}{nC'_{ox}\phi_t} = \sqrt{1+i_{f(r)}} - 1 \tag{2.7}$$

where the forward and reverse normalized currents have been introduced:

$$i_f = \frac{I_F}{I_S}, \qquad i_r = \frac{I_R}{I_S}, \qquad I_S = \frac{\mu nC'_{ox}\phi_t^2}{2}\cdot\frac{W}{L} \tag{2.8}$$

I_S is the so-called normalization current. The forward-normalized current is also properly referred to as the inversion coefficient because it indicates the inversion level of the device [58]. For i_f values greater than 100 the transistor is in strong inversion while i_f values smaller than 1 indicate weak inversion. Intermediate values of i_f indicate moderate inversion. Note that for a saturated transistor, the forward current is much larger than the reverse current ($i_f >> i_r$).

As will be shown, a remarkable and useful characteristic of the ACM model, is that it allows to express, in a simple manner, most DC and AC parameters of the transistor in terms of the inversion level. For example, the relation between normalized currents and node voltages can be derived by using the fundamental approximation of (2.1) in the charge sheet model [21]:

$$V_P - V_{S(D)} = \phi_t \left[\sqrt{1+i_{f(r)}} - \sqrt{1+i_p} + \ln\left(\frac{\sqrt{1+i_{f(r)}} - 1}{\sqrt{1+i_p} - 1} \right) \right] \tag{2.9}$$

$i_p \approx 3$ is the value of the normalized current at pinch-off. The saturation voltage V_{DSsat} can also be deduced from (2.6-2.9) [20]:

$$V_{DSsat} = \phi_t \left[\ln(1/\xi) + \sqrt{1+i_f} - 1 \right] \tag{2.10}$$

where ξ is an arbitrary number, much smaller than 1, related to the saturation level of the transistor. In [20, 21] expressions in terms of the normalized currents of the total inversion (Q_I), depletion (Q_B), source (Q_S), and drain (Q_D) charges are also presented.

2.2 SMALL SIGNAL PARAMETERS.

Small signal parameters defined as the derivatives of the drain current with respect to the node voltages are essential in analog design. For a transistor that is subjected to small variations ΔV_G, ΔV_S, ΔV_D, ΔV_B, at gate, source, drain, and bulk, (Fig.2.1) it is possible to write:

$$\Delta I_D = g_m . \Delta V_G + g_{ms} . \Delta V_S + g_{md} . \Delta V_D + g_{mb} . \Delta V_B \tag{2.11}$$

where $g_m = \left.\frac{\partial I_D}{\partial V_G}\right|_{V_S,V_D,V_B}$, $g_{ms} = \left.\frac{\partial I_D}{\partial V_S}\right|_{V_G,V_D,V_B}$, $g_{md} = \left.\frac{\partial I_D}{\partial V_D}\right|_{V_S,V_G,V_B}$, $g_{mb} = \left.\frac{\partial I_D}{\partial V_B}\right|_{V_S,V_D,V_G}$ are respectively, the gate, source, drain, and bulk transconductances. Note that since a shift in the four node voltages must result in a null current change $\Delta I_D = 0$, it is possible to write $g_m + g_{ms} + g_{md} + g_{mb} = 0$. Thus only three of the four transconductances are independent.

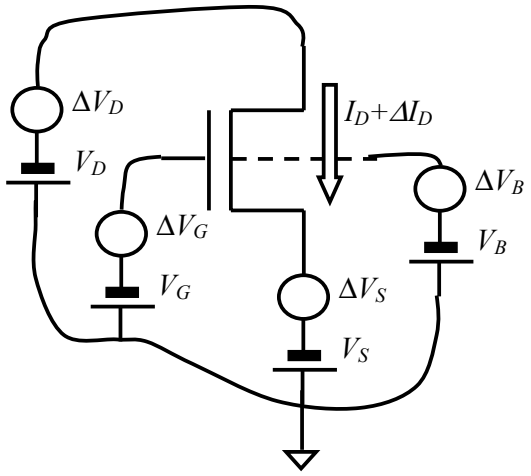

Figure 2.1: Small signal parameter definitions.

The source(drain)-transconductance $g_{ms(d)}$ may be calculated taking the derivative of (2.5):

$$\frac{\partial I_D}{\partial V_{S(D)}} = \mu \frac{W}{L} \phi_t \left(\frac{Q'_{IS(D)}}{nC'_{ox}\phi_t} - 1 \right) \frac{\partial Q'_{IS(D)}}{\partial V_{S(D)}} \tag{2.12}$$

and using the UCCM approximation as in [21] to calculate $\frac{\partial Q'_{IS(D)}}{\partial V_{S(D)}} \cong \frac{nC'_{ox}Q'_{IS(D)}}{Q'_{IS(D)} - nC'_{ox}\phi_t}$.

Consequently:

$$g_{ms} = -\mu \frac{W}{L} Q'_{IS} \tag{2.13a}$$

$$g_{md} = -\mu \frac{W}{L} Q'_{ID} \tag{2.13b}$$

Expressions (2.13) are known as general expressions [50,58] valid in all operation regions for the source and drain transconductances. Using (2.7) these expressions can be rewritten in terms of the inversion levels:

$$g_{ms(d)} = \frac{2I_S}{\phi_t} \left(\sqrt{1 + i_{f(r)}} - 1 \right) \tag{2.14}$$

The gate transconductance (g_m parameter) is essential in analog design. It can be calculated taking the derivative of (2.5) and using UCCM to approximate $\frac{\partial Q'_{IS(D)}}{\partial V_G} \cong -\frac{1}{n} \frac{\partial Q'_{IS(D)}}{\partial V_{S(D)}}$ [21] so, from (2.5) it holds that:

$$g_m = \frac{g_{ms} - g_{md}}{n} \tag{2.15}$$

At saturation $i_f << i_r$ so $g_{md} << g_{ms}$, thus:

$$g_m = \frac{2I_S.i_f}{n\phi_t.\left(\sqrt{1+i_f}+1\right)} \quad ; \quad \frac{g_m}{I_D} = \frac{2}{n\phi_t.\left(\sqrt{1+i_f}+1\right)} \tag{2.16}$$

In the plot of Fig.2.2 both the measured and estimated g_m, and g_m/I_D for a W/L=14µm/3.6µm NMOS transistor are shown. The gate-to-transconductance ratio is an important parameter at transistor level design [59]. The use of the ACM model provides simple analytical expressions, like the one in (2.16), that allow an efficient design space exploration in the inversion level either by hand calculation or with a general programming tool (like MATLAB[54], OCTAVE[55] frequently used in R&D). The interpolation of a curve, previously obtained with a SPICE-like tool, is not required.

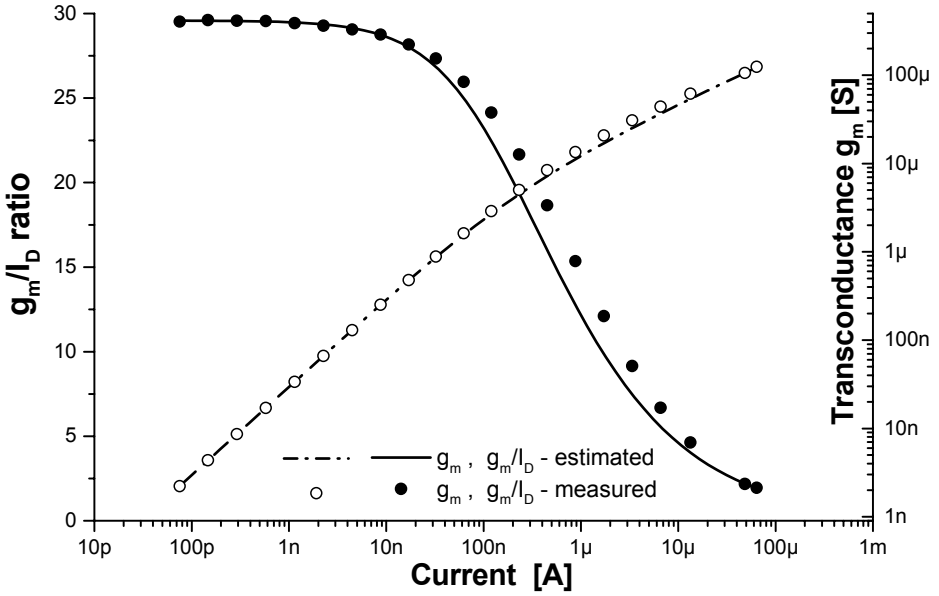

Figure 2.2: Predicted (using (2.16)) and measured transconductance g_m, and g_m/I_D ratio, for a W/L=14.5µm/3.6µm NMOS transistor.

To finish we have the expressions of the intrinsic capacitances, defined as the derivatives of the inversion, depletion, source, and drain total charges (Q_I, Q_B, Q_S, Q_D) with respect to the terminal voltages. In principle it is possible to define 16 capacitances, but only 9 are linearly independent [20,50]. It is possible to deduce the expressions of the capacitances in terms of the inversion levels from the expressions of the total charges. As an example, the result for the gate to source(drain) capacitance is:

$$C_{gs(d)} = C_{ox}\,\frac{2}{3}\left(1-\frac{1}{\sqrt{1+i_{f(r)}}}\right)\left[1-\frac{1+i_{r(f)}}{\left(\sqrt{1+i_f}+\sqrt{1+i_r}\right)^2}\right] \tag{2.17}$$

C_{ox} is the total oxide capacitance of the gate area. In [20] the derivation of the expression for all capacitances is presented.

2.3 MISMATCH MODEL.

There are no two identical transistors, hence two transistors with the same geometry and the same potential at the source, drain, bulk, and gate, will present slightly different drain currents. This random difference in currents is known as mismatch, and it is widely recognized that the performance of most analog or even digital MOS circuits is limited by this phenomenon [60-63,71,72]. The shrinkage of the dimensions of MOSFETs and the reduction in the supply voltage make matching limitations even more important to such an extent that several new studies have been published in recent years [64-68].

It is widely accepted that matching can be modeled by the random variations in geometric, process and/or device parameters. The simplest approach is to consider only variations in the threshold voltage or the current factor. Effectively, when a large number of transistors, each sized W/L, are fabricated in a single die; not all of them will present the same threshold voltage V_T or equal β current factor ($\beta = \mu C'_{ox} W/L$). V_T and β are random variables, usually considered as having normal distribution and standard deviations given by [60,5]:

$$\sigma^2_{V_T} = \frac{A^2_{V_T}}{2WL}, \quad \frac{\sigma^2_\beta}{\beta^2} = \frac{A^2_\beta}{2WL} \tag{2.18}$$

A_{VT}, A_β, are two technology parameters with typical values A_{VT}=13-30mV.µm and A_β=2-4%.µm[70]. For the sake of simplicity, only variations in V_T and β will be considered in this thesis. Nevertheless, all the calculations related to offset that will be here presented can be extended to other models to study the mismatch in MOS transistors [66,67,69], or to obtain more accurate expressions for $\sigma^2_{V_T}$, σ^2_β, which consider, for example, the mismatch dependence on the distance between transistors [60,70]. In analog design, it is common to express mismatch in terms of ΔV_T, $\Delta\beta$, the difference between V_T, β, of two matched transistors. With a careful layout, the dependence of V_T, β, on the distance between the transistors is negligible [60,70] thus $\sigma^2_{\Delta V_T} = 2\sigma^2_{V_T}$, $\sigma^2_{\Delta\beta} = 2\sigma^2_\beta$ [70]. Since offset due to transistor mismatch is a major limitation in analog circuit performance, to reduce it, the designer can increase the area of the transistors (2.18), and should follow as much as possible some layout rules such as providing the same surroundings for the transistors, or using common centroid geometry.

At circuit level what is relevant are variations in the drain current ΔI_D originating from transistor mismatch. A first order analysis can be carried out for transistors with the same geometry and node voltages but fluctuating parameters. Fluctuations in the drain current are:

$$\Delta I_D = \frac{\partial I_D}{\partial V_T}\Delta V_T + \frac{\partial I_D}{\partial \beta}\Delta\beta = -g_m.\Delta V_T + \frac{I_D}{\beta}.\Delta\beta$$

$$\Rightarrow \quad \frac{\sigma^2_{I_D}}{I_D^2} = \left(\frac{g_m}{I_D}\right)^2.\sigma^2_{V_T} + \frac{\sigma^2_\beta}{\beta^2} \tag{2.19}$$

To derive (2.19) it has been assumed that $\partial I_D/\partial V_G = -\partial I_D/\partial V_T = -g_m$ because drain current is a function of $(V_G - V_T)$ (2.9) (this consideration is valid for all MOSFET models). The transconductance to drain current ratio varies from $g_m/I_D \cong 30$ at weak inversion up to 1-2 [73] at deep strong inversion. Considering usual values for $\sigma^2_{V_T}, \sigma^2_\beta/\beta^2$, a rough analysis of (2.19) concludes that mismatch is usually dominated by threshold voltage dispersion, particularly at weak inversion where the circuits that will be presented in this thesis normally operate.

There are several possible ways to improve the model in (2.18). First it is possible to add a term to (2.18) that accounts for the distance between transistors [60,70]. But it is well-known that this correction is negligible unless the distance between transistors becomes large in comparison to transistor size. For the circuits that will be presented here, the layout was carefully drawn (see section 4.5), and such a correction to (2.18) was not necessary. Another possibility is to consider variations in other parameters such as the slope factor [67] in addition to V_T and β. This is essentially what is proposed in some complex mismatch models where several physical, non-correlated, transistor parameters are carefully selected to describe transistor variations. However, an elevated number of parameters to adjust is a major drawback (although of course this will better fit some situations), so the simple model in (2.18) is often preferred by designers. Furthermore, the result of the analysis in (2.19) extended to other MOSFET parameters will normally still be dominated by variations in the threshold voltage.

A third option to improve the mismatch model is to modify the model itself. Eq.(2.18) is the result of the integration of local variations in threshold voltage throughout the channel and consequently, the threshold voltage fluctuation is inversely proportional to the channel area. Such integration assumes that V_T statistics are independent of the position in the channel. An alternative is shown in annex C, where the integration of local variations in V_T along the channel, based on the ACM model, results in a new formulation for mismatch in MOS transistors. The new model is simple, physics-based, consistent, valid in all regions of operations, and has a single technology parameter to adjust.

For the sake of simplicity, the expression (2.18) is employed for mismatch estimation in MOSFETs for the circuits that are here designed. The model has been demonstrated to accurately predict mismatch in several experiments, and it will be shown that it gives a good estimation of the physical model of annex C. Finally, it is important to note that although (2.19) predicts that V_T dominates mismatch at weak inversion, variations in β must be carefully examined in the series-parallel association of transistors. Effectively β is related to transistor geometry through W/L and thus, its effect in the total mismatch of a composed transistor may depend not only on the total gate area, but also on the number of unitary transistors that are series-parallel connected. This topic is discussed in chapter 4.

2.4 LINEARITY OF A MOS DIFFERENTIAL PAIR.

In this section, the ACM model is employed to calculate the linear range of a differential pair in terms of the inversion level i_f of the transistors. For the designer it is very helpful to got available expressions linking the inversion level with several circuit characteristics. As an example, the result of this section will be employed later in chapter 4, to set up a very simple design methodology for special OTAs.

For a given acceptable error α, the linear range V_{Lin} of the differential pair in Fig.2.3 is defined as:

$$\text{if} \quad |V_{in}| < V_{Lin}\ , \qquad \text{then} \quad \left|\frac{I_{diff} - g_{m1}.V_{in}}{g_{m1}.V_{in}}\right| \le \alpha . \tag{2.20}$$

g_{m1} is the gate transconductance of the transistors in the pair, which are sized W_1/L_1. The differential current is $I_{diff} = I_a - I_b$, and the bias current is $I_{bias}=I_a+I_b$ (see Fig.2.3). The definition of linearity in (2.20) is not the most conventional. We preferred to use it instead of IM3 or HD3 (third harmonic distortion expressions) because for our case of study is better to work on signal excurtion rather than on distortion as in RF circuits. However all the expresions here presented can be easy modified to calculate in example HD3 in terms of the invertion level.

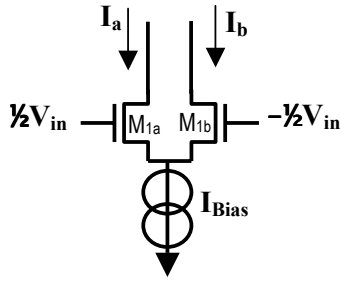

Figure 2.3: A CMOS differential pair.

To calculate $I_{diff}(V_{in})$, the expression in (2.9) is employed: ($i_{fa(b)}, V_{Ga(b)}, V_{Pa(b)}$, are the inversion coefficient, gate voltage, and pinch-off voltage of transistors $M_{1a(b)}$ in Fig.2.3 respectively. Owing to simmetry, when no differential input voltage is applied, $i_{fa} = i_{fb} = i_f$.)

$$V_{in} = V_{Ga} - V_{Gb} = n(V_{Pa} - V_{Pb}) = n\phi_t\left[\sqrt{1+i_{fa}} - \sqrt{1+i_{fb}} + Ln\left(\sqrt{1+i_{fa}} - 1\right) - Ln\left(\sqrt{1+i_{fb}} - 1\right)\right]$$

$$V_{in} = n\phi_t\left[\sqrt{1+\frac{i_b+i_d}{2}} - \sqrt{1+\frac{i_b-i_d}{2}} + Ln\left(\sqrt{1+\frac{i_b+i_d}{2}} - 1\right) - Ln\left(\sqrt{1+\frac{i_b-i_d}{2}} - 1\right)\right] \tag{2.21}$$

i_b, i_d are the normalized bias and differential current, respectively: $I_{diff} = I_S.i_d$, $I_{bias} = I_S.i_b$, with the normalization current being $I_S = \frac{1}{2}\mu C_{ox} n\phi_t^2 (W_1/L_1)$. For fixed i_b, (2.21) defines $V_{in} = f(i_d)$; expanding the inverse function $i_d = f^{-1}(V_{in}) = g(V_{in})$ in series [74]:

$$i_d = \sum_{j=1}^{\infty} k_j . V_{in}^j \qquad k_j = \frac{1}{j!} . \frac{d^j i_d}{dV_{in}^j}\bigg|_{V_{in}=0} = \frac{1}{j!} . \frac{d^j g}{dV_{in}^j}\bigg|_{i_d=0} \tag{2.22}$$

The coefficients up to the third order are calculated with the inverse function derivation rule:

$$g'(i_o) = \frac{1}{f'(i_o)}\bigg|_{i_o=0} = \frac{2i_f}{n\phi_t\left(\sqrt{1+i_f}+1\right)} = \frac{g_{m1}}{I_S} \tag{2.23a}$$

$$g''(i_o) = \frac{-f''(i_o)}{\left(f'(i_o)\right)^3}\bigg|_{i_o=0} = 0 \tag{2.23b}$$

$$g'''(i_o) = \frac{3\left(f''(i_o)\right)^2 - f'(i_o).f'''(i_o)}{\left(f'(i_o)\right)^5}\bigg|_{i_o=0} = \frac{1}{2n^3\phi_t^3} . \frac{\left(\sqrt{1+i_f}-1\right)\left(3\sqrt{1+i_f}-1\right)}{\left(1+i_f\right)^{3/2}} \tag{2.23c}$$

$i_f = i_b/2$ is the inversion level of M_1. In annex A, the explicit calculation of the derivatives of $f(i_0)$ is shown. As expected the second order term in (2.23b) is 0 due to the differential structure. Substituting (2.23) up to the third order in (2.22):

$$I_{diff} = I_S . \left(g'(0).V_{in} + \frac{g'''(0)}{6} .V_{in}^3 + ... \right)$$

$$I_{diff} = g_m . V_{in} + \frac{I_S}{12n^3\phi_t^3} . \frac{\left(\sqrt{1+i_f}-1\right)\left(3\sqrt{1+i_f}-1\right)}{\left(\sqrt{1+i_f}\right)^3} .V_{in}^3 \tag{2.24}$$

Thus, it is possible to estimate the linear range of the differential pair:

$$V_{Lin} = 2n\phi_t \sqrt{\frac{6\alpha\left(1+i_f\right)^{3/2}}{3\left(1+i_f\right)^{1/2}-1}} \tag{2.25a}$$

$$V_{Lin} \approx 3n\phi_t \sqrt{\alpha\left(1+i_f\right)} \tag{2.25b}$$

Eq.(2.25) would be very useful for hand calculations at the design stage of any circuit containing a differential pair. The analysis procedure may also be extended to other circuits like Gilbert multipliers.

2.4.1 Measurements:

The plot in Fig.2.4 shows the linear range of a PMOS differential pair in terms of the inversion level as measured, simulated, and predicted. The measurements were performed varying the bias current of a standard symmetrical OTA with the aid of a HP4155 Semiconductor Parameter Analyzer, the simulated linear range was obtained with SPICE-like software and the ACM model [22], and the predicted curve is obtained with eq.(2.25 a,b). Note the strong similarity between the three plots.

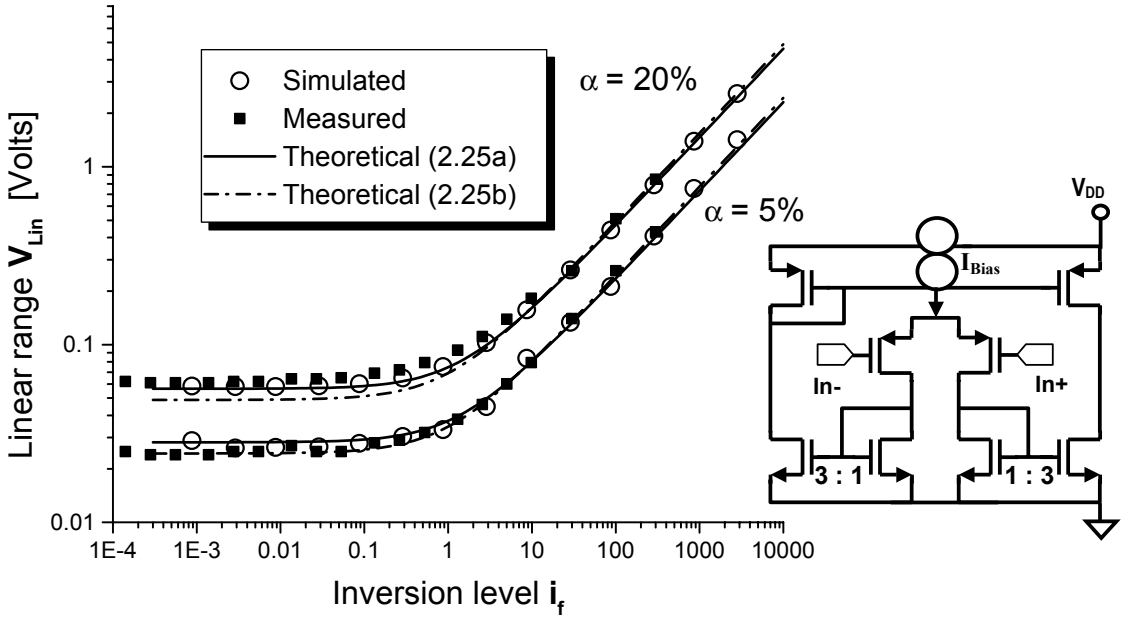

Figure 2.4: Measured, simulated, and theoretical linear range in terms of the i_f of the input pair, for a symmetrical OTA. The measurements were obtained with a symmetrical OTA like the one on the right of the picture.

2.5 CONCLUSIONS.

A brief discussion of the ACM model and its principal equations has been presented. This model is the basis of most theoretical deductions and design methodologies in this thesis. The model allows most relevant transistor parameters to be written in a simple manner in terms of the inversion level, which is a powerful tool for design space exploration. Mismatch models for the MOS transistor have also been discussed.

Finally, to demonstrate its application, the ACM model has been employed to derive a simple expression for the linear range of a MOS differential pair in terms of the inversion level of the transistors.

Chapter 3:

Consistent Noise Models for Analysis and Design of CMOS Circuits.

MOSFET noise is usually expressed as a noise current, a function of the transistor size and bias point, between source and drain as in Fig.3.1. Several physical mechanisms may contribute to the noise current, and at very high frequency gate noise also becomes relevant and should be considered [75]. However, at low and medium frequencies the only noise sources are thermal noise with a flat Power Spectral Density (PSD), and flicker noise with a PSD inversely proportional to the frequency [50,76]. The former occurs due to thermal movement of carriers in the channel, while the latter is a result of random trapping-detrapping of carriers in the channel. The resulting typical noise PSD of a transistor is shown in Fig.3.1 where the corner frequency f_c at which both flicker and thermal noise are equal is also indicated. From the designer's perspective, it is desirable to have noise models that allow an accurate prediction of the noise power spectral density in terms of bias, size and technology of the transistor. These models should not be complex for noise calculation and should employ variables easily handled by a simulator, such as currents or charges in transistor nodes. Another desirable property of a correct noise model is to be consistent regarding series-parallel association of transistors; essentially the noise PSD of a group of series-parallel connected transistors should be the same when calculated for the equivalent transistor, or summing the noise contribution of each single transistor. This property is not frequently discussed in noise related works and particularly series-parallel consistency, for example, is not verified by several common flicker noise models. This chapter starts with a definition of series-parallel consistency of a noise model, presenting as an example, thermal noise in resistors and MOSFETs. But a more interesting case for analysis is flicker noise. The physics behind flicker noise in MOS transistors is still a topic of discussion. It is quite well accepted that the sources of low frequency noise are mainly carrier number and mobility fluctuations due to random trapping–detrapping of carriers in energy states near the surface of the semiconductor [77-87][1]. However, the exact mechanism and the statistics of the resulting noise current, as well as how it is related to technology parameters such as doping concentration or surface quality, are not yet clear.

In this chapter, a physics-based model for the flicker noise in MOS transistors is presented. First, common flicker noise models are revised, concluding that not all of them are self-consistent or adequately represent the expected behavior of flicker noise in all regions of operation. After that, a simple, self-consistent, one-equation–all-regions physics-based model for the flicker noise in long channel MOS transistors is developed. The research on the new model was driven by the interest to find an adequate flicker noise model for the analysis of the circuits in chapters 4, 5, and it forms a main contribution of the present thesis work. The new model uses the approximations, and an integration procedure, based on the ACM model. The integration procedure inherently preserves series-parallel association properties of the noise model.

[1] See annex B for a detailed description of the phenomenon.

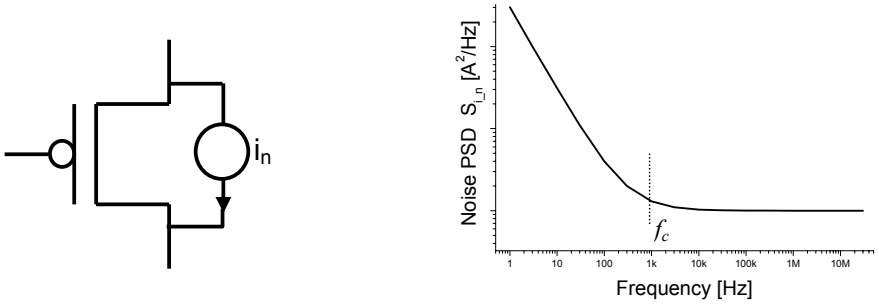

Fig.3.1: A MOS transistor with a noise current i_n that is summed to the ideal drain current I_D. To the right it is shown a typical spectrum of the PSD of the noise current. At low frequencies flicker noise dominates while at high frequency only white noise is relevant. The corner frequency f_c is indicated in the graph.

Because physics-based models of 1/f noise are commonly either too complicated or not general enough for circuit analysis and design [81], analog designers prefer empirical or SPICE models. In this chapter it is shown also that noise models formulated in terms of the inversion level concept [20,53] can conciliate the accuracy and consistency of a physics-based approach with the simplicity necessary in design. The new one-equation physics-based model of the long channel MOSFET flicker noise is rewritten using the inversion level concept. Simple design formulas for the different operating regions are developed. To obtain a complete set of simple noise design equations, thermal noise will be examined and approximated using the ACM model. Classical thermal and flicker noise approximations will be derived, and the proportionality of the flicker noise corner frequency with the transistor transition frequency is proved and experimentally verified under wide bias conditions ranging from subthreshold to strong inversion. Finally a design example consisting of a low-noise, micropower, low-pass filter-amplifier (DC-20Hz,Gain=40) is shown.

3.1 CONSISTENCY OF NOISE MODELS.

A noise model is said to be consistent regarding series or parallel associations when the composition of the noise contributions from individual series (or parallel) elements is the same as the noise from the series (or parallel) equivalent. Obviously, the white noise model (3.1) for a resistor is consistent [88].

$$S_{i_n}(f) = \frac{4k_B T}{R} \tag{3.1}$$

where $S_{i_n}(f)$ is the PSD of the noise current, k_B is the Boltzmann's constant, T is the absolute temperature, and R is the resistor value. For two series elements R_1, R_2 (Fig.3.2(a)) the total noise current introduced into the circuit: $S_{i\_s}(f) = \dfrac{4k_B T}{R_1 + R_2}$ can be obtained with the same result, either by composing the individual noise sources or using (3.1) to calculate the noise of the equivalent resistor $R_{eq\_s} = R_1 + R_2$.

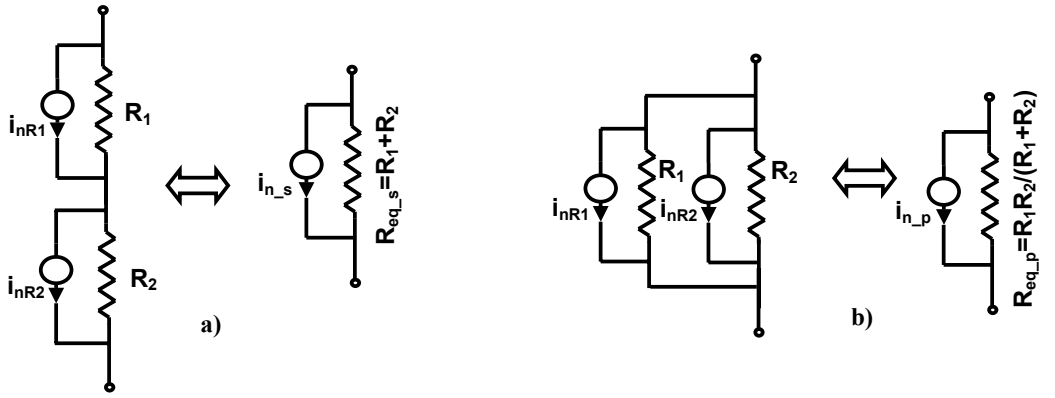

Figure 3.2: a) Two series resistors and their associated noise currents can be seen like a single equivalent resistor with a single noise current. b) Two parallel resistors and their associated noise currents can be seen like a single equivalent resistor with a single noise current.

For two parallel resistors (Fig.3.2(b)) the total noise current introduced into the circuit is also the same calculated either summing the individual noise contribution of each resistor, or using (3.1) to compute the noise current for the equivalent resistor $R_{eq\_p} = \frac{R_1.R_2}{R_1 + R_2}$. Therefore, the model in (3.1) is said to be self-consistent regarding series and parallel association of resistors.

The analysis can be extended to MOS transistors, because for these devices, series and parallel equivalents are well defined (see section 4.1 or references [89,58]). Consider, for example, the virtual cut of a transistor that slices it into two series elements as in Fig.3.3 (a). Suppose that the upper transistor M_u introduces a noise current with a PSD equal to $S_{i_{du}}$, and the lower transistor M_l introduces a noise current $S_{i_{dl}}$. Small signal analysis in Fig.3.3(b) allows the calculation of the PSD of the noise current $S_{i_{d\_s}}$ of the series-composed transistor. Considering non-correlated noise current sources it follows:

$$S_{i_{d\_s}}(f) = \left[\frac{k}{1+k}\right]^2 S_{i_{dl}}(f) + \left[\frac{1}{1+k}\right]^2 S_{i_{du}}(f) \tag{3.2}$$

where $k = \frac{g_{msu}}{g_{mdl}}$, and g_{msu} , g_{mdl} are the source and drain transconductances of transistors M_u and M_l respectively. For the partition of the channel as in Fig.3.3, the use of transconductances expression from (2.13) yields:

$$g_{msu} = -\mu \frac{W}{L-d} Q'_{Ix} \qquad g_{mdl} = -\mu \frac{W}{d} Q'_{Ix} \tag{3.3}$$

where Q'_{Ix} is the inversion charge density evaluated at a point *x* in the channel (Fig. 3.3 (b)).

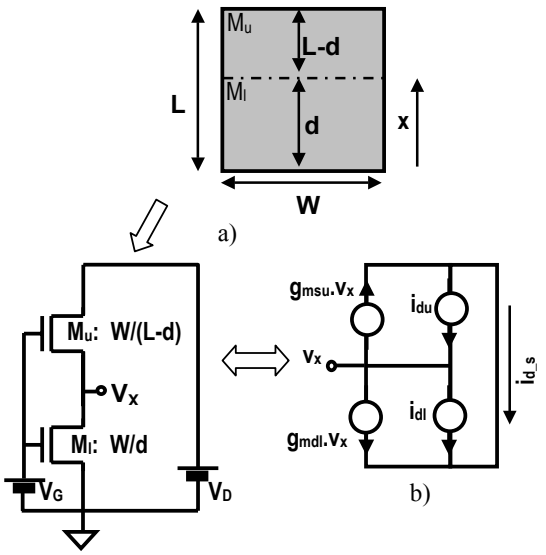

Fig.3.3: a) A sliced transistor.
b) Circuit for the calculation of the total noise produced by two transistors in series.

Consequently, $k = \frac{d}{L-d}$ depends only on the geometry and (3.2) can be rewritten as :

$$S_{i_{d\_s}}(f) = \left[\frac{d}{L}\right]^2 S_{i_{dl}}(f) + \left[\frac{L-d}{L}\right]^2 S_{i_{du}}(f) \tag{3.4}$$

Equation (3.4) must be satisfied in all operation regions for a consistent noise model in terms of series association.

The analysis is simpler for parallel association of transistors. For the case of a virtual split of a transistor into two parallel ones as in Fig.3.4, the sum of the PSD of the noise currents of the left and right transistor must be equivalent to the noise current of the original transistor:

$$S_{i_{d\_p}}(f) = S_{i_{d\_ri}}(f) + S_{i_{d\_le}}(f) \tag{3.5}$$

In (3.5) $S_{i_{d\_le}}$ is the noise current PSD of the transistor on the left, $S_{i_{d\_ri}}$ of the transistor on the right, and $S_{i_{d\_p}}$ of the parallel-composed transistor. Equation (3.5) must be satisfied in all operation regions for a consistent noise model in terms of parallel association.

As an example, let us now consider the application of (3.4), (3.5) to thermal noise. It is well known [50] that the PSD of the thermal channel noise is:

$$S_{iw} = \frac{-4k_B T \mu Q_I}{L^2} \tag{3.6}$$

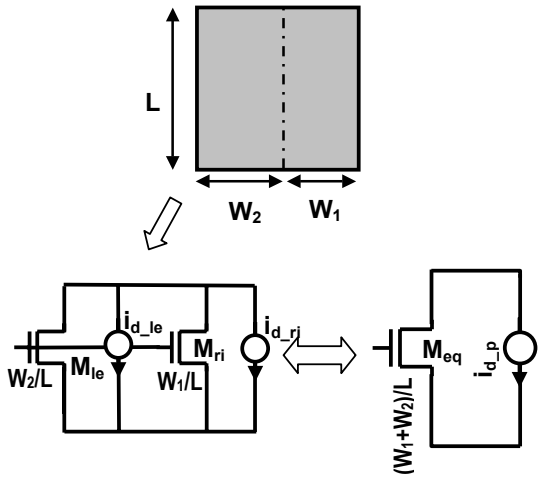

Fig.3.4: Circuit for the calculation of the total noise produced by two transistors in parallel.

where Q_I is the total inversion charge in the channel. For series transistors, calculating the PSD of the upper and lower transistor using (3.6) and substituting into (3.4):

$$S_{iw} = -4k_B T\mu\left[\frac{Q_{Il}}{d^2}\left(\frac{d}{L}\right)^2 + \frac{Q_{Iu}}{(L-d)^2}\left(\frac{L-d}{L}\right)^2\right] = \frac{-4k_B T\mu Q_I}{L^2} \tag{3.7}$$

where Q_{Il}, Q_{Iu}, are the total inversion charge in the channel of the lower and upper transistor respectively.

For parallel transistors as in Fig.3.4, calculating the PSD of the left and right transistor using (3.6) and substituting into (3.5) gives:

$$S_{iw} = -\left[\frac{4k_B T\mu Q_{I_{ri}}}{L^2} + \frac{4k_B T\mu Q_{I_{le}}}{L^2}\right] = \frac{-4k_B T\mu Q_I}{L^2} \tag{3.8}$$

As expected, the classical thermal noise model of the MOSFET is consistent with series and parallel associations of transistors.

Not all noise models are consistent. In Table 3.1, columns 2-3, the series and parallel association properties for some SPICE-implemented flicker noise models [90,91] are presented, showing the limitations of common flicker noise models in this sense. Model NLEV=1 consistently represents the series association of transistors, but NLEV=0 and NLEV=2,3 do not. According to the manual [52], BSIM3v3 uses a different model for strong and weak inversion, both models verify series-parallel association but that is not necessarily true in the interpolation region.

MODEL	SERIES EQUIVALENT	PARALELL EQUIVALENT	NORMALIZED P.S.D.: S_{Id}/I_D^2
Spice NLEV=0 $S_{I_d} = \frac{K_F I_D^{AF}}{C'_{OX}.L^2}.\frac{1}{f}$	✗	Only if AF =1 →	✗ Tends to ∞ in W.I.
Spice NLEV=1: $S_{I_d} = \frac{K_F I_D^{AF}}{C'_{OX}.W.L}.\frac{1}{f}$	✓	Only if AF =2 →	✗ Remains constant in the whole operating range.
Spice NLEV=2,3: $S_{I_d} = \frac{K_F g_m^2}{C'_{OX}.W.L}.\frac{1}{f^{EF}}$	✗ .	✓	✓ $\propto \frac{g_m^2}{I_D^2}$
BSIM 3v3 See ref .[52,80] for description.	✓ (see note (*))	✓	✓

Table 3.1: Typical flicker noise models implemented in SPICE.
✓: model is consistent with experimental results
X: model fails to predict
(*)According to the manual [52], BSIM3v3 uses a different model for strong and weak inversion.

3.2 A SELF-CONSISTENT, PHYSICS-BASED MODEL FOR FLICKER NOISE IN MOS TRANSISTORS.

Flicker noise or simply 1/f noise is such that its power spectral density varies with frequency in the form [77-87]:

$$S(f) = \frac{K}{f^{\gamma}} \tag{3.9}$$

with K, γ constants, $\gamma \approx 1$ [2]. It also receives the name "pink" noise as opposed to "white" noise because light with a spectral density of the same form would appear as a weak pink color to the human eye. 1/f noise is present in most natural phenomena. Wentai Li [92] reports an extensive bibliography grouped into several categories, ranging from 1/f noise in electronics, biology and chemical systems to 1/f noise in music and highway traffic. However, it is in electronic devices that 1/f noise has received most attention and particularly in MOS transistors because it becomes an important limitation in circuit design, especially for instrumentation.

As previously mentioned, there is still controversy regarding the origin of flicker noise in MOS transistors, and a general, consistent, single-piece flicker noise model has not yet been

[2] For a complete discussion on γ see annex B.

developed. In this section, a one-equation –all-regions model for the flicker noise in long channel MOS transistors is developed. To calculate the total current noise in a MOS transistor, the noise current caused by trapping-detrapping of carriers in each channel element must be integrated. To perform this integration, the MOSFET model from section 2.1 is employed.

3.2.1 - The behavior of common flicker noise models.

Experimental results show that the normalized PSD of flicker noise current S_{I_d}/I_D^2 presents a plateau in weak inversion and decreases in strong inversion [79,93]. Moderate and weak inversion are very important for modern low-voltage low-power design, however, some of the available models of flicker noise do not give correct results in weak or moderate inversion. In Table 1, column 4, the behavior of the ratio S_{I_d}/I_D^2 for common models of flicker noise [90,91] is shown. Spice models NLEV=0, 1 predict wrong dependencies of the noise performance in terms of the bias point. In model NLEV=0, S_{I_d}/I_D^2 tends toward infinity in weak inversion. Spice NLEV=1 gives a constant S_{I_d}/I_D^2 for all the operating regions. On the other hand, Spice NLEV=2, 3 approximately represent the behavior of the ratio S_{I_d}/I_D^2, since this ratio is proportional to g_m^2/I_D^2. The BSIM3v3 noise model shows the correct behavior for the S_{I_d}/I_D^2 ratio from weak to strong inversion and is consistent for series and parallel associations. However, the BSIM3v3 noise model interpolates flicker noise in moderate inversion [52,80] and it has the drawback of having three fitting parameters.

3.2.2 - A new physics-based model for flicker noise in MOS transistor.

To integrate the elementary noise contributions along the channel we split the transistor into three series elements: the upper transistor, the lower transistor, and a small channel element of length Δx and area $\Delta A = W.\Delta x$ as in Fig.3.5(a). Small signal analysis can be carried out, considering the general expression for the source (drain) transconductance $g_{ms(d)}$ of (3.3). We define the resistance ΔR of a small element of the channel of length Δx with the aid of (2.4):

$$\Delta R = \Delta V_x / I_D = -\Delta x/\left(\mu W Q_I'\right) = -\Delta x/\left(\mu W q\, N'\right) \tag{3.10}$$

Representing the channel element by a resistance, and considering the transconductances proportional to the inversion charge densities, are both consequences of the quasi-Fermi potential formulation for the drain current. Calling the noise current produced by the channel element $i_{\Delta A}$ (Fig.3.5(c)), small signal analysis allows one to calculate the resulting effect of $i_{\Delta A}$ on the drain current noise. As shown in Fig.3.5 (c), current division between the channel element and the equivalent small signal resistance of the rest of the channel gives $\Delta I_d = (\Delta x/L).i_{\Delta A}$. Thus, the total squared drain current fluctuation is summed for all channel elements:

$$(\Delta I_D)^2 = \sum_L (\Delta I_d)^2 = \lim_{\Delta x \to 0} \sum \left[(\Delta x/L) i_{\Delta A}\right]^2 = \frac{1}{L^2} \int_0^L \left[\Delta x (i_{\Delta A})^2\right] dx \tag{3.11}$$

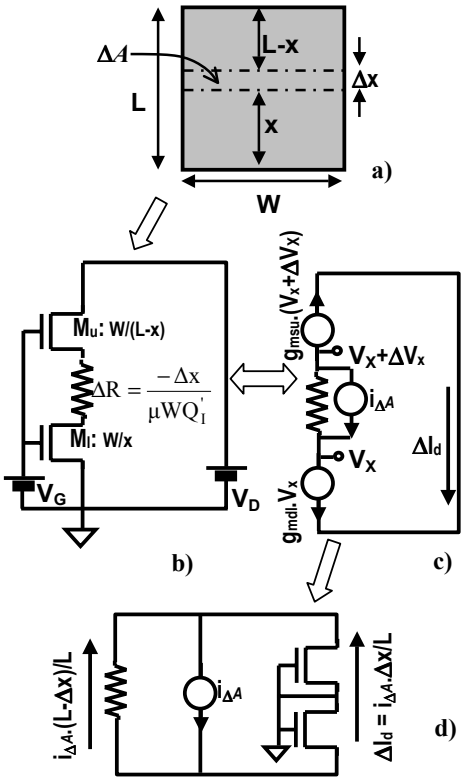

Fig.3.5: a) A MOS transistor channel and a element $\Delta A = W.\Delta x$ in it. b) The transistor is separated into 3 series components c) Small signal analysis to calculate the noise contribution to the drain current of the noisy element ΔA.

Note that since $i_{\Delta A}$ is related to the average of the local fluctuations of the carrier density N' in the channel in the area ΔA, its PSD must be proportional to $1/\Delta A = 1/(W.\Delta x)$. Equation (3.11) is widely general and could be employed with any model for the noise $i_{\Delta A}$ of a single channel element such as the thermal noise model, Hooge's model [95], or the carrier number fluctuation model usually employed for the deduction of physical based flicker noise models [80,83]. We will employ the latter so we must relate the carrier number fluctuation to the noise current $i_{\Delta A}$. To start with, it is possible to derive, using classical physical hypotheses, the PSD of N'_A, the number of occupied traps in the oxide above the channel element ΔA. From annex B, (B.26): $S_{N'_A} = \frac{1}{\Delta A} N_t k_B T \lambda . \frac{1}{f} = \frac{N_{ot}}{\Delta A} . \frac{1}{f}$. N_{ot} [1/m^2] is the effective number of traps [82], a technology parameter to be adjusted and λ is the tunneling constant, both defined in annex B. The PSD $S_{N'_A}$ has the particular 1/f shape. Variations in N'_A are related to variations in N' through the r coefficient that was calculated with a simple charge balance in 1983 by Reimbold [79]:

$$r = \left| \frac{\delta N'}{\delta N'_A} \right| = \frac{-Q'_I/\phi_t}{C'_b + C'_{ox} - Q'_I/\phi_t} \cong \frac{-Q'_I}{nC'_{ox}\phi_t - Q'_I} \tag{3.12}$$

The last approximation in (3.12) takes advantage of the fundamental approximation for the depletion capacitance per unit area C_b' of the ACM model in eq.(2.1). Finally, variations in N' are related to variations in current by a simple first order expansion of (3.10) similar to the derivation in [79,80]:

$$i_{\Delta A} = I_D \frac{\delta N'}{N'} \tag{3.13}$$

where $\delta N'$ is the fluctuation of the number of carriers per unit area N', in the channel element of area ΔA. For the sake of simplicity we will consider only fluctuation in the number of carriers, but the analysis could be extended to include fluctuation in the mobility [80].

It follows from equations (B.26), (3.12), that the PSD of the time-fluctuations $\delta N'$ of the carrier density in the channel area ΔA can be written as:

$$S_{N'}(f) = \frac{N_{ot}.\left(Q_I'\right)^2}{\Delta A.\left(Q_I' - nC_{ox}'\phi_t\right)^2} \cdot \frac{1}{f} \tag{3.14}$$

We obtain an expression of the PSD of the drain current using (3.14) and (3.13) to calculate $S_{i_{\Delta A}}(x,f)$, and inserting the result into (3.11). With the aid of (2.2) the integration over the channel length in (3.15a) is changed into the integration over the channel charge density:

$$S_{I_d} = \frac{q^2 N_{ot}.{I_D}^2}{W.L^2} \cdot \frac{1}{f} . \int_0^L \frac{1}{\left(nC_{ox}'\phi_t - Q_I'\right)^2} dx \tag{3.15a}$$

$$S_{I_d} = \frac{q^2 N_{ot}\mu I_D}{nC_{ox}'L^2} \cdot \frac{1}{f} \int_{Q_{IS}'}^{Q_{ID}'} \frac{1}{nC_{ox}'\phi_t - Q_I'} dQ_I' \,. \tag{3.15b}$$

It follows:

$$\frac{S_{I_d}}{I_D^2} = \frac{q^2 N_{ot}\mu}{L^2 nC_{ox}' I_D} . \ln\left[\frac{nC_{ox}'\phi_t - Q_{IS}'}{nC_{ox}'\phi_t - Q_{ID}'}\right] . \frac{1}{f} \tag{3.16}$$

An expression similar to (3.16) is used in BSIM [52,80] to model strong inversion noise due to charge trapping, but it must be emphasized that (3.16) is valid for any inversion level, including moderate inversion.

- In weak inversion, $Q_{IS}', Q_{ID}' << nC_{OX}'\phi_t$. Making a first order series expansion, it is possible to rewrite (3.16) in a more concise manner :

$$\frac{S_{I_d}}{I_D^2} = \frac{N_{ot}}{WLN^{*2}} . \frac{1}{f} \tag{3.17}$$

where $N^* = nC_{OX}'\phi_t / q$ [80]. (3.17) is the same expression used in BSIM3 and 4 to model flicker noise in weak inversion ($N_{ot} = A.k_B T/\gamma$ in [80]) and, it is also equivalent to the formula proposed by Reimbold in [79].

- In strong inversion and in the linear region, $Q'_{IS} \cong Q'_{ID} \cong -C'_{ox}(V_{GS} - V_T)$, and the first order expansion of (3.16) leads to:

$$\frac{S_{I_d}}{I_D^2} = \frac{q^2 N_{ot}}{WLC'^2_{OX}(V_{GS} - V_T)^2} \cdot \frac{1}{f} \tag{3.18}$$

Also in this case, the result is the same as that obtained in [79].

Summarizing the bias dependence of the drain current PSD, in subthreshold, S_{I_d} increases with I_D^2 following (3.17) while in saturation in strong inversion S_{I_d} increases with I_D as predicted by (3.16) if we neglect the variation in the logarithmic term.

Finally, let us remark that the model in equation (3.16) is consistent when applied to the parallel or series association of transistors. Effectively splicing a transistor into two series elements similar to those in Fig.3.3, equation (3.4) is satisfied in all operation regions using the flicker noise model of (3.16) for the calculation of the PSDs $S_{i_{du}}, S_{i_{dl}}, S_{i_{d\_s}}$. Eq. (3.5) is also verified when splicing the transistor as in Fig.3.4.

3.2.3 - Measurement results.

Some noise measurements were performed in MOS transistors covering all regions of operation to experimentally verify the model in (3.16). Noise spectra were recorded with the aid of a Stanford Research SR560 low noise amplifier, and a Hewlett Packard HP3582A spectrum analyzer. To measure the drain current and fix the node voltages, a Hewlett Packard HP4155 Semiconductor Parameter Analyzer with the addition of RC filters for noise reduction was employed (Fig.3.6). In all cases the PSD closely follows a $1/f$ dependence. This is consistent with the assumption $\gamma = 1$ associated with a uniform spatial distribution of the traps inside the oxide [81], and also with the fitted values of γ that are presented in annex B. For the adjustment of the noise model, the measured noise spectra were acquired from 0.3 to 30Hz because in this region, the PSD is high enough to measure flicker noise particularly in weak inversion; and we also avoid the effect of the AC line and its harmonics. Once acquired, every measured spectrum $S_{I_d}(f)$ was adjusted by means of least squares to (3.9) to obtain the value of K with γ=1. Each estimated *K* value is used for a single point in Figs.3.8-3.12; so in spite of the graphs showing either S_{I_d} or S_{I_d}/I_D^2 at a frequency of 1Hz, each point in the graphs represents information obtained over the whole frequency range of measurement. In Fig.3.7 several measured frequency spectra are shown; each dashed line fits a measured spectrum, and corresponds to a single point in Fig.3.12. For the calculation of the theoretical model, the charge densities $Q'_{IS(D)}$ were estimated with the aid of a circuit simulator and the ACM model with typical parameters for the MOS transistor. The parameter N_{ot} of the model in (3.16) is adjusted to best fit the measurements in the logarithmic domain, that is to minimize the distance of the measured points to the theoretical curve of (3.16) in the log-log plot.

Figs.3.8 and 3.9 show the simulation and measurements of flicker noise for an n-channel MOSFET of a 0.8µm CMOS process. The transistor has an aspect ratio W/L=200µm/5µm. A wide transistor was chosen in order to be able to comfortably characterize weak inversion operation. Fig. 3.8 covers all the operating regions for the saturated transistor, from weak to strong inversion; note here the plateau of the normalized PSD S_{I_d}/I_D^2 in weak inversion.

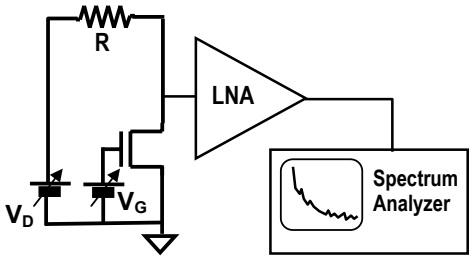

Figure 3.6: Simplified experimental setup for flicker noise measurements.

Fig. 3.9 was obtained for the same transistor operating in strong inversion and in the linear region. In Fig.3.10, the predicted and measured flicker noise for a W/L=20µm/10µm NMOS transistor covering different V_{DS} values from linear region up to saturation with a gate voltage V_G=3.3V are shown. Both transistors were fabricated in the same technology but in different runs which may explain the different N_{ot} values.

In Fig. 3.11 the flicker noise is shown for a saturated p-channel transistor of the same technology and with the same aspect ratio. As shown in Fig.3.8, it is still possible to observe the plateau in weak inversion.

Finally, in Fig. 3.12 measurements and simulations of flicker noise for a L_{min}=2.4µm technology are also presented. In this case the measurements were performed for two NMOS transistors of different sizes. Once again the measurements show a good agreement with the model and the extracted N_{ot} value is similar to the values determined for the 0.8µm process.

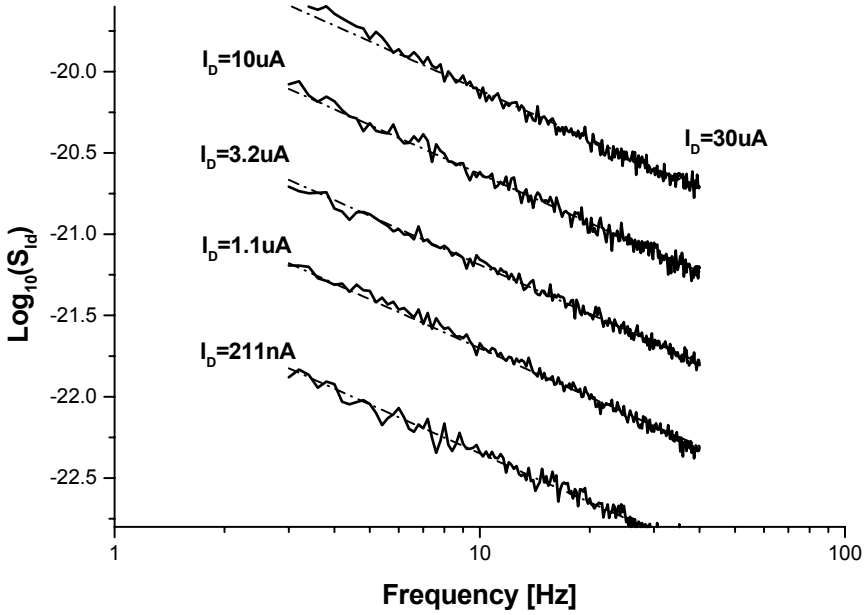

Figure 3.7: Measured flicker noise spectrums for a saturated NMOS transistor fabricated in a 2.4µ process.W/L=40µm/12µm.

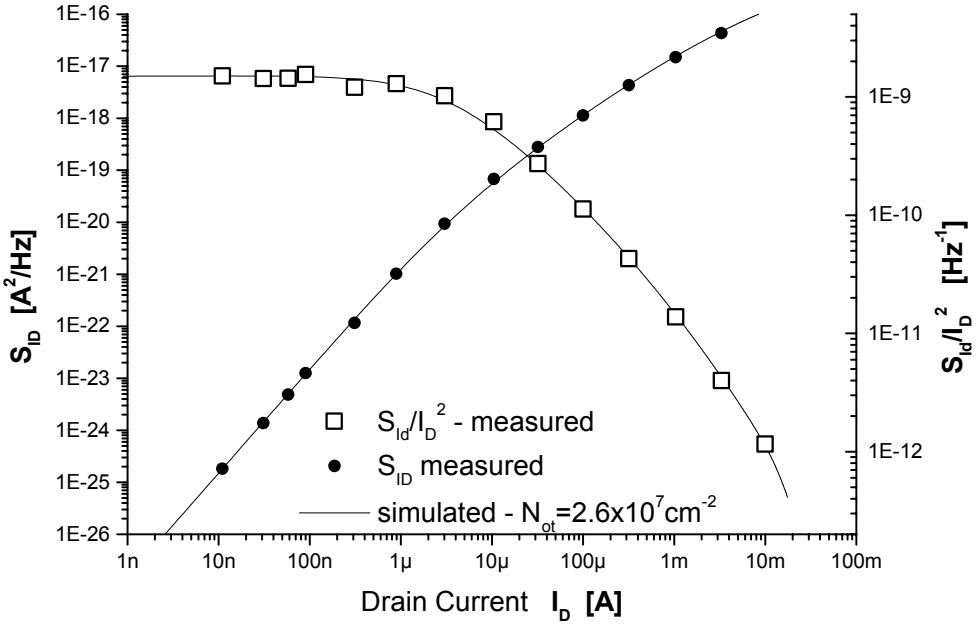

Figure 3.8: Flicker noise PSD, and normalized P.S.D. S_{I_d} / I_D^2 , at f=1Hz for a saturated NMOS transistor (W/L=200µm/5µm).

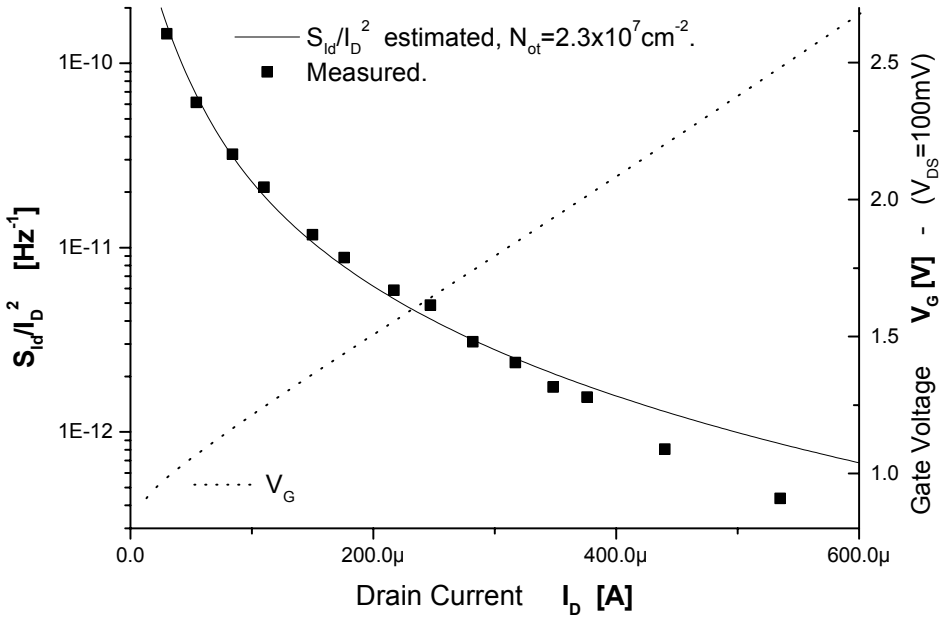

Figure 3.9: Normalized PSD. S_{I_d} / I_D^2 at f=1Hz for a NMOS transistor (W/L=200µm/5µm) in the linear region. Gate voltage V_G ranging up to 3V with Drain-to-Source voltage V_{DS} fixed at 100mV.

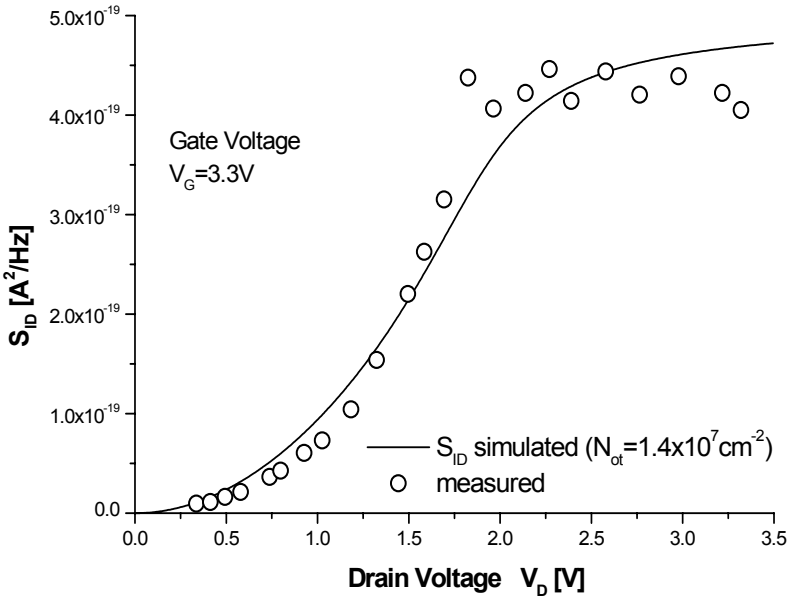

Figure 3.10: Flicker noise PSD at f=1Hz, for a W/L=20µm/10µm NMOS transistor, from linear region up to saturation.

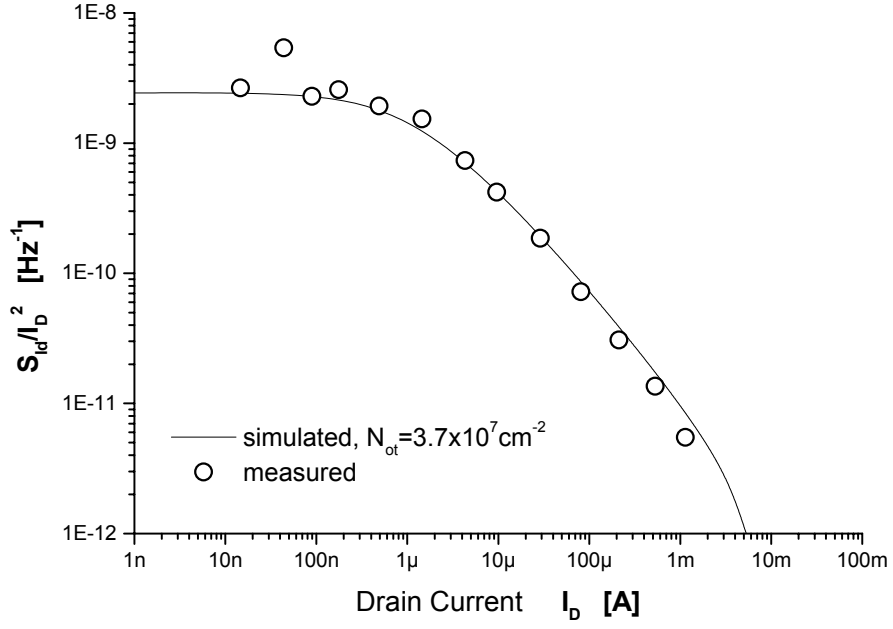

Figure 3.11: Normalized PSD. S_{I_d} / I_D^2 at f=1Hz for a saturated PMOS transistor (W/L=200µm/5µm).

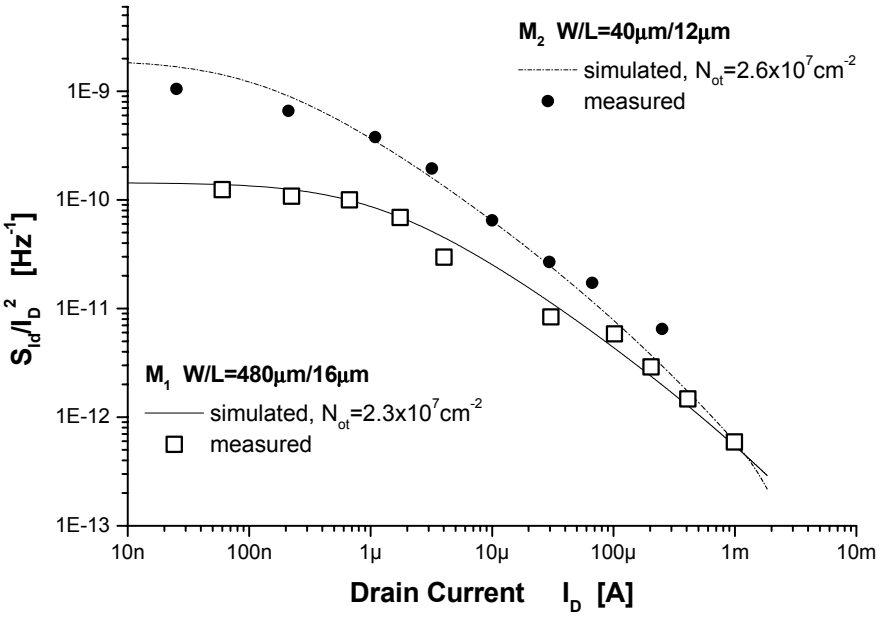

Figure 3.12: Normalized P.S.D. S_{I_d} / I_D^2 at f=1Hz for two saturated NMOS transistors fabricated in a 2.4µm process.

3.3 FLICKER NOISE MODEL IN TERMS OF INVERSION LEVELS.

A useful alternative expression for (3.16) is obtained if the charge densities at source (drain) are expressed in terms of the normalized forward and reverse currents i_f, i_r. Using the relationship between normalized charges and currents from (2.7) expression (3.16) can be rewritten as :

$$\frac{S_{I_d}}{I_D^2} = \frac{N_{ot}}{WLN^{*2}} \cdot \frac{1}{f} \cdot \frac{1}{(i_f - i_r)} \ln\left[\frac{1+i_f}{1+i_r}\right] \tag{3.19}$$

From weak to strong inversion in the linear region, $i_f \approx i_r$ and (3.19) reduces to

$$\frac{S_{I_d}}{I_D^2} = \frac{N_{ot}}{WLN^{*2}} \cdot \frac{1}{f} \frac{1}{1+i_f} \tag{3.20}$$

That is equivalent to (3.18). In weak inversion, $i_r << 1$, and the first order series expansion of (3.19) leads to (3.17).

Designers sometimes prefer the input referred noise $S_{Vgate}=S_{Id}/g_m^2$. Writing the current to transconductance ratio in terms of the inversion level for a transistor operating in saturation it follows from (3.19) that

$$S_{Vgate} = \frac{q^2 N_{ot}}{WL C'^2_{ox}} \cdot \frac{1}{f} . \psi(i_f) \tag{3.21}$$

where

$$\psi(i_f) = \left(\frac{1+\sqrt{1+i_f}}{2} \right)^2 \frac{ln(1+i_f)}{i_f} \tag{3.22}$$

Because $\psi(i_f)$ shows very small variations with i_f as depicted in Fig.3.13, one of the so-called empirical models [50] follows if we considered this function equal to 1, or, equivalently

$$S_{Vgate} \cong \frac{q^2 N_{ot}}{WL C'^2_{ox}} \cdot \frac{1}{f} \tag{3.23}$$

Due to its simplicity, the empirical model (3.23) is very convenient for hand calculations. It can be used with SPICE defining K_F as $K_F = q^2 N_{ot} / C'_{ox}$ in SPICE NLEV 2, 3 (Table 3.1). Even though the empirical model gives a good estimation of the flicker noise of a transistor in saturation it is not consistent with expression (3.4). In effect, the empirical model does not consider the distributed nature of the MOSFET, because it represents noise as a gate voltage source independent of the bias condition ($\psi(i_f)$=1).

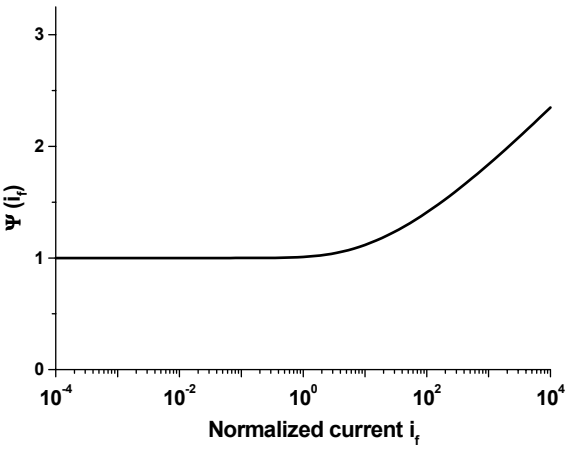

Figure 3.13: Function $\psi(i_f)$.

3.4 THERMAL NOISE AND CORNER FREQUENCY.

To complete a set of simple low noise equations for design purposes, it is still necessary to examine thermal noise.

3.4.1 - Thermal noise.

From the classical model for thermal channel noise (3.6) and the expression of the total inversion charge in terms of the channel charge densities at the ends of the channel [50,96] it follows that

$$S_{iw} = -4k_B T\mu \frac{W}{L} \frac{\frac{2}{3}\left(Q'^2_{IS} + Q'_{IS}Q'_{ID} + Q'^2_{ID}\right) - n C'_{ox}\phi_t \left(Q'_{IS} + Q'_{ID}\right)}{Q'_{IS} + Q'_{ID} - 2n C'_{ox}\phi_t} \tag{3.24}$$

The expression above is valid in all the operating regions, from weak to strong inversion and from the linear to the saturation region, but is rather cumbersome. Useful design expressions in different operating regions in terms of the transistor transconductances are easily deduced. In the linear region, from weak to strong, inversion $Q'_{IS} \cong Q'_{ID}$, and

$$S_{iw} \cong -4 k_B T \mu \frac{W}{L} Q'_{IS} = 4 k_B T g_{ms} \cong 4 k_B T g_{md} \tag{3.25}$$

As expected the channel behaves as a resistance of value $1/g_{ms}=1/g_{md}$. In weak inversion, $\left|Q'_{IS(D)}\right| << n C'_{ox} \phi_t$, and it is possible to rewrite (3.24) as:

$$S_{iw} \cong -4 k_B T \mu \frac{W}{L} \frac{\left(Q'_{IS} + Q'_{ID}\right)}{2} = 4 k_B T \frac{g_{ms} + g_{md}}{2} \tag{3.26}$$

For a saturated transistor in weak inversion

$$S_{iw} = 2 n k_B T g_m \tag{3.27}$$

In saturation $\left|Q'_{ID}\right| << \left|Q'_{ISD}\right|$ and strong inversion, $\left|Q'_{IS}\right| >> n C'_{ox} \phi_t$, and it is possible to rewrite (3.24) as:

$$S_{iw} = \frac{8}{3} n k_B T g_m \tag{3.28}$$

Using that $g_m = \frac{2 . I_S . i_f}{n \phi_t \left(\sqrt{1 + i_f} + 1\right)}$ allows us to write (3.27),(3.28) in terms of the transistor's inversion level. In Fig.3.14, the calculated and measured values of the normalized PSD of white noise are shown and compared to flicker noise (same transistor as in fig.3.8). These measurements were obtained at a frequency of several kHz to minimize the effect of flicker noise. In the same figure, simulations using (3.16) and SPICE NLEV 2, 3 with $K_F = q^2 N_{ot} / C'_{ox}$ are presented for flicker noise. Note the slight underestimation of flicker noise in strong inversion using the empirical model (3.23).

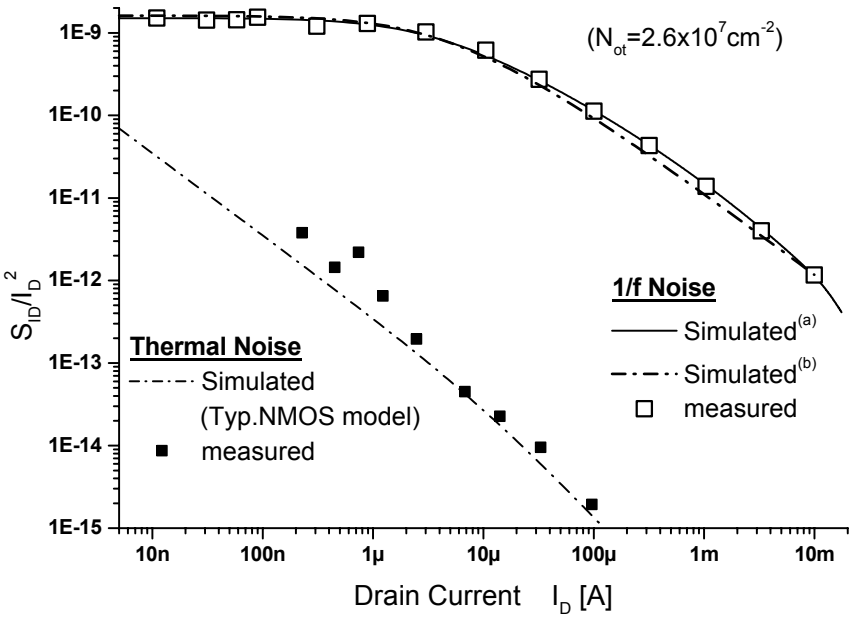

Figure 3.14: Normalized flicker and thermal PSD at f=1Hz for a saturated NMOS (W/L=200µm/5µm). Flicker noise is simulated using [a] physical model (3.16) [b] SPICE NLEV=2, 3 approximation (3.23)

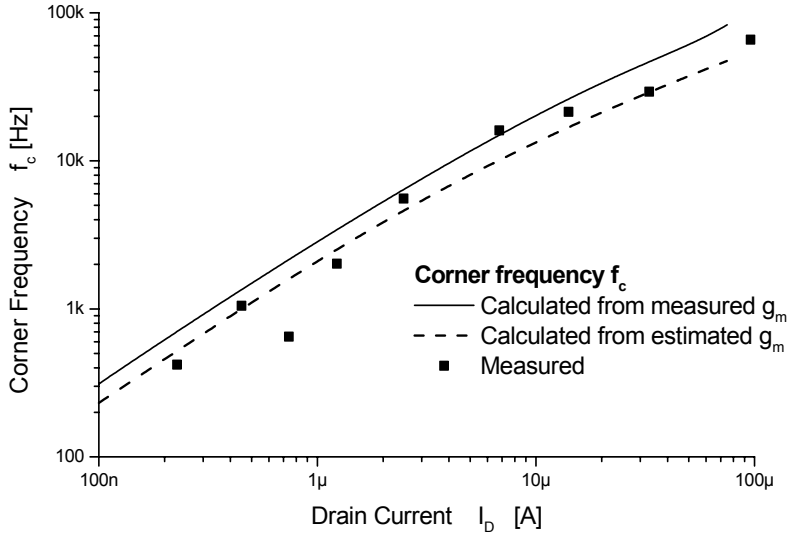

Figure 3.15: Calculated and measured values of the corner frequency f_c , for a W/L=200µm/5µm NMOS transistor.

3.4.2 - Corner Frequency.

The corner frequency f_c, defined as the frequency at which the flicker noise and thermal noise PSD have the same value, can be calculated directly in terms of Q'_{IS}, Q'_{ID} from equations (3.16) and (3.24). However, simpler results were obtained determining f_c in weak inversion with equation (3.17) and (3.27) and in strong inversion with the help of (3.18) and (3.28).

$$f_c = \frac{\alpha g_m}{WLC'_{ox}} \frac{N_{ot}}{N^*} \cong \frac{\pi}{2} \frac{N_{ot}}{N^*} \cdot f_T \tag{3.29}$$

with $\alpha = \frac{1}{2}$ in weak inversion and $\alpha \cong \frac{9}{16}$ in strong inversion. Note that the corner frequency in eq.(3.29) is proportional to the transition frequency f_T of the transistor [20,50], which results in a useful approximation for the designer.

The total noise in a frequency band (f_2-f_1) resulting from the contributions of thermal and flicker noise can be calculated as an equivalent gate rms voltage. For a saturated transistor operating in weak inversion, the integration of both (3.23) and (3.27) , yields:

$$\bar{v}^2_{gate} = \frac{2nk_BT}{g_m}\left((f_2 - f_1) + f_c \ln\left(\frac{f_2}{f_1}\right)\right) \tag{3.30}$$

For strong inversion, an analogous formula exists with slightly different coefficients. Using (3.29) in (3.30) leads to total transistor noise in the form:

$$\bar{v}^2_{gate} = \frac{A}{g_m} + \frac{B}{WL}, \quad \text{with} \quad A = 2nk_BT(f_2 - f_1) \quad B = \frac{nk_BTN_{ot}}{WLC'_{ox}N^*} \ln\left(\frac{f_2}{f_1}\right) \tag{3.31}$$

Eq.(3.30)(3.31), are a classical way to write noise dependence in transistor size and bias point, with a flicker noise term related to the area, and a thermal noise term related to transistor transconductance g_m [97-99] [3]. In Fig.3.15, the simulated and measured corner frequency of a saturated NMOS transistor for various bias currents is presented. The solid line represents f_c calculated using (3.29), together with the measured value for g_m. The dashed line represents f_c calculated using expression of g_m in terms of the inversion level. For the measured technology the dimensionless factor $\frac{\pi}{2}.\frac{N_{ot}}{N^*} \cong 0.8\text{x}10^{-3}$. Both simulations and measurements predict that the corner frequency decreases as the transistor operates deep in weak inversion. This is in accordance with the noise measurements presented in [35].

[3] If the adequate noise models are employed.

3.5 DESIGN EXAMPLE.

The low-noise, low-frequency G_m-C preamplifier of Fig.(3.16a) will be employed in an implantable sensor device where noise and power consumption are critical. The transfer function of the circuit is lowpass:

$$G(f) = \frac{G_{m1}}{G_{m2}} \left(\frac{1}{1 + j2\pi fC/G_{m2}} \right) \tag{3.32}$$

The cut-off frequency of the filter should be set at 20Hz[4]. The signal frequency range from 0.3 to 10Hz with a required input referred noise of less than $25\mu V_{rms}$. The gain G_{m1}/G_{m2}=40. Linearity of G_{m1} is not a major issue due to a low input voltage swing, but the linear range of G_{m2} should be at least 100mV. To achieve the required performance, series-parallel division of currents [18,19][5] has been employed for G_{m2} (Fig.6(c)), while G_{m1} is a standard symmetrical OTA (Fig.3.16(b)). The PSD of the total noise voltage S_{Vin} at the input of the circuit is calculated summing the contribution of both OTAs:

$$S_{Vin} = S_{VG_{m1}} + S_{VG_{m2}} \left(\frac{G_{m2}}{G_{m1}} \right)^2 \tag{3.33}$$

$S_{VG_{m1}}, S_{VG_{m2}}$ are the PSDs of the input referred noise voltage of G_{m1}, G_{m2}, respectively. So unless G_{m2} is excessively noisy, the total noise is mainly determined by the input OTA (because $(G_{m1}/G_{m2})^2 >> 1$). Thus, design starts with an exploration in Fig.3.17, of the design space for G_{m1}. Because of the low frequencies involved and the low power specification, all transistors in G_{m1} are assumed to operate in weak inversion. Each transistor in the symmetrical OTA introduces approximately the same amount of noise if they have the same area, assuming the same number of effective traps for n-MOS and p-MOS transistors. Consequently, the input referred noise for G_{m1}, plotted in Fig.3.17, is simply 8 times the rms voltage given by eq.(3.31). For the specific area budget, the chosen solution was a $1000\mu m^2$ gate area for each transistor. A transconductance G_{m1}=100nS was chosen according to (3.29) to set the corner frequency $f_c \approx 10$Hz , just above the signal band. The reason for this criterion is that at the selected point (indicated by the vertical dashed line in Fig.3.17) flicker noise dominates, and it is only possible to reduce total input noise by increasing the gate area but not the transconductance G_{m1}. It is a near optimal solution in the sense of minimum total input noise for a given transistor gate area, with a minimum G_{m1} (and thus minimum power consumption). The input transistors were finally sized W/L=120μm/10μm (a bit higher gate area than the selected operating point), biased with 3.5nA each (I_{Bias}=7nA), and the simulated transconductance G_{m1} was 110nS.

The G_{m2} OTA topology is shown in Fig.3.16(c), with series-parallel division of current to achieve a transconductance of 2.35nS. The desired linear range[6] determines the inversion

[4] Note that this specification slightly differ from those for the accelerometer's signal conditioning circuit of chapter 1.
[5] For a deep analysis concerning G_{m2} circuit refer to chapter 4, this example is focused on G_{m1}.
[6] From eq.(2.25).

level of the input pair and the division factor results from $G_{m2} = g_{m1}/(N_1.N_2)$, where g_{m1} is the gate transconductance of the input pair. In this design the current division factor is 72 ($N_1 = 9$, $N_2 = 8$). The series-parallel current division OTA configuration will be presented in detail in chapter 4, as well as a detailed noise calculation based on the previously presented equations. It will be demonstrated that both flicker and thermal noise in a series-parallel division OTA can be approximated to the expressions in (3.31) with the addition of an excess noise correction factor. Among others, noise estimation will be presented specifically for G_{m2}, demonstrating that noise in (3.33) is essentially the noise of the transonductor G_{m1}. The corner frequency for G_{m2} was estimated at 0.5Hz.

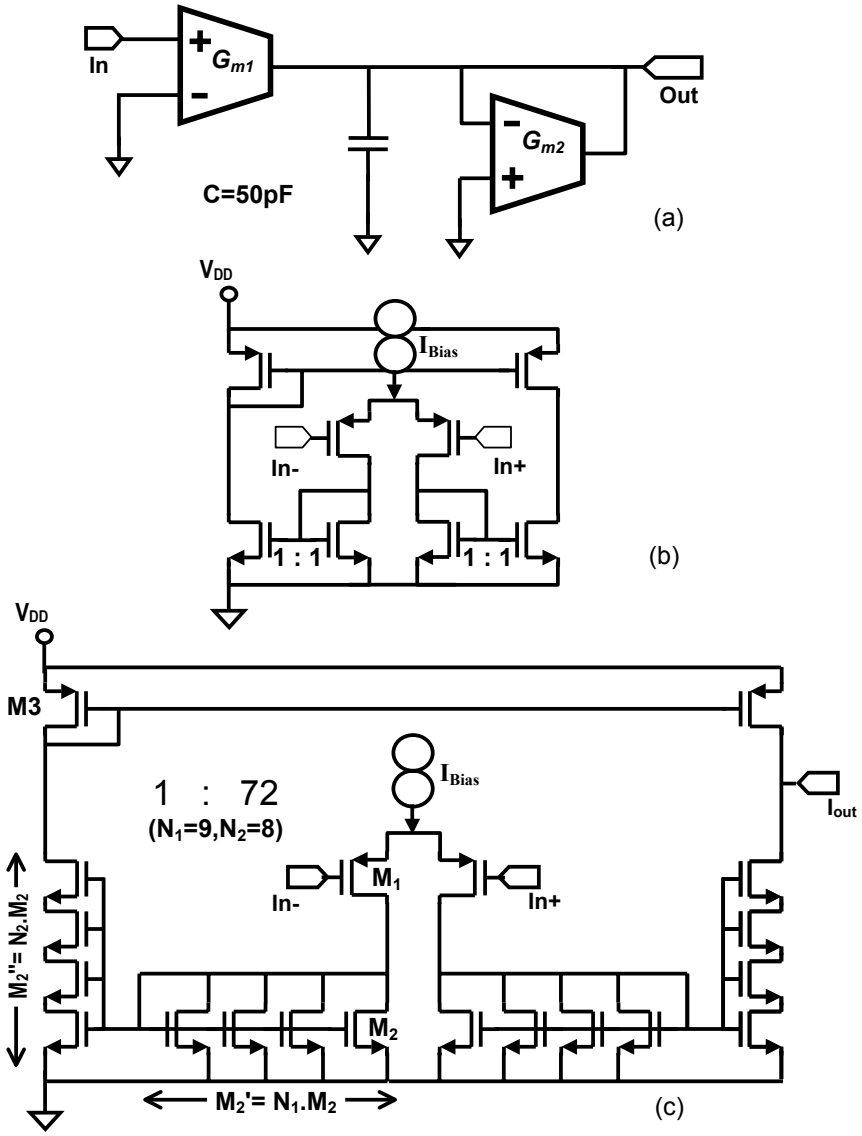

Figure 3.16: (a) Topology for the target low-noise amplifier. (b) G_{m1} OTA. (c) G_{m2} OTA with series-parallel current division.

The preamplifier and stand-alone OTAs were fabricated in a 0.8μm standard CMOS technology. In Fig.3.18 the measured voltage transfer function of the amplifier, as well as the measured and predicted input noise for G_{m1} are shown. Fig.3.19 shows the transfer function -output current against input voltage- of G_{m1}. Note that the measured transconductance is in accordance with the expected value. The total measured noise input voltage in the band of interest (from 0.3 to 10Hz assuming 20db/dec bandpass filter) were $5\mu V_{rms}$ for G_{m1}, $30\mu V_{rms}$ for G_{m2}, and $5\mu V_{rms}$ for the amplifier, while the estimated values were $6\mu V_{rms}$, $49\mu V_{rms}$, and $6\mu V_{rms}$ respectively. The measured corner frequency for G_{m1} was 8Hz. The circuit occupies a total area of $0.1mm^2$, and operates down to a 2V supply voltage with a current consumption of 14nA for G_{m1} and 43nA for G_{m2}.

3.6 CONCLUSIONS.

The consistency of noise models regarding series-parallel association of transistors has been analyzed, and the flaws in some simple flicker noise models have been stated.

A flicker noise model for long channel CMOS transistors, continuous in all the operating regions from weak to strong inversion has been developed. The new model is based on common physics hypotheses but we used a procedure to integrate the contribution to the transistor noise current of all the noisy elements in the channel that inherently preserves the series association properties of the model. With the aid of an advanced compact transistor model, this integration procedure results in a simple, single-piece, and consistent model for flicker noise in MOS transistors. The new model has also been formulated in terms of the inversion level to fulfil the designer's requirement for simplicity, and it has been demonstrated that it can be approximated to the empirical model without an excessive penalty in accuracy.

Several measurements confirm that the presented model accurately represents the behavior of flicker noise under various bias conditions. Particularly it has been observed that the normalized PSD remains approximately constant in weak inversion and decreases with the predicted slope as the transistor enters the strong inversion region, for both saturated PMOS and NMOS devices. Although a compact model could hardly fit every transistor situation, we expect this work could help predict accurately and in a simple manner, the behavior of flicker noise from weak to strong inversion of non-minimum size transistors commonly found in analog design.

To formulate a complete set of simple design equations, thermal noise was also formulated in terms of the inversion levels, and classical thermal noise approximations were derived. Design oriented expressions for the different operation regions have been given, and the proportionality between corner frequency and transition frequency has been derived and experimentally verified. As the final example shows, the expressions presented can provide a powerful tool for both hand calculations and computer-assisted analysis and design of MOSFET integrated circuits.

3.6.1 Corollary: The equivalence between mismatch offset and flicker noise.

The integration procedure in section 3.2.2 is widely general, and can be employed to examine the effect of any kind of fluctuations in the channel. The application of this procedure to study variations in the number of impurities, that locally affects threshold

voltage along the channel, allows us to derive a physical and consistent model for random mismatch in MOSFETs. Note that this case refers to space-fluctuations along the channel, rather than time-fluctuations as in flicker noise. The resulting expression for mismatch offset is:

$$\frac{\sigma^2_{I_D}}{I^2_D} = \frac{q^2 N_{oi}\mu}{L^2 n C'_{ox} I_D} ln\left(\frac{nC'_{ox}\varphi_t - Q'_{IS}}{nC'_{ox}\varphi_t - Q'_{ID}}\right) \tag{3.34}$$

where N_{oi} is the average number of impurities per unit volume in the depletion region. A detailed description of the model and calculations are presented in annex C. Eq.(3.34) substitutes the simpler form of (2.18) but it is necessary to remark that all the considerations regarding to flicker noise in terms of the inversion level are valid for mismatch. Particularly (2.18) is a good estimation of (3.34) in the same form as the empirical noise model in (3.23) is a good approximation of the physics-based model in (3.16). Moreover, mismatch can be seen as a DC - extension of flicker noise because both (3.34) and (3.16) are formally equivalent. At transistor level, a design for minimum offset is a design for minimum flicker noise, and vice-versa.

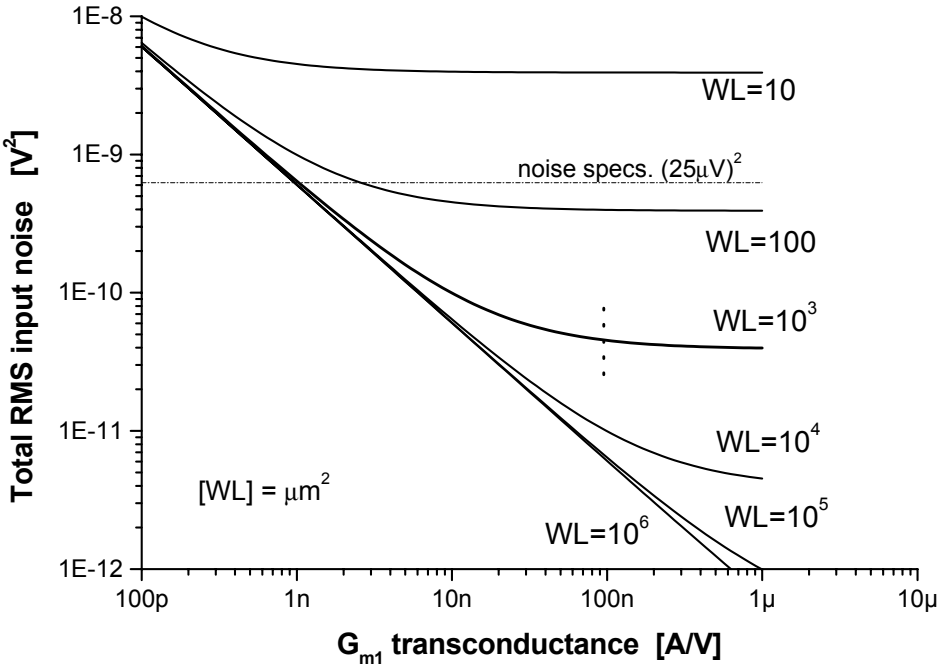

Figure 3.17: Simplified design space for G_{m1}: total input referred noise in the band of interest in terms of the gate area of the input pair, and G_{m1} transconductance. The horizontal dashed line indicates the maximum acceptable noise floor while the vertical line indicates the approximate selected solution.

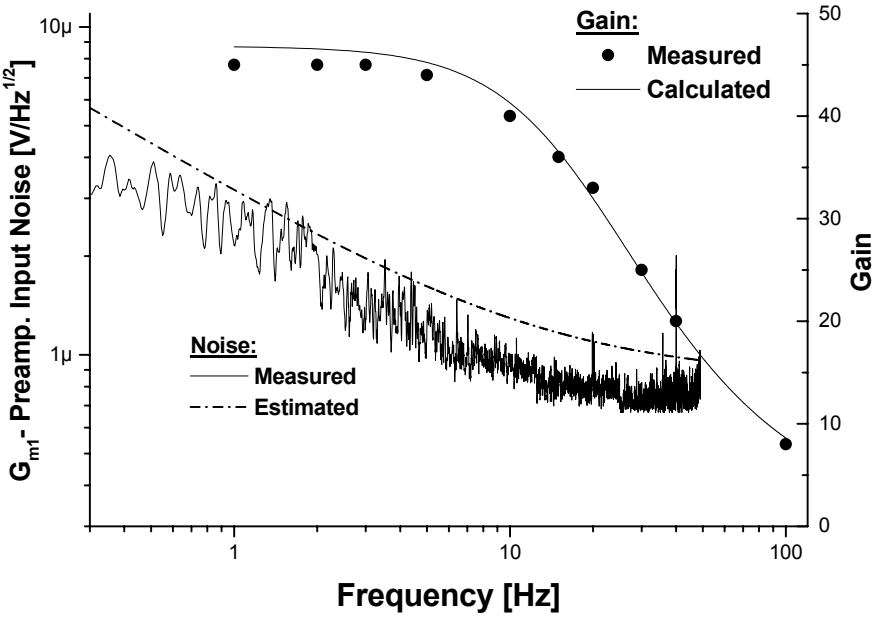

Figure 3.18: Estimated and measured noise for G_{m1}, and estimated and measured gain for the preamplifier.

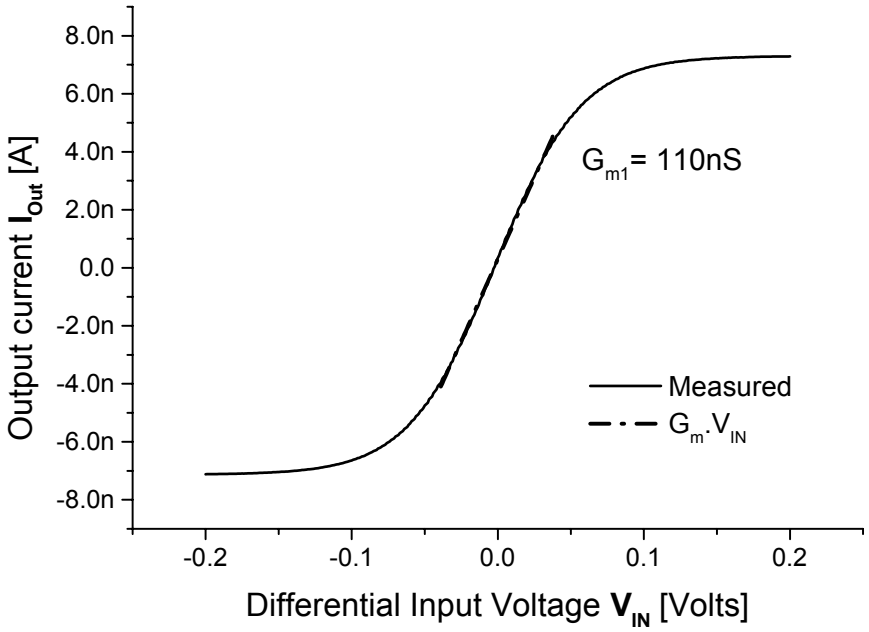

Figure 3.19: Measured transference for G_{m1}, note the reduced linear range.

Chapter 4:

Design of OTAs with Very Small Transconductance and Extended Linear Range, Using Series-Parallel Current Division.

In recent years there has been considerable research effort in the development of integrated transconductance amplifiers (OTAs) with very small transconductance and improved linear range due mainly to their application in biomedical circuits and in neural networks [36]. Several OTA topologies have been developed to achieve transconductances in the order of a few nA/V with linear range in the volt order [36-40]. The use of complex OTA architectures also increases noise, mismatch offset, and transistor area, and results in design trade-offs [36]. Simple division of the output current of a differential pair by a high ratio has been widely considered an expensive technique in terms of area. However, the use of series-parallel division of current [18] in an OTA, allows the implementation of an area-efficient current divider. The technique of using series-parallel association of transistors in current mirrors with extremely large copy factors will be employed in this chapter, to design OTAs with very low transconductance, and an extended linear range. The design and test of OTAs up to 33pS, equivalent to 30GΩ resistors, and up to ±500mV linear range, is shown. Series-parallel OTAs have shown to be an excellent trade-off solution in terms of area, power-consumption, linearity, noise, and particularly offset, for the design of G_m-C filters with extremely large time constants. Although there are reported designs using this technique [18], it has not been widely employed probably because the designer has a lack of adequate transistor-DC, noise, and mismatch, models accurately representing series-parallel association of transistors.

It is a well-known fact in analog design that circuit techniques are sometimes re-discovered, proving to be relevant for modern circuits; in this chapter a series-parallel current division/multiplication technique will be reviewed. The previously presented background of thermal and flicker noise, and offset, will be used to demonstrate that the technique is reliable; that the stack of a large number of transistors either series or parallel associated, does not increase significantly the noise nor mismatch of a circuit. Moreover, the use of a large number of unitary transistors to build two matched composed ones allows the compliance to most usual matching layout rules regarding transistor boundaries, orientation, etc, even if the two composed transistors have a very different geometry. Thus a reduced offset can be expected even while matching transistors with very different aspect ratios.

The reliable handling of series-parallel current mirrors would be valuable in any analog circuit that requires the copy of currents in a wide range. The current division technique can be applied not only to OTAs, but also in example to the derivation of several bias currents

from a single external (internal) current reference. We hope that this work will provide the designer with accurate and useful tools for handling such kinds of circuits.

The chapter begins with a brief revision of series-parallel association properties of MOS transistors. Current mirrors utilizing series-parallel association of transistors are then examined particularly regarding mismatch. Precise expressions for mismatch offset, and noise will be derived. Some examples demonstrating the reduction of mismatch offset due to the employment of series-parallel association of transistors are presented.

Then series-parallel current dividers are employed in the design of very small transconductance OTA's, and the question of what is the minimum possible transconductance using this technique is answered. A design methodology for this family of circuits is presented. Expressions for total noise, input offset and dynamic range, are discussed. Finally several designed, fabricated, and tested OTA´s are presented. These OTAs range from 33pS to 28nS, with linear range from ±150 to ±500mV, and will be employed later in chapter 5 to implement the accelerometer bandpass amplifier described in chapter 1.

4.1 SERIES-PARALLEL ASOCIATION OF MOS TRANSISTORS.

Series-parallel association of transistors can help in obtaining different transistor geometries by combining a large number of unitary transistors. For the simple example of the composite transistor in Fig.4.1, where two rectangular transistors M_S, M_D, are series connected, its equivalent transistor is well defined [58,89]. The equivalent aspect ratio of the composite transistor $(W/L)_{eq}$ is [89]:

$$\left(\frac{W}{L}\right)_{eq} = \frac{(W/L)_S.(W/L)_D}{(W/L)_S + (W/L)_D} \tag{4.1}$$

It should be stated what this equivalence means; in the triode region the composite transistor has a DC behavior equal to that of a single transistor whose aspect ratio is defined by (4.1). Also the saturation current is approximately the same for both the composite and equivalent transistor at the same gate voltage overdrive V_{GS}, but the output conductance may be different from one transistor to another. The output conductance g_{ds} (formerly named g_{md}) is associated to the channel width at the drain end [89][1]. Series-parallel association as well as eq.(4.1) may be extended to a large number of transistors. For example in Fig.4.2, four different arrays of unitary transistors sized $(W/L)_u$ are shown, all of them with the same equivalent aspect ratio $(W/L)_{eq}=4/7(W/L)_u$. Three of them show the same output conductance since their width at drain is the same. The fourth composite transistor on the left has a lower output conductance.

[1] Also in [21] it is presented a detailed analysis of the output conductance of a transistor in the perspective of the ACM model, including channel length modulation, and drain induced barrier lowering effects.

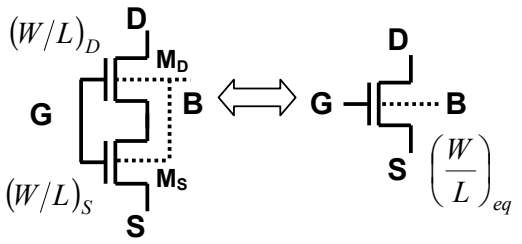

Figure 4.1: A series-composed transistor and its equivalent on the right.

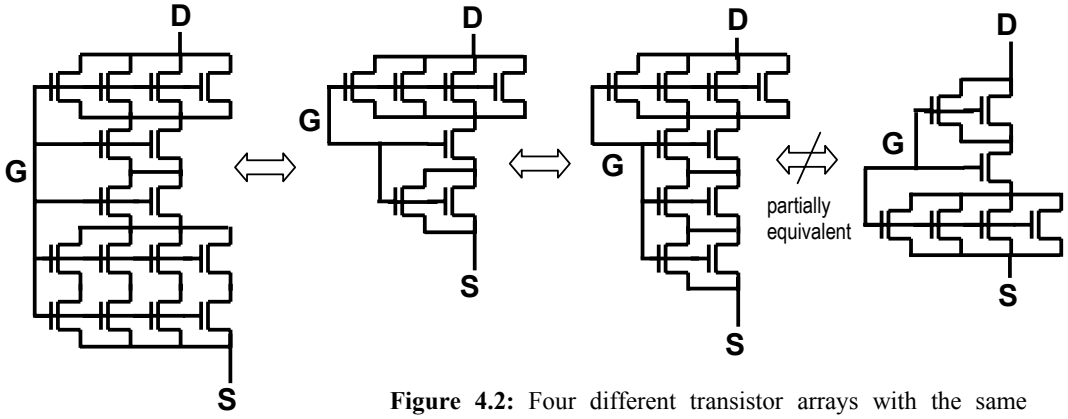

Figure 4.2: Four different transistor arrays with the same equivalent aspect ratio $(W/L)_{eq} = 4/7(W/L)_u$, (a), (b), (c) are equivalent in the sense of [89], while (d) is partially equivalent because it has a different output conductance.

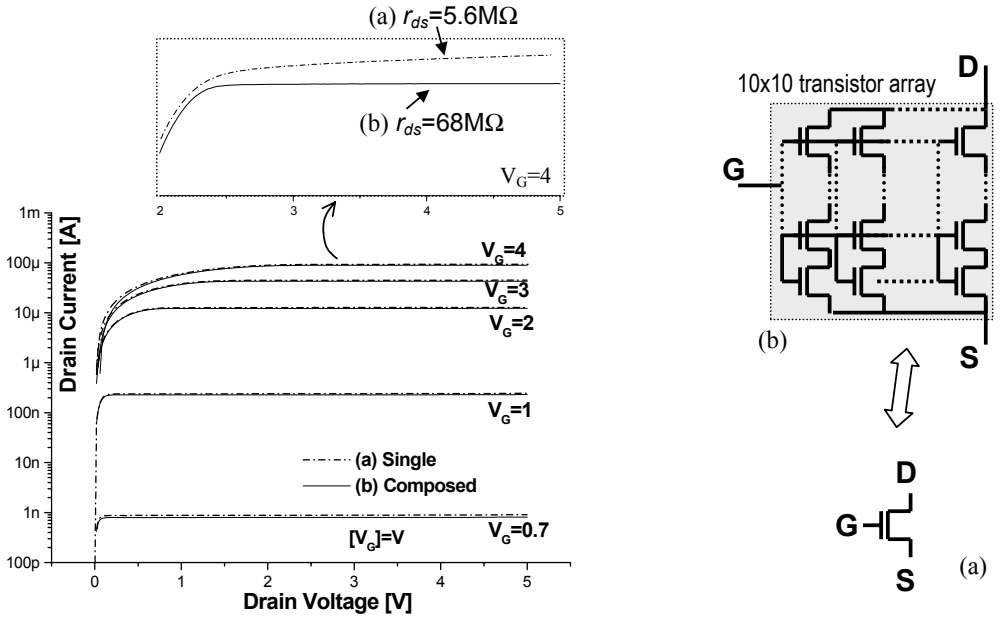

Figure 4.3: Measured I_D-V_D curves of (a) single W_u/L_u=4µm/12µm transistor. (b) 10x10 transistor array of the same unitary transistor. At the top, saturation region is magnified(linear scale) for V_G=4V to observe the change in g_{ds} from (a) to (b). As expected, the ouput resistance in (b) is near 10 times the one in (a).

In Fig.4.3, measured drain current vs. drain voltage curves for a single unitary transistor, and for a 10 by 10 array of the same transistor are shown. The dimensions of the unitary transistors are W_u/L_u=4µm/10µm, fabricated in 0.8µm CMOS technology. The two plots are similar, but note in the upper plot that the drain-source transconductance g_{ds} is much smaller in the case of the composed transistor. The output resistance $r_{ds} = 1/g_{ds}$ of the single transistor is 5.6MΩ while r_{ds} is 65MΩ for the 10x10 array. These values correspond to Early voltages of 36V/µm, and 45V/µm respectively, and are consistent with the usual assumption that the Early voltage per unit channel length is approximately constant. As a rule of thumb, the output conductance of a given composed transistor will be inversely proportional to the equivalent channel length, and to the channel width at drain end.

4.2 SERIES-PARALLEL ASSOCIATION OF TRANSISTORS FOR MISMATCH OFFSET AND FLICKER NOISE REDUCTION IN NON-UNITY CURRENT MIRRORS.

Offset due to transistor mismatch is a major limitation in analog circuit performance. Classic current mirrors (Fig.4.4(a)) with a copy factor M>>1 are very sensitive to mismatch offset because at the output, there is a single transistor M_B with a reduced area, that generates spread variations in its threshold voltage and current factor V_{Tb}, β_b. In a 2-transistor current mirror M_A,M_B - as in Fig.4.4(a) - the copy factor is calculated as the ratio between their aspect ratios:

$$\frac{(W/L)_A}{(W/L)_B} = M \tag{4.2}$$

The 10x10 composed transistor of Fig.4.3(b) - equivalent to a single one - can substitute M_B in Fig.4.4(a), to implement a current mirror with the desired copy factor M, but with the same number of unitary transistors at both input and output branches of the mirror. This circuit is shown in Fig.4.4(c). A better matching and a reduction in random offset are expected if usual layout matching rules are followed, because a large number of unitary transistors have been matched together. In this section, the series-parallel association of transistors applied to current mirrors with a non-unitary copy factor is studied from the perspective of mismatch. This technique will be demonstrated to be a valuable tool in the design of low-offset oriented analog circuits. Accurate analytical expressions to estimate current offset due to random mismatch in current mirrors using series-parallel associations of transistors will be obtained below.

In Fig.4.4, three different topologies for a current mirror to perform a M:1 current copy are shown: (a) M unitary transistors in parallel copy to a single one, (b) N-parallel transistors copy to N series-stacked transistors, (c) M unitary transistors in parallel copy to a N-series-N-parallel composed transistor. If series-parallel equivalence, and the copy factor formula in (4.2) are applied to both circuits in Fig.4(b),(c), the result is that they perform an M:1 copy. It is also expected that they present a lower current random offset in comparison to the circuit in Fig.4.4(a), because the area of the equivalent transistor M'_B (M''_B) matched to the input transistor M'_A (M''_A), is larger.

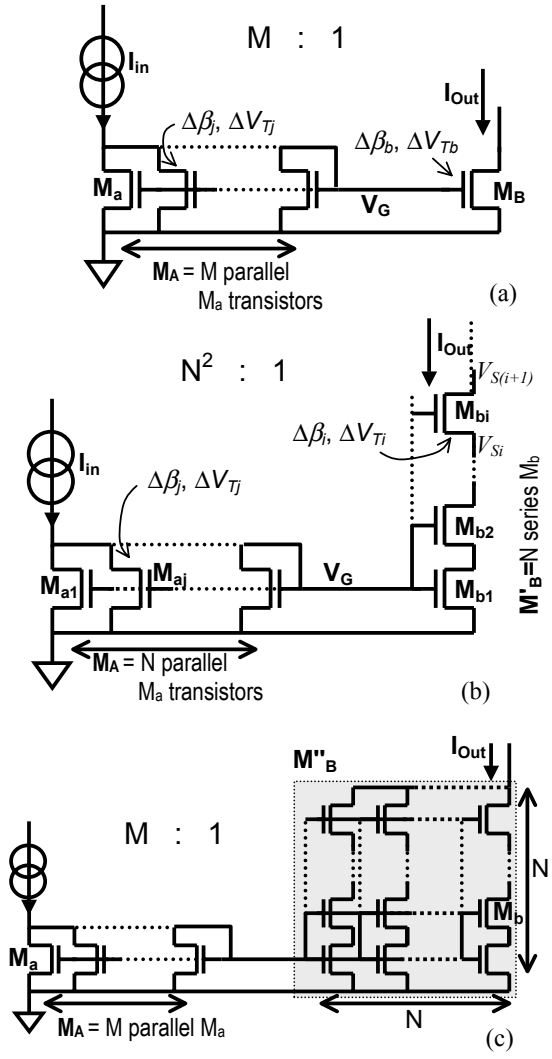

Figure 4.4: Three M:1 current copiers: (a) A M_A transistor composed by M unitary transistors M_a in parallel, copy to single transistor M_B. (b) A M'_A transistor composed by N unitary transistors M_a in parallel copy to M'_B transistor composed of N series-stacked unitary transistors M_b. (c) A M''_A transistor composed by M unitary transistors M_a in parallel, copy to M''_B transistor composed of N-series-N-parallel unitary transistors M_b. All unitary transistors $M_a \equiv M_b$ have the same $(\sigma_\beta/\beta)_u^2$, $(\sigma_{VT})_u^2$.

The normalized random current mismatch in the circuit of Fig.4(a) is calculated with small signal analysis, assuming that each unitary transistor M_a, M_B has the same standard deviation $\left(\sigma_\beta^2/\beta^2\right)_u$ in β factor and $\left(\sigma_{V_T}^2\right)_u$ in threshold voltage. All offset estimations in this chapter will be expressed in terms of $\left(\sigma_\beta^2/\beta^2\right)_u$, $\left(\sigma_{V_T}^2\right)_u$ regardless the selected mismatch model, however using the simple model for mismatch in (2.18):

$$\left(\sigma_\beta^2/\beta^2\right)_u = \frac{A_\beta^2}{2W_uL_u} \quad , \qquad \left(\sigma_{V_T}^2\right)_u = \frac{A_{V_T}^2}{2W_uL_u} \tag{4.3}$$

where W_u, L_u, are gate width, and length, of the unitary transistor, repectively. Eq.(4.3) means that unitary transistor matching is inversely proportional to gate area.

In Fig.4.4(a) the input transistor M_A produces variations in the gate voltage V_G due to variations in the threshold voltage and current factor V_{Tj}, β_j of each single M_a transistor. The resulting variations are calculated with a first order analysis analog to that of eq.(2.19):

$$\Delta V_G = \sum_{j=1}^{M}\left[\frac{I_{in}}{M.g_{mA}}.\frac{\Delta\beta_j}{\beta_j} - \frac{g_{ma}}{g_{mA}}\Delta V_{Tj}\right] \quad , \quad \frac{g_{ma}}{g_{mA}} = \frac{1}{M} \tag{4.4}$$

Variations in the output current originate not only due to variations in V_G, but also due to variations in the threshold voltage and current factor V_{T_B}, β_B, of the output transistor M_B:

$$\Delta I_{Out} = g_{mB}\Delta V_G + \frac{\partial I_{Out}}{\partial V_{T_B}}\Delta V_{T_B} + \frac{\partial I_{Out}}{\partial \beta_B}\Delta\beta_B$$

$$\Delta I_{Out} = g_{mB}\Delta V_G - g_{mB}\Delta V_{T_B} + I_{Out}\frac{\Delta\beta_B}{\beta_B} \tag{4.5}$$

In (4.4),(4.5), I_{Out} is the output current of the mirrors, and g_{mA}, g_{mB} are the gate transconductance of M_A, and M_B respectively. Because M_B, M_{aj} are all unitary transistors, $\beta_j = \beta_B = \beta$ is assumed, and (4.3) is used to compute the standard deviation of fluctuations that are assumed to be non correlated. Therefore (4.5) becomes:

$$\left(\frac{\sigma_{I_{Out}}^2}{I_{Out}^2}\right)_{(a)} = \left(1+\frac{1}{M}\right)\left[\frac{\sigma_\beta^2}{\beta^2}\right]_u + \left(1+\frac{1}{M}\right)\frac{g_{mB}^2}{I_{Out}^2}.\left[\sigma_{V_T}^2\right]_u \tag{4.6}$$

where $\left(\frac{\sigma_{I_{Out}}^2}{I_{Out}^2}\right)_{(a)}$ stands for the normalized standard deviation of fluctuations in the output current of the circuit in Fig.4.4(a). The same notation will be employed for the circuits in Fig.4(b),(c). A matching calculation for the case in Fig.4.4(b) is a bit more complex. $\Delta I_{Out(b)}$ variations in the output current are produced due to $\Delta\beta_{i(j)}$, $\Delta V_{Ti(j)}$ variations in series (parallel) transistors. Each contribution may be calculated separately by means of small signal analysis, the four $\Delta I_{Out(b)}$ terms originating from ΔV_{Ti}, ΔV_{Tj}, $\Delta\beta_i$, $\Delta\beta_j$ variations are then summed. To start, let us call ΔI_{V_TS} to the variations in the output current originating from ΔV_{Ti} variations in the series stacked transistors of the current mirror in Fig.4.4(b). For each M_{bi} transistor it is possible to write, assuming $\Delta V_{Tj} = 0$, $\Delta\beta_i = 0$, $\Delta\beta_j = 0$:

$$\Delta I_{V_T s} = \frac{\partial I_{Di}}{\partial V_{Ti}}.\Delta V_{Ti} + \frac{\partial I_{Di}}{\partial V_{Si}}.\Delta V_{Si} + \frac{\partial I_{Di}}{\partial V_{Di}}.\Delta V_{S(i-1)}$$

$$= -g_{m_i}\Delta V_{Ti} - g_{ms_i}\Delta V_{Si} + g_{md_i}\Delta V_{S(i-1)} \tag{4.7}$$

where $g_{m_i}, g_{ms_i}, g_{md_i}$ are gate, source, and drain transconductances of M_{bi}, respectively. (4.7) has been derived for a generic transistor M_{bi} but $\Delta I_{V_T s}$ is always the same since transistors are series connected. Also because transistors are series connected $Q'_{ID_i} = Q'_{IS_{(i-1)}}$, so the use of (2.13) to evaluate $g_{ms_{(i-1)}}, g_{md_i}$, allows to conclude that the two are equal. Using $g_{md_i} = g_{ms_{(i-1)}}$ and summing the equivalent of (4.7) for all the series transistors leads to:

$$N\Delta I_{V_T s} = \sum_{i=1}^{N} - g_{m_i}.\Delta V_{Ti} \tag{4.8}$$

Assuming that the ΔV_{Ti} variations are non-correlated allows us to calculate the standard deviation:

$$\sigma^2_{\Delta I_{V_T s}} = \frac{\left(\sigma^2_{V_T}\right)_u}{N^2}.\sum_{i=1}^{N} g^2_{m_i} \approx \frac{g^2_{mB'}}{N^2}\left(\sigma^2_{V_T}\right)_u \tag{4.9}$$

where $g_{mB'}$, $g_{mA'}$ are the gate transconductance of the series/parallel composed-transistor M'_B, M'_A respectively. Note that the result of the sum in (4.9) is not exact, it has been approximated assuming differential-length series transistors, and the integration procedure and approximations presented in section 3.2. Effectively, the gate transconductance of a differential length transistor at a point x in the channel, can be expressed as a function of the drain current, and channel charge density at that point, by combining (2.2),(2.13),(2.15):

$$g_{m_i}(x) = \frac{I_D C'_{ox}}{(-Q'_I + nC'_{ox}\phi_t)} \tag{4.10}$$

The discrete sum in (4.8) can then be approximated by substituting it with an integral using $N = \infty$ differential length transistors. The integration variable can be changed to charge density as in (3.15b):

$$\sum_{i=1}^{N} g^2_{m_i} \approx \int_0^L g^2_m(x).dx = \frac{\mu W I_D C'_{ox}}{nL} \int_{Q'_{IS}}^{Q'_{ID}} \frac{1}{nC'_{ox}\phi_t - Q'_I}.dQ'_I = \frac{\mu W I_D C'_{ox}}{nL}.\ln\left[\frac{nC'_{ox}\phi_t - Q'_{IS}}{nC'_{ox}\phi_t - Q'_{ID}}\right] \tag{4.11}$$

Note the formal equivalence between the final expression in eq.(4.11) and the flicker noise model in (3.16). The analysis in section 3.3 can then be extended to conclude that the

expression in (4.11) is approximately equal to the square of the gate transconductance, in all the operating regions of the transistor. So $\sum_{i=1}^{N} g_{m_i}^2 \approx g_{mB'}^2$.

ΔI_{β_s} variations in the output current of the current mirror in Fig.4.4(b), due to $\Delta\beta_i$ fluctuations in series transistors, are calculated following the same steps used in equations (4.7) to (4.9) assuming $\Delta V_{Tj} = 0$, $\Delta V_{Ti} = 0$, $\Delta\beta_j = 0$. For a generic M_{bi} transistor:

$$\Delta I_{\beta\_s} = \frac{\partial I_{Di}}{\partial \beta_i}.\Delta\beta_i + \frac{\partial I_{Di}}{\partial V_{Si}}.\Delta V_{Si} + \frac{\partial I_{Di}}{\partial V_{Di}}.\Delta V_{S(i-1)}$$

$$= \frac{I_{Out}}{\beta_i}\Delta\beta_i - g_{ms_i}\Delta V_{Si} + g_{md_i}\Delta V_{S(i-1)} \tag{4.12}$$

summing the equivalent of (4.12) for all the series transistors:

$$N\Delta I_{\beta\_s} = I_{Out}\sum_{i=1}^{N}.\frac{\Delta\beta_i}{\beta} \tag{4.13}$$

Assuming that $\Delta\beta_i$ are non correlated:

$$\sigma^2_{\Delta I_{\beta\_s}} = \frac{I_{Out}^2}{N}.\left(\frac{\sigma_\beta^2}{\beta^2}\right)_u \tag{4.14}$$

Finally, variations ΔI_p in the output current originating from the V_{Tj}, β_j variations in threshold voltage and current factor in parallel transistors M_{aj}, is calculated considering fluctuations in the gate voltage V_G. These fluctuations are expressed as in (4.4) because the input branches of both circuits in Fig.4(a),(b) are essentially the same. Fluctuations in V_G are related to the output current through the gate transconductance of the output transistor g_{mB}'.

$$\Delta I_p = g_{mB'}.\Delta V_G = g_{mB'}\sum_{j=1}^{N}\left[\frac{I_{in}}{g_{ma}}.\frac{\Delta\beta_j}{\beta_j} + \frac{\Delta V_{Tj}}{N}\right] \tag{4.15}$$

Using statistics, and $I_{in}=N^2 I_{Out}$, $g_{mB'} = N g_{ma}$:

$$\sigma^2_{\Delta I_p} = \frac{I_{Out}^2}{N}\left(\frac{\sigma_\beta^2}{\beta^2}\right)_u + \frac{g_{mB'}^2}{N}\left(\sigma^2_{V_T}\right)_u \tag{4.16}$$

The resulting mismatch current standard deviation for the circuit in Fig.4.4(b) is obtained summing the effect of $\Delta I_{V_T s}$ from (4.9), ΔI_{β_s} from (4.14), and ΔI_p from (4.16):

$$\left(\frac{\sigma^2_{I_{Out}}}{I^2_{Out}}\right)_{(b)} = \frac{1}{N}\left[2\left(\frac{\sigma^2_\beta}{\beta^2}\right)_u + 2\frac{g^2_{mB'}}{I^2_{out}}.\left(\sigma^2_{V_T}\right)_u\right] \tag{4.17}$$

To derive (4.16) and (4.17) it has been taken that $g_{mA'}/I_{in} = g_{mB'}/I_{out}$ because both M'_A, M'_B have the same specific current [20]. The case of Fig.4(c) is quite similar to the one in Fig.4(b) but multiple series-composed transistors should be considered.

The analysis can be further extended to the general topology of Fig.4.5. With this configuration:

$$\frac{I_{Out}}{I_{in}} = \frac{S.P}{R.Q} = M \tag{4.18}$$

where P, R, Q and S are the number of unitary transistors in series and parallel in each branch. For this generic case, output current standard deviation is obtained by extending the previous procedure. Owing to simplicity, detailed calculations will not be presented, the resulting mismatch being:

$$\left(\frac{\sigma^2_{I_{Out}}}{I^2_{Out}}\right) = \left(\frac{1}{RS} + \frac{1}{PQ}\right).\left[\left(\frac{\sigma^2_\beta}{\beta^2}\right)_u + \frac{g^2_{mB}}{I^2_{Out}}.\left(\sigma^2_{V_T}\right)_u\right] \tag{4.19}$$

Current fluctuation $\left(\sigma^2_{I_{Out}}/I^2_{Out}\right)_{(c)}$ of the mirror in Fig.4.4(c) can be calculated using (4.19) and P=1, Q=M, R=S=N.

For a 100:1 copy, the circuit in Fig.4.4(a) requires 101 unitary transistors, the one in Fig.4.4(b) only 20, and 200 are required for the circuit in Fig.4.4(c). Meanwhile, from (4.6), (4.17),(4.19), the standard deviation in output current fluctuation is:

$$\left(\frac{\sigma^2_{Iout}}{I^2_{Out}}\right)_{(a)} \approx 5\left(\frac{\sigma^2_{Iout}}{I^2_{Out}}\right)_{(b)} \approx 50\left(\frac{\sigma^2_{Iout}}{I^2_{Out}}\right)_{(c)} \tag{4.20}$$

A major conclusion is that $\sigma^2_{Iout}/I^2_{Out}$ has been substantially reduced from the circuit in Fig.4.4(a) to those of Fig4.4(b) or Fig.4.4(c), thereby proving the relevance of series-parallel association of transistors in current dividers. Note that although squared standard deviation is ten times lower, comparing case (c) to (b), the former also requires 200 unitary transistors against 20. Although a further analysis would improve circuit comparison, a first conclusion is that to achieve the same required mismatch offset the circuits of Fig.4.4(b),(c) are very efficient regarding their occupied area, while that in Fig.4.4(a) is not.

It should be pointed that the estimation of the offset using series-parallel association of transistors, concerning threshold voltage fluctuations, could have been derived with less complexity and the same result, by using the consistent model of annex C and approximations. However, the detailed analysis from eqs.(4.7) to (4.19) allows us to arrive at offset expressions regardless of the mismatch model for the transistor. In effect, expressions for $\left(\sigma_\beta^2/\beta^2\right)_u$ and $\left(\sigma_{V_T}^2\right)_u$ can substitute those in (4.3) for different mismatch models (i.e. [65-67]). It should be noted that variations in β may be related not only to the area as in the simple expression of (4.3). Each transistor boundaries, for example, can also introduce errors in the aspect ratios.

In Fig.4.6 calculated and measured I_{out}, $\sigma_{Iout}^2/I_{out}^2$ in terms of the input current are shown for a 100:1 NMOS current mirror with the topologies of Fig.4.4(a) (M=100) and (c) (M=100, N=10). A σ_{Iout}^2 value was obtained from 10 samples of the circuit in the same run in 0.8µm technology. Unitary transistors were sized W_u/L_u=4µm/12µm, and A_{VT}=.03Vµm, A_β=.02µm values were employed[2] for the offset estimation using (4.6), (4.19). The underestimation in $\left(\sigma_{I_{Out}}^2/I_{Out}^2\right)_{(a)}$ is assumed to come from the simplification in (4.3) of distance-related terms [60,70]. As expected, the measurements indicate a considerable offset reduction from (a) to (c).

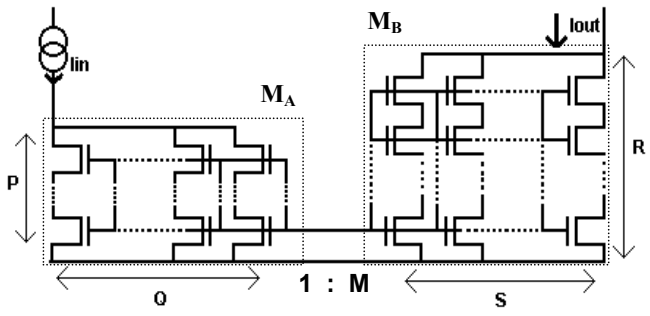

Figure 4.5: Schematic of a generic series-parallel current mirror with a copy factor M=(SP)/(RQ). All unitary transistors are supposed equal having the same $(\sigma_\beta/\beta)_u^2$, $(\sigma_{VT})_u^2$.

[2] These values are obtained from [5,70] but them were extracted for technologies with a greater minimum gate legth. However, from our previous experience with the target proccess, these A_{VT}, A_β, accurately help to predict offset in several circuits: opamps, transconductors, etc. Since an adequate mismatch parameter extraction was not performed in this study, nor mismach parameters are provided by the IC manufacturer, A_{VT}=.03$V\mu m$, A_β=.02μm values were chosen for offset estimation. Along this work, offset estimations and measurements shown an adequate accordance in all cases.

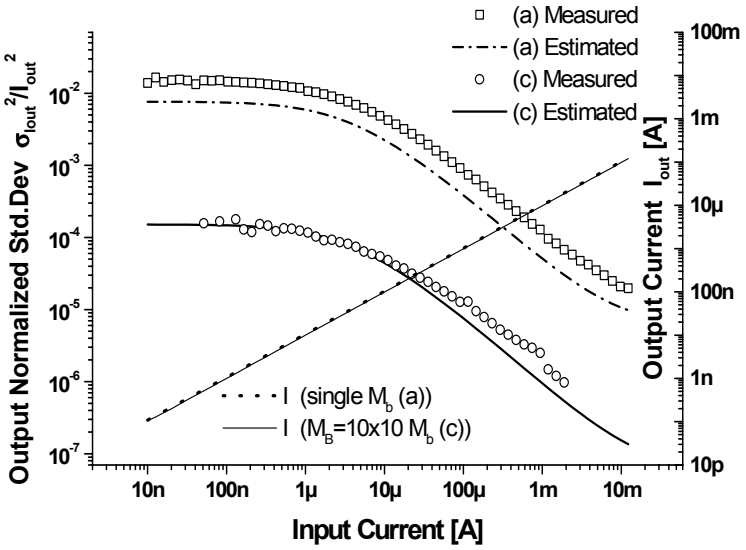

Figure 4.6: Calculated and measured I_{out}, $\sigma_{I_{out}}^2 / I_{out}^2$ in a 100:1 current copier as in Fig.1(a) and (c).

Current copiers with different copy factors are usual in analog integrated circuits; therefore series-parallel association of transistors is a powerful tool for the designer. For example, by combining several series-parallel unitary transistors as in Fig.4.7, it is possible to derive a wide range of copies of a single bias current, as usually required in analog design, very efficiently in terms of area and mismatch. The circuit in Fig.4.7 has been designed to derive 120nA and 10nA currents for bias analog circuitry from a single 40nA reference. It occupies only 0.015mm^2 and the expected standard deviation is σ_{Iout1}=1.4nA, σ_{Iout2}=0.26nA, using W_u/L_u=15µm/20µm unitary transistors.

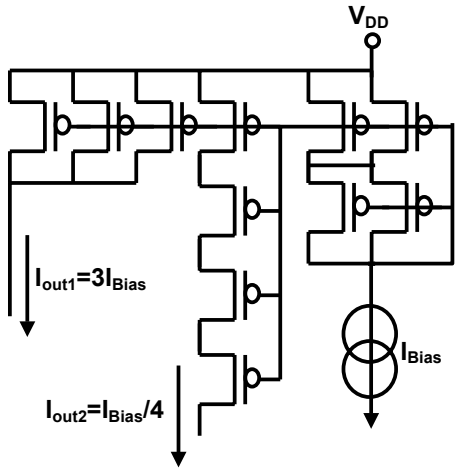

Figure 4.7: An efficient 4:1, 1:3 current copier.

4.2.1 - Thermal and flicker noise.

Consistent models for both thermal and flicker noise have been presented in chapter 3, preserving series-parallel association properties of transistors, essential for the analysis of circuits like those in Fig.4.2-4.5. Simplified empirical models have been shown to accurately approximate consistent ones, and may be used to compute, in a simple manner, the output current noise of the series-parallel current mirror in Fig.4.5. In effect, using expressions (3.23) and (3.27) to estimate noise, the output current noise is obtained.

Thermal noise:
$$\frac{S_{I_{Out}w}}{I_{Out}^2} \approx 2nk_BT\left(\frac{g_{mB}}{I_{Out}}\right)\left(\frac{1}{I_{in}}+\frac{1}{I_{out}}\right) \tag{4.21}$$

Flicker noise:
$$\frac{S_{I_{Out}\frac{1}{f}}}{I_{Out}^2} = \frac{q^2N_{ot}}{nC_{OX}'^2(WL)_u}\left(\frac{1}{RS}+\frac{1}{PQ}\right).\frac{g_{mB}^2}{I_{out}^2}.\frac{1}{f} \tag{4.22}$$

The expression for flicker noise, is analogous to the expression for mismatch. It is important to remark, from the analysis of (4.21) and (4.22), that output noise does not increase significantly when using series-parallel current mirrors even with extremely high current division factors (I_{out}<<<I_{in}) .

4.2.2 - Further considerations on systematic offset.

Although using series-parallel current copiers, as described, may help to drastically reduce random mismatch effects, for certain current copiers systematic offset may become the main offset source. In example, owing to the drain transconductance $g_{ds\_A''}$ of M_A" in Fig.4.4(c), part of the input current is not 'copied' and it can be seen as derived through a series resistor r_{ds_A} in series with M_A" (small signal analysis). On the output branch, the output conductance of M_B" can be considered negligible $r_{ds\_B} >> r_{ds\_A}/100$ due to its channel length and drain current. There is therefore a systematic current error at the output, that becomes more visible as M_A enters the strong inversion region because g_{ds_A} increases, as does the drain voltage of M_A.

To cancel systematic offset effects, and observe only the effect of random mismatch, in the plot of Fig.4.6 the standard deviation at the output has been calculated as:

$$\sigma_{Iout}^2 = \frac{1}{K}\sum_{i=1}^{K}\left(I_{out_i} - \langle I_{out}\rangle\right)^2 \tag{4.23}$$

where K=10 is the number of measured ICs, I_{out_i} is the output current of each IC, and $\langle I_{out}\rangle$ is the average output current, which when no systematic offset is present, is expected to be the input current divided by 100. Normally $\langle I_{out}\rangle \neq I_{in}/100$ due to systematic current offset, but this does not affect σ_{Iout}^2 in eq.(4.23) because systematic errors are cancelled out since they are included in both $I_{out_i}, \langle I_{out}\rangle$. The plot of Fig.4.8 repeats that of Fig.4.6; in addition it includes the same measurements but the alternative definition

$$\sigma_{Iout}^2 = \frac{1}{K}\sum_{i=1}^{K}\left(I_{out_i} - \frac{I_{in}}{100}\right)^2 \tag{4.24}$$

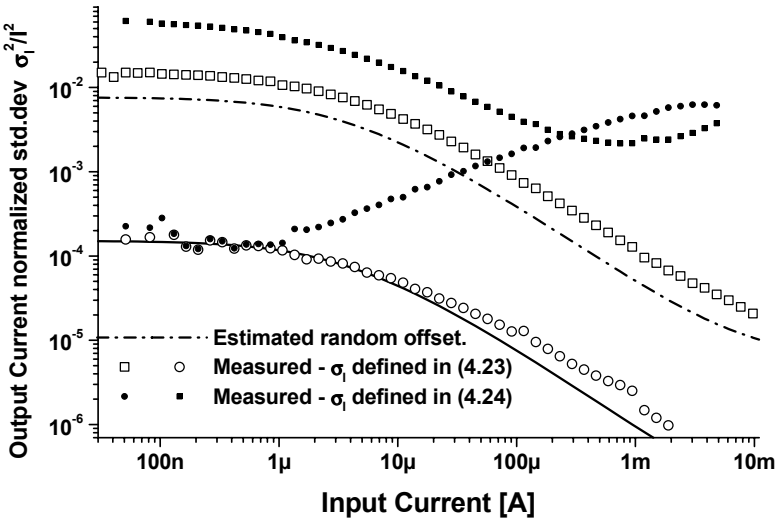

Figure 4.8: Calculated and measured $\sigma^2_{I_{Out}} / I^2_{Out}$ in a 100:1 as in Fig.4.6, and using the definition in (4.24) for $\sigma^2_{I_{Out}} / I^2_{Out}$. It is clear the influence of systematic offset specially at strong inversion, while at weak inversion random mismatch effect dominates.

substitutes that in (4.23). Because systematic offset is no longer cancelled, the result of the new plot may be different. At weak inversion the plots in Figs.4.6, and 4.8 are near equal (it is only possible to observe a slight shift attributed to the offset of the measurement system) but the previously observed offset reduction decreases as the transistor enters the strong inversion region.

Summarizing, in a precision current copier using series-parallel association of transistors, systematic offset may affect the accuracy particularly when transistors operate at strong inversion. But the effect has been shown (estimation-simulations-measurements) not to be significant in the designs of this and the following chapter, where the circuits operate mostly in the weak inversion region.

4.3 OTAs WITH SMALL TRANSCONDUCTANCE AND EXTENDED LINEAR RANGE.

In this section, series-parallel transistors for current division are applied in standard OTAs to obtain extremely low transconductances with an extended linear range.

4.3.1 - Series-Parallel division OTAs: Basic Idea.

To achieve a low transconductance OTA with an extended linear range, the current divider of Fig.4.4(b) - or that in Fig.4.5 with more generality - may be employed to divide by a high factor the output current of a MOS differential pair biased in moderate or strong inversion that has an enhanced linear range. This circuit scheme is shown in Fig.4.9. For the NMOS current mirrors, N unity transistors M_2 are placed in series or in parallel to achieve an effective output transconductance G_m,

$$G_m = g_{m1} / N^2 \tag{4.25}$$

where g_{m1} is the tranconductance of the transistors M_1 in the differential input pair. Biasing the input pair at strong inversion, the linear range of the transistor may be extended to a desired value predicted, in terms of the inversion level i_{f1} of M_1, using (2.25). By using a high division factor N^2, it is possible to obtain transconductances in the order of pico-A/V, limited only by leakage current [35]. For example, using this technique, a 33 pico-A/V transconductor with a ±150mV linear range has been designed, and tested in section 4.4.2.

Although biasing the input differential pair deep in strong inversion allows a wide linear range to be achieved, it may not be suitable for a low voltage power supply. In this case the series-parallel current division technique is still valuable but a different topology for the input pair is required as, for example, the ones proposed in [37,48,49]. In Fig.4.10 a series-parallel OTA with the linearized differential pair of [49] is shown.

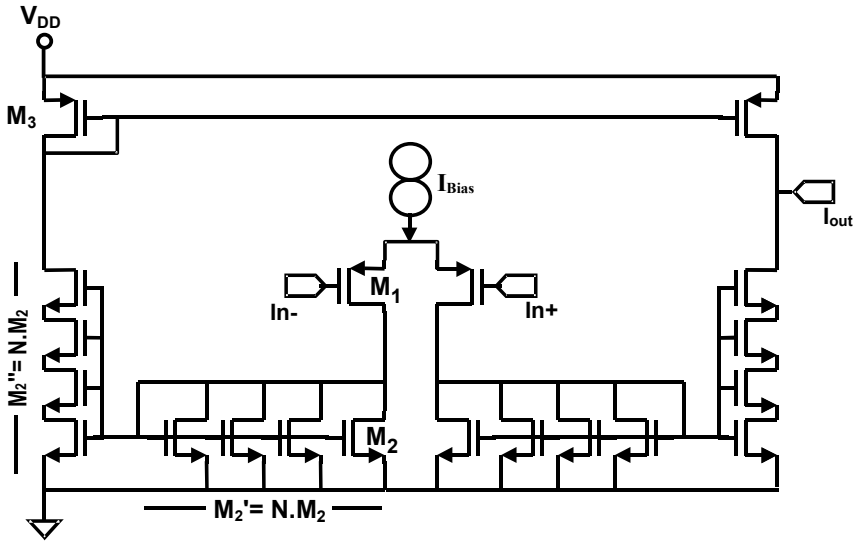

Figure 4.9: Circuit topology for a series-parallel current division OTA.

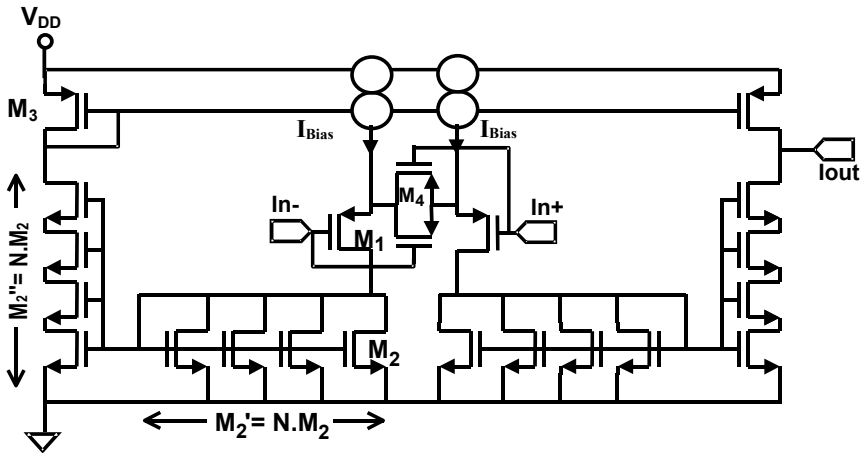

Figure 4.10: Circuit topology for a series-parallel current division OTA using a linerized input pair. This topology will be used for G_{m5}-G_{m6} in section 4.4.3.

4.3.2 - What is the minimum effective G_m possible with this technique?

The output branch in Fig.4.9 may be biased with a current as low as a few pA. Operation at such low currents is still reliable when using long channel transistors (such as M_2") [35]. Transistor size was shown not to be a limitation (see section 4.4 or [19]). Consequently, the only limitation to an extremely low bias current is the sum of the leakage at the source (drain) of each series transistor in M_2". Leakage current should be much less than bias current in the same branch, not only to allow proper transistor operation, but also to reduce the offset originating from leakage mismatch. For hand calculations, leakage mismatch was estimated as 25% [100].

Leakage currents were estimated from the manufacturer's data-sheet for the target process, including both area, and perimeter coefficients[3]. For this technology, as well as for others examined, leakage in p-doped diffusions are notoriously higher than those in an n-doped diffusion. The relation is near 4 times greater in this case. Because it will include a large number of source and drain diffusions in its layout, the series branch of the current mirror in Fig.4.9 or Fig.4.10 is the main leakage contribution. For this reason all the OTAs that will be presented include a PMOS differential pair, and a NMOS series-parallel current mirror. For the selected technology, the leakage current was estimated as I_{leak}=3fA for a 4µm x 2µm n+ diffusion.

The selected design criterion is that the leakages should be at least 10 times smaller than the bias current in the output branch of the current mirror:

$$\sum I_{leak} = N.I_{leak} < \frac{\frac{1}{2} I_{Bias}}{10N^2} \tag{4.26}$$

[3] The leakage for a single sorce(drain) is estimated as the sum of the area and perimeter of the source(drain), multiplied respectively by the area and perimeter leakage coefficients for a n+diffusion-p-substrate diode in the case of NMOS transistor (or p+diffusion - n-well diode in the case of a PMOS transistor).

(½I_{Bias} is the bias current of each transistor in the input pair) which imposes a limit on the minimum achievable transconductance G_{mX}. Using a non-degenerate differential input pair, a worst case estimate for the minimum G_{mX} according to (4.26) is 15pS, equivalent to a 60GΩ resistor. This value was estimated for N=100, and g_{m1}/I_d = 5 at the input pair, that is (although reasonable) an arbitrary worst case condition. To fix a non-arbitrary limit for the minimum achievable transconductance, eq.(4.26) should be examined according to specific circuit restrictions like area, power consumption, linear range (i.e., if no restrictions apply, the bias current can be selected as low as necessary to achieve an extremely low transconductance in detriment of the linear range). Using (4.25) it is possible re-write (4.26) including G_m:

$$G_{mX}^{3/2} > 10.\left(g_m/I_d\right)_1^{3/2}.I_{leak}.\sqrt{\tfrac{1}{2}I_{bias}} \tag{4.27}$$

Because in a differential pair, the linear range is a function of the inversion level, the latter is fixed. A fixed i_f in the moderate or strong inversion region (for a enhanced linearity), limits the minimum bias current because an arbitrary large transistor cannot be realized. So, examining eq.(4.27), the minimum G_{mX} value is a function of the circuit topology, desired linear range, and available transistor area.

4.3.3 - Design methodology.

In this section there is presented a design methodology to obtain bias current, transistor size, and current division factor, in an OTA with a required transconductance and linear range.

The relation between the linear range of a differential pair and i_f deduced in chapter 2, is very convenient for design. Suppose an analog circuit that requires a transconductor with an extremely low G_{mX} value, and an input linear range V_{Lin_X}; using the topology of Fig.4.9 the inversion level i_{f1} of the input pair is determined by that relation in eq.(2.25a-b). For a given bias current, the normalization current is $I_S = 2I_{bias}/i_{f1}$. g_{m1} from eq.(2.16), $\left(W_1/L_1\right)$ from I_S definition, and $N = \sqrt{g_{m1}/G_{mX}}$ from eq.(4.25), can then be determined. The design space has been reduced to a single dimension, the bias current of the input pair that can be determined from the power consumption and area budgets. M_2, and M_3, in Fig.4.9 only influence leakage currents, matching, and noise; their size may be selected depending on whether the circuit is oriented to minimum area, noise, or matching. Fig.4.11 shows a scheme of the proposed design methodology for series-parallel OTAs.

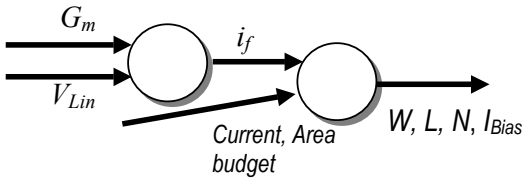

Fig.4.11: A scheme for the design procedure of a series-parallel OTA.

If a linearized differential pair as in Fig.4.10 is used, the linearity estimation of eq.(2.25a-b) is no longer valid. Either an alternative expression (using the guidelines in annex D or [49,101]), or simulation, is required to determine the linear range and use the proposed methodology.

4.3.4 - Noise and offset analysis.

It is expected that series-parallel association of transistors would not drastically increase noise. A simple noise calculation for an OTA like the one in Fig.4.9, is possible considering that $M_2^{"}, M_3$ are in weak inversion and $N^2 >> 1$. The detailed calculation is presented in annex D. The approximated equivalent thermal noise at the input results in:

$$v_{input\_w}^2(f) \approx \frac{4nk_BT}{G_m}(\sqrt{1+i_{f1}}+1) \tag{4.28}$$

Note that expression (4.28) is very similar to that obtained for a simple symmetrical OTA, but here we are paying a price in noise for the linearization represented by the factor $(\sqrt{1+i_{f1}}+1)$. An equation similar to (4.28) can be derived for flicker noise (see annex D) where a noise surcharge dependent on the same $(\sqrt{1+i_{f1}}+1)$ factor is also observed.

We have been paying special attention to offset throughout this chapter. Although sometimes dominant, series-parallel mirrors are not the only offset source. All transistors contribute to offset in the OTA of Fig.4.9: input differential pair transistors M_1, PMOS current mirror transistors M_3, and series-parallel current dividers. In the case of the linearized pair in Fig.4.10, transistors M_4 do not introduce offset because voltage at the source of both input transistors M_1 is the same at V_{in}=0 but an extra offset is introduced by the current mirror M_5 - shown in Fig.D.2 of annex D - that generates bias currents for the differential pair.[4]

4.4 DESIGN EXAMPLES.

Several OTA structures were designed, fabricated in a 0.8μm standard CMOS technology, and tested, to characterize the above described circuit technique. These OTAs named G_{m2}, G_{m3}, G_{m4}, G_{m5} - G_{m6}, fulfill the requirements of the low frequency band-pass filter of chapter 5. G_{m5}, G_{m6}, are built together, taking advantage of the same linearized input pair (to reduce the area), but using different current mirrors. The detailed design procedure of each OTA, as well as OTA measurements are presented below.

[4] A detailed offset estimation for series-parallel current division OTAs using either standard, and linearized, differential input pairs is also presented in annex D.

4.4.1 - G_{m2}: 2.35 nS OTA with 150mV linear range.

The requirements for G_{m2} are as follows: 2.35nS transconductance with V_{Lin} = 150mV linear range with α=10% using the definition from (2.20). With such a modest linear range, in principle it should be enough to choose a standard differential input pair with series-parallel current division as in Fig.4.9. The previously presented methodology is used for transistor biasing. Starting with the minimum required V_{Lin} , the inversion level of transistor M_1 is constrained to $i_{f1} \geq 25$ using (2.25b). The inversion level is fixed by the bias current and the size of M_1 so, to select the transistor size the curve of Fig.4.12 is employed. This plot shows the size of the transistor against bias current at i_{f1} = 25, supposing a transistor width W_{min} of 4μm. Bias current is chosen as 21nA (each M_1) because:

- It is a reasonable value for the application.
- It is an exact multiple of the bias current of G_{m1} - in chapter 3 - which simplifies bias circuitry.
- It gives a reasonable area (<500μm^2) for the input transistors M_1. Much smaller values for the transistor gate area may also lead to an undesirable offset value.

Finally a definitive size of $(W/L)_1$=110/5 [5] was chosen but this is quite arbitrary. It was selected to re-use a similar layout block from a previous circuit.

In order to achieve the required division factor of 72, a series-parallel current division using Q=18 parallel transistors, that copy to an array of R=8 series by S=2 parallel ones is used. Eq.(4.25) is re-written as $G_m = g_{m1}/(RQ/S)$. M_2 transistors are sized $(W/L)_2$ = 4/8 which is quite reasonable for a unitary transistor. Main transistor biasing data for the circuit as well as layout structure for each transistor are shown in Table 4.1. It should be pointed out that for the sake of matching, in all cases transistors were drawn using arrays of smaller unitary transistors (see section 4.6). The total gate areas of transistors in G_{m2} and the other OTAs, were chosen to be always in the same order because a single M_1, M_2', M_2'', or M_3 small transistor may introduce a high amount of flicker noise and mismatch offset to the whole OTA circuit. The current mirror transistors M_3 are sized $(W/L)_3$ = 8/64.

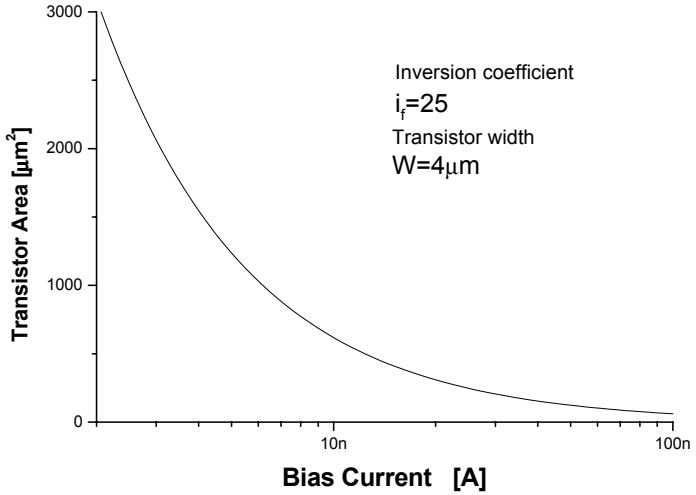

Figure 4.12: Gate area of the input transistor in G_{m2} as a function of the bias current.

[5] Otherwise indicated, transistor size are expressed from now in μm/μm.

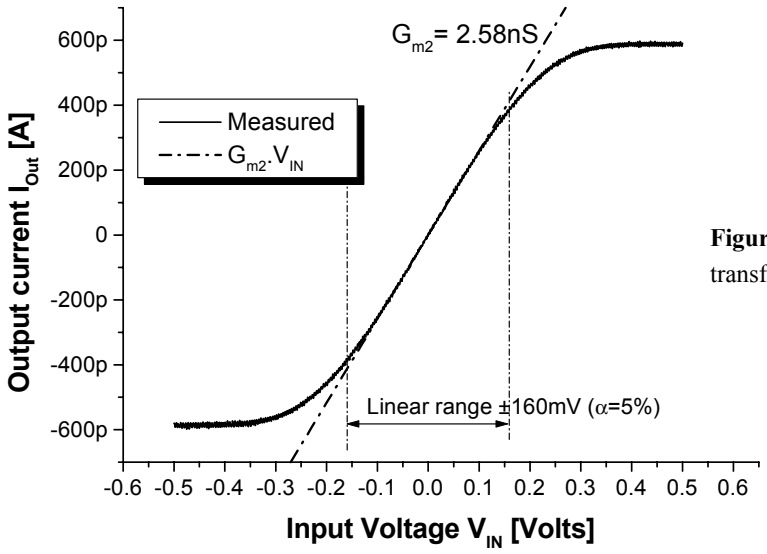

Figure 4.13: Measured transfer characteristic of G_{m2}.

In Fig.4.13 the measured transfer function of G_{m2} is shown along with its linear range, the observed transconductance was 2.58nS against the expected value of 2.35nS. Measurements were obtained with the aid of an HP4155 semiconductor parameter analyzer at a power supply voltage V_{DD} = 2.8V and one input fixed at V_{Bias}=0.7V. For G_{m2} to G_{m6}, measurements were repeated at V_{DD}=2.4V, V_{DD}=2V[6] to demonstrate that the circuit fulfills the requirements of the filter in chapter 5. A brief discussion on input and output voltage swing is presented in section 4.5 while in Table 4.5 either measured or estimated transconductance, noise, input offset, circuit area, from G_{m1} to G_{m6} are presented. In annex E, detailed schematics for this and all the other OTAs are shown.

Transistor	W/L	g_m	I_{Bias}	g_m/I_D	i_f
M_1	5/110	174 nS	21nA	8.3	34
M_2'	72/8	580nS	21nA	25	.057
M_2"	8/64	7.5nS	291pA	26	.057
M_3	8/64	8.2nS	291pA	28	.017

Transistor	Array structure	$(W/L)_u$	Gate Area	Total Transistor Area
M_1	11 series	5/10	550µm^2	0.011 mm^2 [1]
M_2'	18 parallel	4/8	576µm^2	0.0087 mm^2 [2]
M_2"	8 series x 2 parallel	4/8	512µm^2	
M_3	8 series x 2 parallel	4/8	576µm^2	0.0084 mm^2 [1]

Table 4.1: Transistor sizing and layout structure for G_{m2}. All dimensions refer to drawn values.
[1] Area of 2 matched transistors i.e. M_1. [2] Total area of matched mirror.

[6] G_{m5-6} shown a slight performance degradation at 2V supply voltage as indicated in section 4.5.

4.4.2 - G_{m3}: 35 pS OTA with 150mV linear range.

The requirements for G_{m3} are as follows: 35pS (30GΩ!) transconductance with 150mV linear range. Mismatch offset should be as low as possible because this transconductor will be employed for offset cancellation. Since the required linear range is the same, the layout of the input pair of G_{m2} is re-utilized. The circuit topology is still that in Fig.4.9 using N=70 series-parallel M_2 transistors to achieve the required 35pS with a N^2=4900 division factor. M_2 transistors are sized $(W/L)_2$ = 4/4. The current mirror transistors M_3 are sized $(W/L)_3$ = 20/60. M_3 size is selected to be large enough to neglect the effect of its output conductance.

In Fig.4.14 the measured transfer function of G_{m3} is shown. Direct measurement of such low currents may be very inaccurate so the indirect measurement setup of Fig.4.15 [35] was used. G_{m3} charges an internal 2pF capacitor (connected to an output buffer) that is periodically discharged, the transconductance is measured with the slope of the charging (discharging) curve. The resulting transconductance is 33pS. Also an indirect measurement of the input noise [35] of 140μV_{rms}, in the band from 0.5-10Hz, was possible.

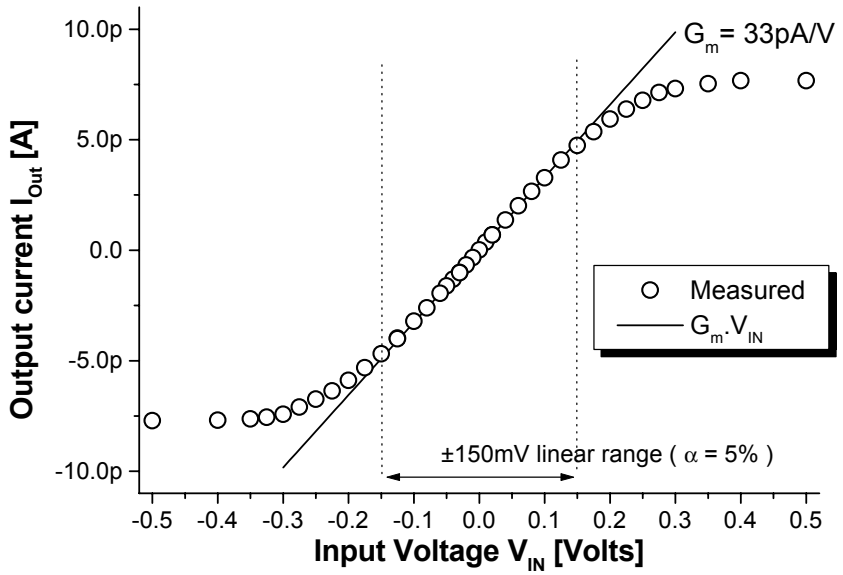

Figure 4.14: Measured transfer characteristic of G_{m3}.

Concerning offset, in Table 4.5 individual measurements for the 10 ICs used for offset characterization of G_{m3} (as well as the rest of the OTAs) are shown. Note that an extremely low transconductance has been implemented without a significant penalty in input offset voltage.

In Table 4.2 main transistor biasing data for the circuit as well as the layout structure for each transistor are shown. Because G_{m3} is designed to directly attack an unprotected output pad, protective double guards were added to all transistors.

Transistor	W/L	g_m	I_{Bias}	g_m/I_D	i_f
M_1	5/110	174 nS	21nA	8.3	34
M_2'	280/4	546nS	21nA	26	0.007
M_2"	4/280	110pS	4.3pA	26	0.007
M_3	20/60	120pS	4.3pA	28	0.003

Transistor	Array structure	$(W/L)_u$	Gate Area	Total Transistor Area
M_1	11 series	5/10	550μm^2	0.012 mm^2 [1]
M_2'	70 parallel	4/4	576μm^2	0.026 mm^2 [2]
M_2"	70 series	4/4	512μm^2	
M_3	4 parallel	5/60	576μm^2	0.012 mm^2 [1]

Table 4.2: Transistor sizing and layout structure for G_{m3}. All dimensions refer to drawn values.
[1] Area of 2 matched transistors i.e. M_1 - includes protective guard.
[2] Total area of matched mirror - includes protective guard

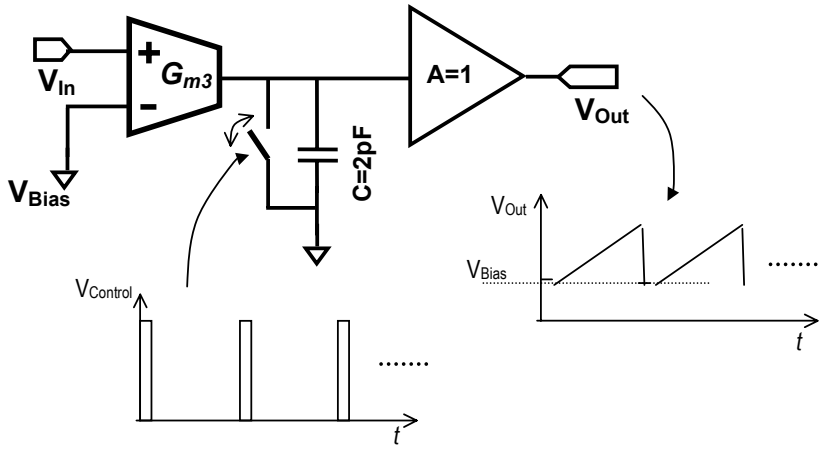

Figure 4.15: Measurent circuit employed for the characterization of the output current of G_{m3}.

4.4.3 - G_{m4}: 21 nS OTA with 150mV linear range.

The requirements for G_{m4} are a 21nS transconductance with 150mV linear range. No other strict requisites apply, so the input pair of G_{m2} is once again used. With the schematic in Fig.4.9, an 8:1 M_2'-M_2" mirror is required. The selected layout is composed of 28 $(W/L)_u$=4μ/12μ transistors in parallel to form M_2', while M_2" is an array of 7 parallel by 2 series of the same unitary transistors. Such a configuration was selected to reuse the NMOS current mirror in section 4.4.4 with a minimum of changes. Due to practical considerations when prototyping the IC, an isolated G_{m4} was not fabricated, thus there are no measurement results for this OTA. A simulation of the transference of G_{m4} is given in Fig.4.16.

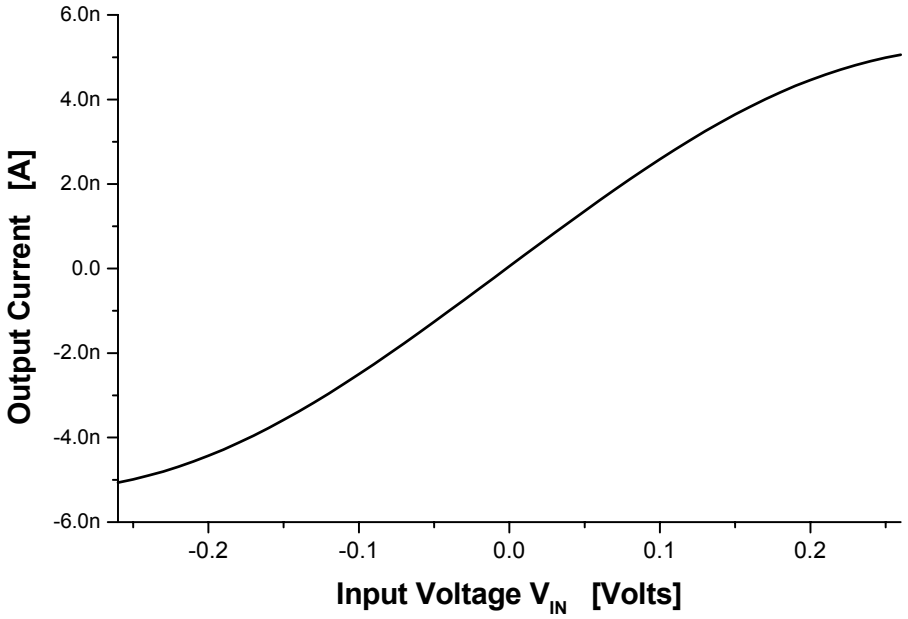

Figure 4.16: Simulated transfer characteristic of G_{m4}.

4.4.4 - G_{m5}, G_{m6}, 2.4 nS, and 89 pS OTAs with ±500mV linear range.

The requirements for G_{m5}, G_{m6} are: 2.5nS, 89pS transconductances with at least 500mV linear range. Mismatch offset is critical in G_{m6} because it will be used in an offset cancellation loop. Because the elevated linear range requires the input pair to be in deep strong inversion which is impractical at low power supply voltage, the linearized architecture of Fig.4.10 was selected. Because the input pair structure resulted large, and since G_{m5} and G_{m6} are connected to the same input nodes in the filter, they share the linearized input pair but use a different current divider, to minimize the occupied area. They will be represented as in Fig.4.17 while a detailed circuit schematic is shown in annex E. The selected solution is the following: a effective transconductance g_{m_eff} = 70nS linearized pair was designed according to the guidelines in [49] (or see annex D) and simulation, using 21nA bias currents, resulting in the transistor sizes of table 4.3. N^2 = 784 division factor was selected by using N=28 series-parallel M_2 transistors in G_{m6}. M_2, M_3 transistor size were selected to be as large as possible to reduce offset. Finally, G_{m5} requires a 28 division factor. Since in the input branch of G_{m5} (shared with G_{m6}) there are 28 parallel transistors, an optimal solution to preserve a reduced offset is to place a 5x5 square transistor in the output branch, resulting in a topology similar to the current mirror in Fig.4.4(c).

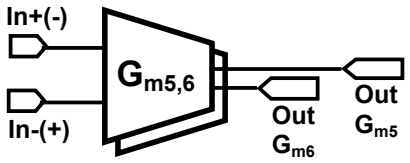

Figure 4.17: G_{m5}, G_{m6} share the input stage.

In Figs.4.18-4.19, the measured transfer functions of G_{m5}, G_{m6} [7] are shown along with their linear range. The offset increase in Table

[7] The measurement setup of Fig.4.15 was employed for G_{m6} with a 50pF charging capacitor.

4.4 of G_{m5}, G_{m6}, in comparison to G_{m1}, G_{m2}, G_{m3}, is a consequence of the use of the linearized input pair, but see annex D for a clear identification of excess offset sources.

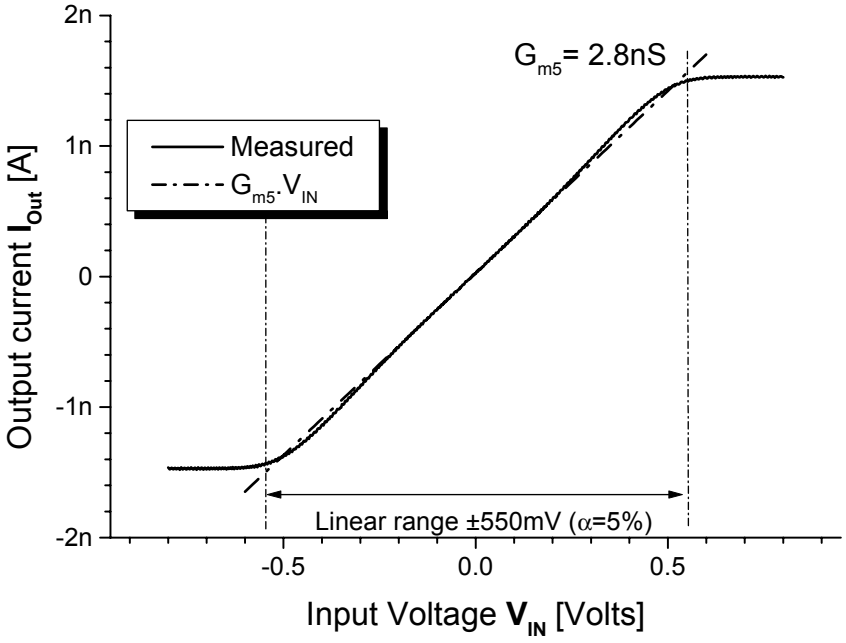

Figure 4.18: Measured transfer characteristic of G_{m5}.

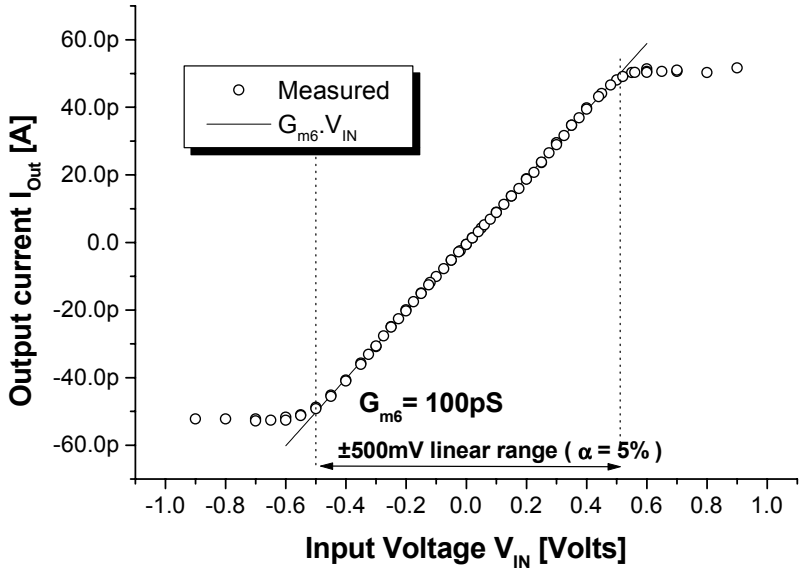

Figure 4.19: Measured transfer characteristic of G_{m6}.

Transistor	W/L	g_m	I_{Bias}	g_m/I_D	i_f
M_1	10/130	174 nS	21nA	8.3	34
M_4	5/520	linear region			
	Total linearized input pair g_{m1_eq}=70nS				
M_2'	112/12	550nS	21nA	26	0.051
M_2" - G_{m5}	20/60	19.5nS	0.75nA	26	0.051
M_2" - G_{m6}	4/336	0.7nS	27pA	26	0.051
M_3 - G_{m5}	20/60	19nS	0.75nA	25	.16
M_3 - G_{m6}	20/60	0.75nS	27pA	28	0059

Transistor	Array structure	$(W/L)_u$	Gate Area	Total Transistor Area
M_1	13 series x 2 parallel	5/10	1300µm^2	0.076 mm^2 [1]
M_4	52 series	5/10	2600µm^2	
M_2'	28 parallel	4/12	1344µm^2	0.029 mm^2 [2]
M_2" - G_{m5}	5 series x 5 parallel	4/12	1200µm^2	
M_2" - G_{m6}	28 series	4/12	1344µm^2	
M_3- G_{m5},G_{m6}	4 parallel	5/60	576µm^2	0.012 mm^2 [3]

Table 4.3: Transistor sizing and layout structure for G_{m5}, G_{m6}. All dimensions refer to drawn values.
[1] Area of 4 matched transistors M_1 , M_4.
[2] Total area of matched mirror.
[3] Area of 2 matched transistors M_3.

4.5 - INPUT AND OUTPUT DYNAMIC RANGE.

Consider an OTA with a given linear range V_{Lin}; one input is connected to a fixed bias voltage V_{Bias}, and the other to an input voltage V_{in} varying in the range $(V_{Bias}\text{-}V_{Lin}) < V_{in} < (V_{Bias} + V_{Lin})$ (Fig.4.20). What is the range of voltages for V_{Bias} that guarantees a proper operation of the OTA in the full range of V_{in}?. As in a classic common-mode range analysis, transistors M_1, M_2, M_{Bias} in Fig.4.20 must operate in saturation. The upper boundary for V_{Bias} appears when focusing on $M_{1\text{-}a}$:

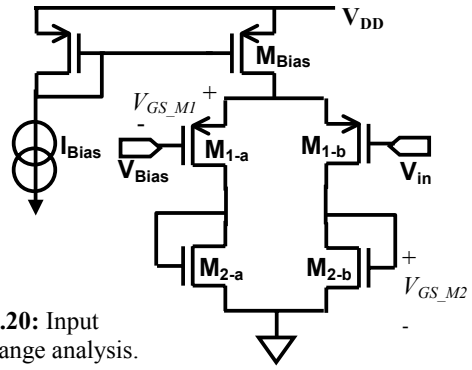

Figure 4.20: Input voltage range analysis.

$$V_{DD} - V_{DSsat_{MBias}} - V_{GS_{M1-a}} > V_{Bias} \tag{4.29}$$

What is slightly different to classical input common mode range analysis is that eq.(4.29) must be valid for the whole range of V_{in}. Particularly at V_{in}=($V_{Bias} + V_{Lin}$) most of the current is channeled through $M_{1\text{-}a}$ so $V_{GS_{M1}}$ should be calculated with a drain current $I_{D1} = I_{Bias}$ (twice its value at bias condition with a null differential input). When the input voltage goes down the limit is $M_{1\text{-}b}$

$$V_{GS_{M2}} + V_{DSsat_{M1}} - V_{GS_{M1-b}} < V_{Bias} - V_{Lin} \tag{4.30}$$

with similar considerations about $V_{GS_{M1}}$. It should be stated that equations (4.29) and (4.30) are still valid for the circuit in Fig.4.10. When estimating the input range for G_{m6} - the most compromised OTA regarding dynamic range due to its large input signal - with V_{DD} = 2V, the result is 0.3V<V_{Bias}<0.6V; the latter value is in accordance to measurements in Fig.4.22.

The other voltage limitation in G_{m6} is at the output because both $M_{2''}$, $M_{3,}$ in Fig.4.10 must operate in saturation. Even at low currents with both transistors operating in weak inversion, V_{DSsat} will be around 150mV. However a measured G_{m5} OTA demonstrated to operate with its output at 100mV without an observable performance degradation.

Fixing the appropriate V_{Bias} for adequate operation at nominal V_{DD}=2.8V and up to 2V, is a problem at circuit level and it will be discussed on chapter 5.

In the plot of Fig.4.21 several simulations of the transference of G_{m6} while varying the bias voltage, and threshold voltage V_{TP} of the input pair transistors are shown. V_{TP} is important because it strongly affects $V_{GS_{M1}}$ in eq.(4.29). At the typical V_{TP} value of 0.8V, the OTA operates as expected, but the curves are affected as the input voltage increase for increasing V_{TP} or V_{Bias} values. In this study, all the designed OTAs have been simulated with a typical transistor model, and measured, to properly operate across their entire required linear range, up to 2V, with a 0.7V V_{Bias}. Simulations where also performed with worst case BSIM3v3 models provided by the foundry, and the ACM model with V_{TP}=1V, at V_{DD}=2V, and V_{Bias}=0.6 - 0.7 V. Although under these conditions, the input voltage in some cases is pushed outside the permitted boundaries and the transfer function is slightly modified as in Fig.4.21, 4.22, these worst cases where judged not to seriously affect circuit performance. The reason for this is that the target application allows a slight degradation in performance at 2V operation at the end of the pacemaker's life. As an example, in Fig.4.22, several measured curves for G_{m5} showing its transference at several bias and power supply voltages are presented.

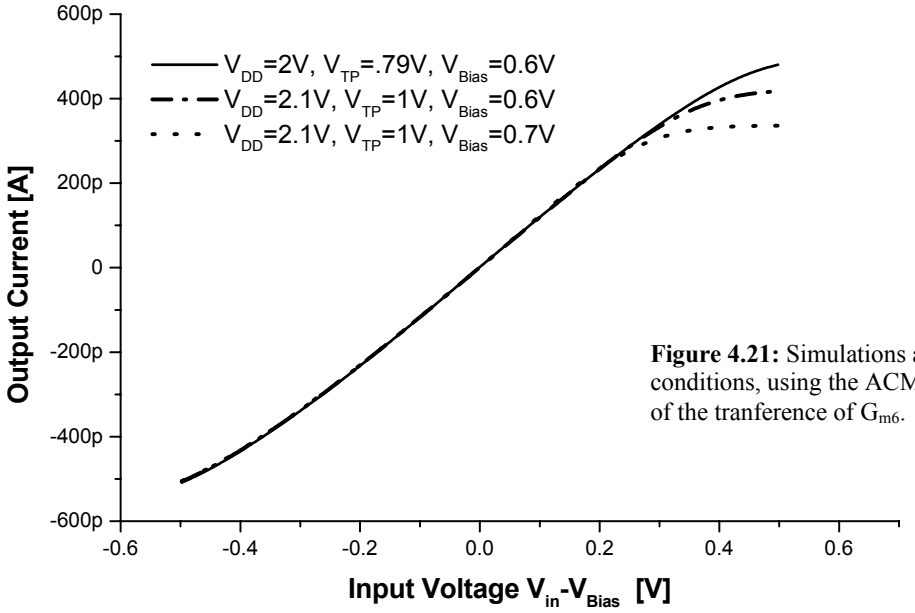

Figure 4.21: Simulations at various conditions, using the ACM model, of the tranference of G_{m6}.

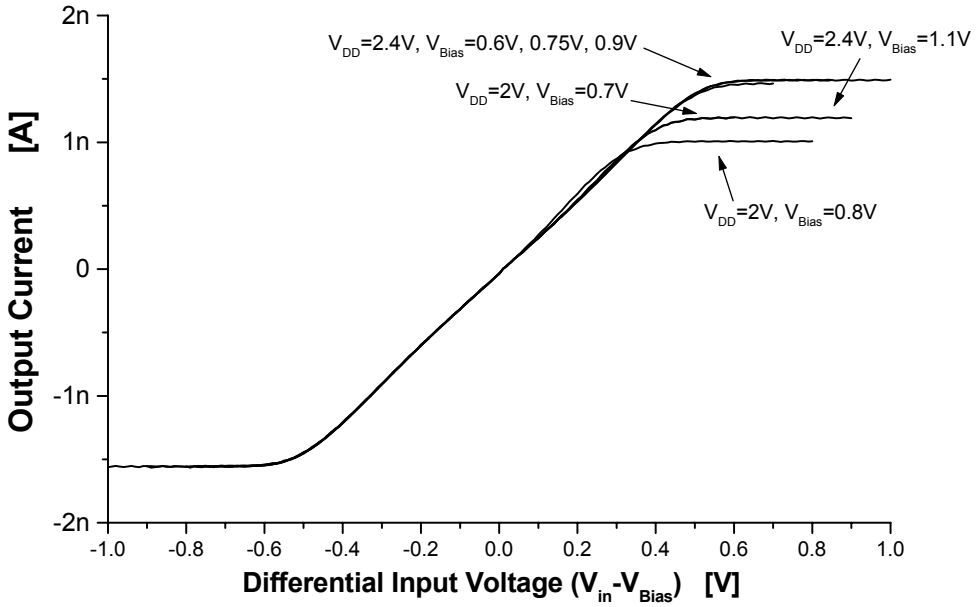

Figure 4.22: Measurements at various conditions, of the output current vs. input voltage of G_{m5}.

4.6 LAYOUT TECHNIQUES.

Adequate layout techniques should be employed to obtain a reduced mismatch between transistors. The layout structure used for matched transistors, whether differential pair or series-parallel current mirrors, was in all cases the same: a large row of equal sized transistors placed together at minimum distance, and then connected with metal wires. The layout editor employed was Tanner L-Edit.

The layout technique can be seen in e Fig.4.23, corresponding to G_{m2}. Particular care was taken to:
- When matching two arrays M_A, M_B, of transistors, if one unitary transistor of the row corresponds to M_A, their neighbors correspond to M_B. If more than two arrays are matched together, unitary transistors are also interleaved.
- At both ends of the row there are dummy structures.
- No minimum size transistors are employed. Minimum allowed distance is preserved between unitary transistors.
- Current flow direction is always the same in unitary transistors.

For example, to realize in G_{m2} a 72:1 current mirror composed of 18 transistors in parallel copying to an array of 8series-by-2parallel unitary ones, a 36-transistor row is drawn. The last transistors on the left and on the right are shortened (dummies). Odd transistors are connected in parallel, while even ones are connected in the 8 by 2 array[8]. Connections are set up so that current flows is in the same direction for all 34 active transistors (drain is always up).

[8] There are 17 even transistors, a single even transistor is also connected in parallel to the odd ones to complete 18 parallel transistors.

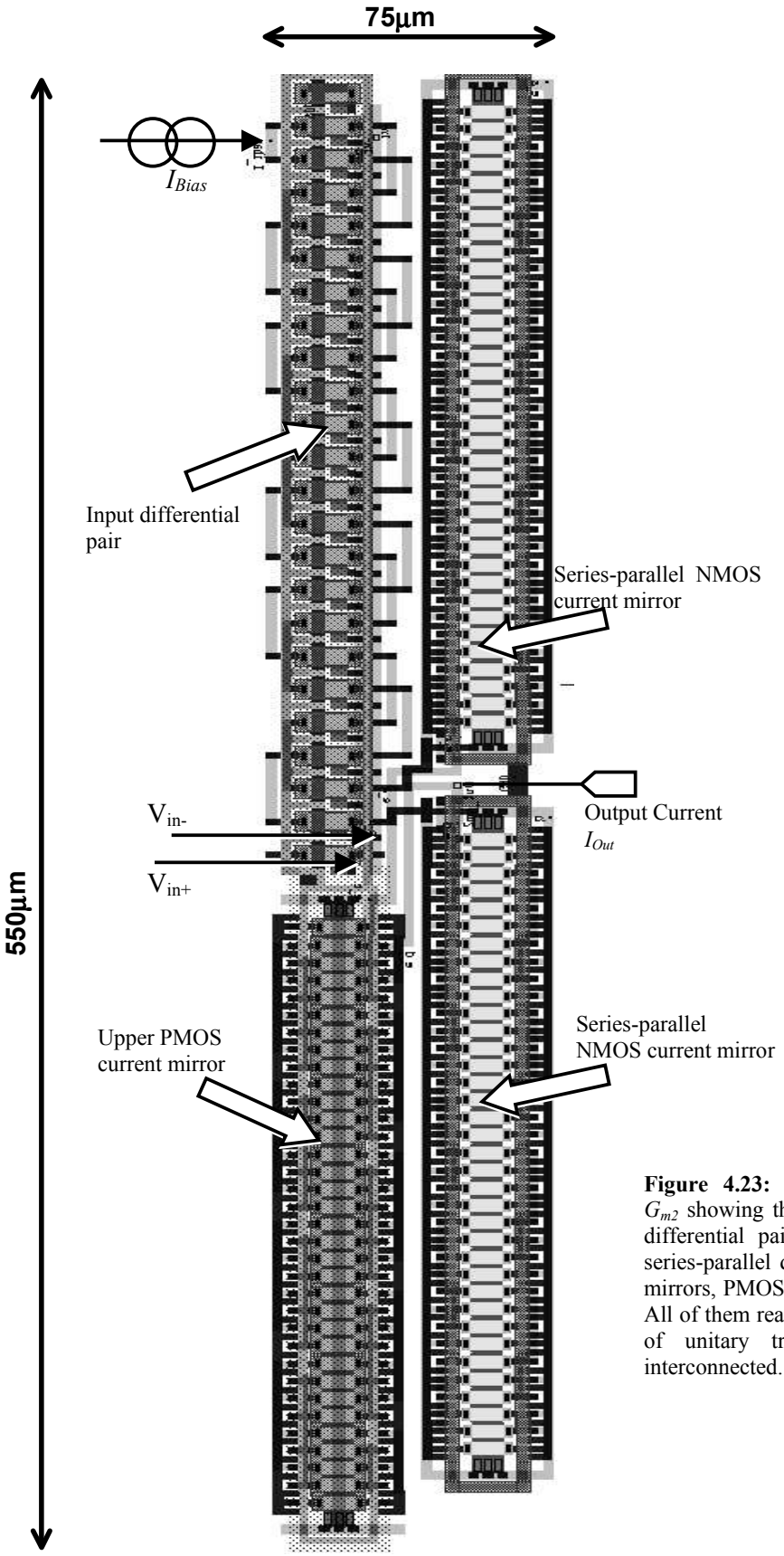

Figure 4.23: The layout of G_{m2} showing the PMOS input differential pair, two NMOS series-parallel division current mirrors, PMOS current mirror. All of them realized with rows of unitary transistors then interconnected.

This row structure has the following advantages:

- Minimum extra space is used since only two dummies are required to obtain the same surroundings for all unitary transistors.
- Layout blocks are easily re-usable since transistor rows can be employed in current mirrors with widely different copy factors, or in a differential pair whether linearized or not, just by changing metal wire connections.
- When matching transistor arrays, common centroid geometry is obtianed since the centroids of both matched arrays are very close to each other.[9]

4.7 - OFFSET MEASUREMENTS AND PERFORMANCE COMPARISON.

In Table 4.4 input offset measurements for 10 samples of each OTA (G_{m1} from section 3.5 is also included) on different chips from the same batch are shown. A reduced offset is observed in all cases with an average measured input offset - bottom row - below 10mV for all the OTAs. The table, shows an adequate degree of agreement between estimated and measured offset.

Chip #	G_{m1}	G_{m2}	G_{m3}	G_{m5}	G_{m6}
	Measured input offset [mV]				
1	0.87	0.48	-1	4.57	-3
2	-0.25	8.37	-2.3	5.43	-8
3	0.27	3.20	3	5.46	-11
4	-1.67	0.71	-1.5	8.82	6.5
5	-1.15	6.14	1.5	13.75	0
6	-2.53	1.93	-4	1.18	8
7	-0.81	-4.92	1.5	21.21	-11.5
8	-0.75	-4.81	0	0.41	4
9	-0.42	3.41	-2	-4.50	2
10	0.09	-2.95	-0.5	-2.71	3.5
$\overline{\sigma_{V_{off}}}$ [1]	1.7mV	8mV	5.4mV	8.8mV	9mV
$\overline{V_{off}}$ [2]	**1.1**mV	**4.4**mV	**2.1**mV	**9.1**mV	**6.8**mV

Table 4.4: Measured input referred offset voltage for 10 samples of the tested OTAs.

[1] Estimated - See annex D.

[2] Average measured input voltage calculated as: $\overline{V_{off}} = \sqrt{\frac{1}{10}\cdot\sum_{1}^{10} V_{off\_i}^2}$

[9] Even when matching two arrays with a very different aspect ratio. Only both must contain the same number of unitary transistors, regardless the way them are connected.

In Table 4.5 several measured and predicted characteristics of the fabricated OTAs are presented together. In comparison with several other implementations of very low transconductance OTAs [36-41,43,47-48], series-parallel current division shows a good compromise in terms of area and power consumption, while preserving an adequate linear range. Noise is preserved low, but more importantly, input referred offset is only a few millivolts. It should be remarked that reduced noise, offset, power consumption, and occupied area characteristics, are obtained, even for a few pS linearized transconductance OTA, which is below, as far as we know, that achieved by previous studies.

OTA	Transc. Simulated (Measured)	Linear range. V_{Lin} [mV]	Input noise.[μV_{rms}] Simulated - (Meas.)	Area [mm^2].
G_{m1}	110(110)nS	60	5 (4)	.019
G_{m2}	2.35(2.58)nS	150	42	.040
G_{m3}	35(33)pS	150	163(130)	.092
G_{m4}	21nS	150		.051
G_{m5}	2.4(2.8)nS	500		.18
G_{m6}	89(100)pS	500		

OTA	Power [nW] Simulated - Measured	Current Cons. [nA]	Input Offset. σ_{Voff} [mV]
G_{m1}	7.8	14	1.1
G_{m2}	123	43	4.4
G_{m3}	117	42	2.1
G_{m4}	134	47	
G_{m5}	123	44	9.1
G_{m6}			6.8

Table 4.5. Measured transconductance , linear range V_{Lin} (error α<5%), estimated (measured) input referred noise in the passband, total area, current consumption, and measured offset for the OTAs.

4.8 CONCLUSIONS.

Series-parallel association of transistors applied to the efficient area-mismatch-noise implementation of current mirrors with a wide range of copy factors was presented. A general expression was deduced, to estimate mismatch offset in series-parallel current mirrors. From both measurements and theoretical estimation, the technique was shown to be valuable in terms of mismatch offset reduction. Particularly, it was shown that extremely large current multiplication(division) factors could be obtained without a significant loss in terms of area, offset, or noise.

Series-parallel division of current in symmetrical OTAs was used to achieve low transconductances with extended linear range. This architecture has been studied in detail; the measured and predicted performance of the OTAs resulted in a very good trade-off in terms of occupied area, current consumption, linearity, noise, and mismatch offset. A design methodology for such a family of OTAs was presented as well as some designed, fabricated,

and measured examples. The tested OTAs range from 30pS -equivalent to a 30GΩ resistor- to 28nS, with linear range from ±150 to ±500mV, and an input referred offset of a few mV. These OTAs may help to implement very efficient G_m-C filters in the sub-Hz frequencies.

Chapter 5:

A Fully Integrated 0.5-7Hz, 40db/dec, CMOS Bandpass Amplifier.

This chapter presents the designing of the physical activity sensing circuit specified in chapter 1, which is part of a rate adaptive pacemaker. The system is composed of a piezoelectric accelerometer and its signal conditioning circuitry. The central block of the signal chain is a bandpass filter-amplifier, with a rectifier and time average also being required.

The detailed design, and test result, for a $G \cong 400$ gain, 0.5-7Hz bandpass amplifier is presented, while the design and simulation of a rectifier and 3-second time average are shown. The bandpass filter-amplifier is G_m-C continuous-time, which uses series-parallel current division OTAs to achieve the required large time constants and gain. The OTA blocks are those presented in chapter 3-4. The design methodology is emphasized so it can be easily extended to other ultra-low-power, very large time constant filters.

Firstly, the filter-amplifier topology and basic relations are discussed. The detailed design methodology is then presented. The filter has been fabricated in a standard 0.8µm minimum gate length CMOS technology, and tested. The main test results are shown including transfer function, and noise analysis. A discussion of possible fluctuations in the filter transfer function depending on variations of technology parameters is presented. This study is essential since the circuit is intended to be incorporated in an industry application without using a tuning scheme. Finally the design of the required rectifier, and 3-second averaging is shown, using several of the circuit blocks previously employed in the bandpass amplifier.

The bandpass filter topology is shown in Fig.5.1; it has two cascaded single-ended stages with a total gain of $G=385$: a preamplifier stage with a gain of $G_1=46.4$ formed by G_{m1}, G_{m2}, G_{m3}, C_1, C_2, and a gain stage with a gain of $G_2=8.4$ formed by G_{m4}, G_{m5}, G_{m6}, C_3, C_4. Each stage is composed of a lowpass gain structure (given by $G_{m1(4)}$, $G_{m2(5)}$, $C_{2(4)}$) similar to that proposed in [38] for a capacitive microphone, and a DC cancellation loop (given by $G_{m3(6)}$, $C_{1(3)}$). The external piezoelectric sensor is modeled as a capacitor with an input voltage in series[1]. Note in Fig.5.1 that the sensor capacitance itself is used in the filter, taking advantage of a 550pF-capacitor -much greater than common integrated capacitors-. The preamplifier DC cancellation loop also provides a virtual ground to the upper node of the accelerometer, eliminating in this way the need for any resistor connected to ground.

[1] Sensor specifications are detailed in Table 1.1 or datasheet [23]

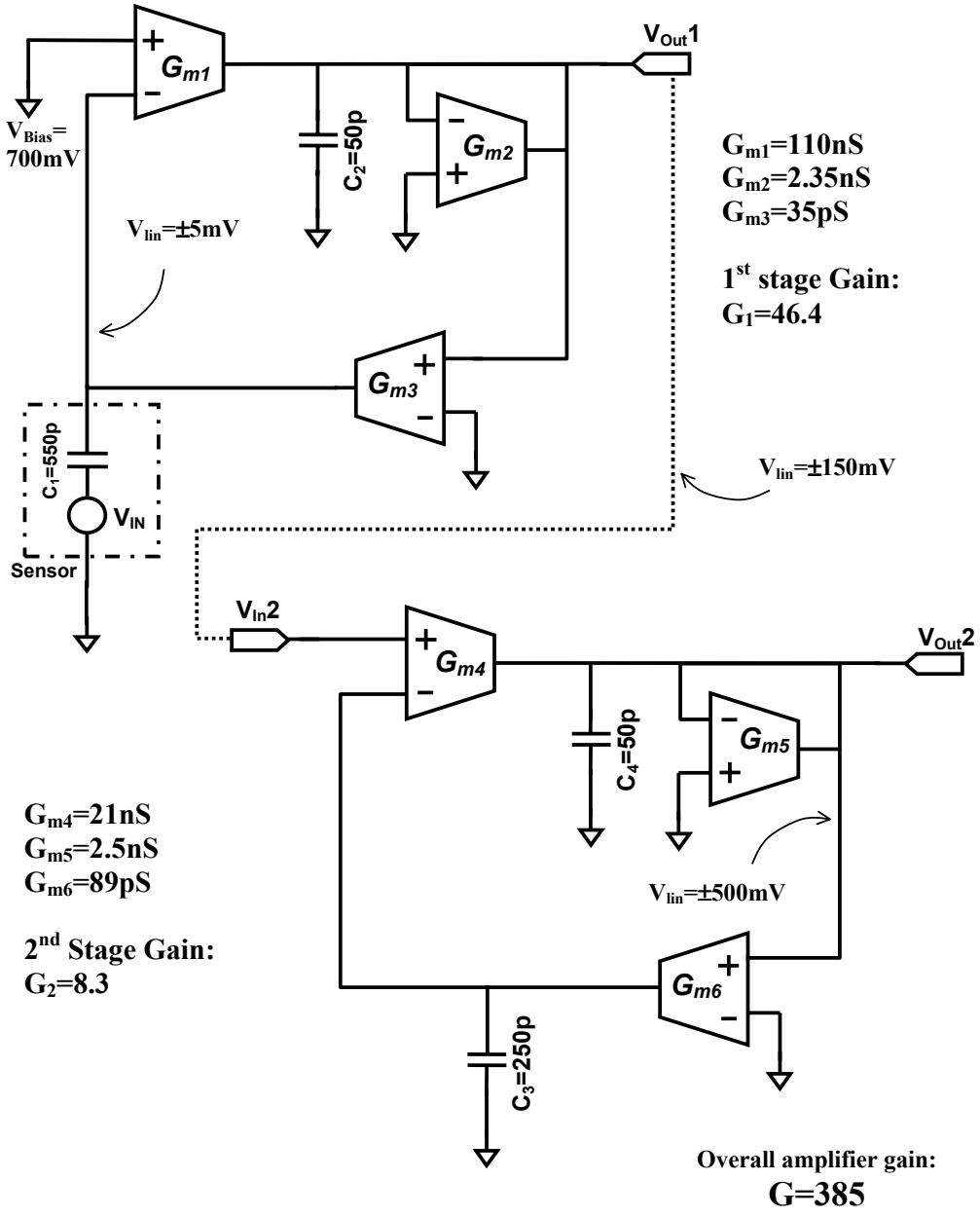

Figure 5.1: The topology of the designed 40dB/dec 0.5-7Hz G_m-C bandpass filter-amplifier. The value of the circuit elements and each stage gain are indicated. There are also indicated the required linear range for the OTAs connected on each node. Note that the sensor itself is incorporated as a part of the filter.

Detailed OTA design is shown in sections 3.5 and 4.4, while circuit schematics at transistor level are shown in annex E.

5.1 FILTER TOPOLOGY

In this section the filter topology is examined. Some issues are discussed such as the bias voltage value, the relationship between transconductances and capacitors in the obtention of the desired filter transfer function, capacitor sizing, and the gain of each stage.

5.1.1 Selecting the bias voltage V_{Bias}.

All the signals in the filter are referred to a bias voltage V_{Bias} that is, for test purpose, an external-ideal voltage source. The limits for V_{Bias} come from the dynamic range of the OTAs[2]. If V_{Bias} is too large, i.e. 900mV, then for a large input signal the OTAs will escape from their linear range (see section 4.5) seriously affecting the accuracy of the circuit. The effect will be particularly significant as the supply voltage approaches the minimum 2V value. On the other hand, an extremely low V_{Bias} i.e. 400mV will limit the large signal excursion. In accordance with the dynamic range of the OTAs, an appropriate range for V_{Bias} is between 600 to 700mV. Particularly, a 700mV V_{Bias} is assumed in the rest of this chapter and for the measurements. The filter-amplifier was tested to operate with such bias voltage and 2V power supply, without a qualitative significant performance degradation. However, since the dynamic range of the OTAs is strongly related to technology parameters -in particular the threshold voltage of transistors- it is not possible to extend the result of this test to future fabrication runs of the same circuit. In effect, even simulation with a typical threshold voltage V_{TP}=.8V for PMOS transistors shows a significant non-linearity in $G_{m5\text{-}6}$ OTAs with a 2V supply voltage while using 700mV V_{Bias}.

Although the issue should be discussed in the case of an industrial application, 700mV V_{Bias} seems to be the adequate value because:

- In a real pacemaker with regular medical supervision, the battery voltage rarely reaches 2Volts, and the whole pacemaker is replaced as soon as the battery approaches the end of its life. During most pacemaker lifetime the battery voltage is above 2.4 Volts [3] so it is unwise to optimize the design for 2V operation.
- Despite a performance degradation, when simulated with V_{TP}=1V, and 2V power supply voltage, the whole filter-amplifier was operative, giving a physical activity output signal. Simulations were performed for corner parameters (slow NMOS-PMOS transistors).

It should be noted that 700mV voltage source is required on-chip. In principle it does not seem difficult to derive 700mV voltage from traditional voltage references. But the question arises on how this voltage is generated and of course if this circuit's power consumption is much less than that of the bandpass filter itself. Also into a pacemaker there are required several voltage references so in the case of an industrila application, the voltage reference should be examined in a more general framework. Owing to these reasons the generation of bias voltage is not discussed in this work, but the issue requires a carefull analysis.

5.1.1 Analysis of a 2nd order G_m-C stage.

The architecture of each stage in the filter of Fig.5.1 corresponds to a low-pass amplifier in a feedback loop (Fig.5.2). Taking as an example the preamplifier stage, the lowpass transfer

[2] See section 4.5.

function is $A = \frac{A_0}{(1 + j\,\omega/\omega_L)}$, where A_0=G_{m1}/G_{m2} is the DC gain and $\omega_L = \frac{G_{m2}}{C_2}$ is the cutoff frequency. The feedback network is an ideal integrator: $\beta = \frac{k}{j\omega}$ with $k = \frac{G_{m3}}{C_1}$. The open loop A_{OL}, and closed loop A_{CL} of the system are:

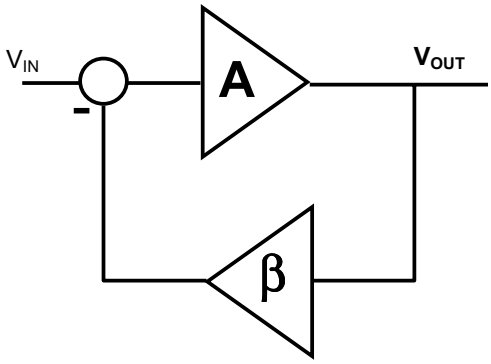

Figure 5.2: Scheme of the preamplifier feedback loop:

$$A = \frac{G_{m1}}{G_{m2}(1 + j\,\omega C_2/G_{m2})}, \quad \beta = \frac{G_{m3}}{j\omega C_1}$$

$$A_{OL} = A\beta = \frac{A_0 k}{j\omega(1 + j\omega/\omega_L)} \tag{5.1}$$

$$A_{CL} = \frac{A}{1 + A\beta} = \frac{j\omega A_0}{j\omega(1 + j\omega/\omega_L) + A_0 k} \tag{5.2}$$

The closed loop gain can be better expressed in the usual form of a second order stage [17] using center frequency ω_0 , and quality factor Q:

$$A_{CL} = \frac{Q\omega_0}{k} \cdot \frac{j\omega.\omega_0/Q}{\omega_0^2 + j\omega.\omega_0/Q - \omega^2} \tag{5.3}$$

with $\omega_0^2 = A_0 k.\omega_L$, $Q = \sqrt{\frac{A_0 k}{\omega_L}}$. In our case the positions of the poles must be $\omega_{p1} = 2\pi.(0.5Hz)$, $\omega_{p2} = 2\pi.(7Hz)$ so the values of ω_0, Q, and k, should be determined to obtain them. The roots of the polynom in the denominator of (5.3) are:

$$\omega_0^2 + j\omega.\omega_0/Q - \omega^2 \qquad \begin{cases} \omega_{p1} = -j\omega_0\left[\frac{1}{2Q} - \sqrt{\frac{1}{4Q^2} - 1}\right] \\ \omega_{p2} = -j\omega_0\left[\frac{1}{2Q} + \sqrt{\frac{1}{4Q^2} - 1}\right] \end{cases} \tag{5.4}$$

Adjusting them to their desired value yields:

$$Q \approx 0.25$$
$$\omega_0 \approx 11.8 \tag{5.5}$$

From (5.3), the gain at the center frequency of each stage is

$$G_1 = \frac{Q\omega_0}{k} \approx \frac{3C_1}{G_{m3}} \quad , \quad G_2 \approx \frac{3C_3}{G_{m6}} \tag{5.6}$$

From (5.5), and ω_0, Q definitions, the relations that must satisfy the elements of each stage are:

$$A_0 = \frac{g_{m1}}{g_{m2}} = \frac{g_{m4}}{g_{m5}} = 2.93 \tag{5.7a}$$

$$\omega_L = \frac{g_{m2}}{C_2} = \frac{g_{m5}}{C_4} = 47 \tag{5.7b}$$

where the factors

$$k = \frac{g_{m3}}{C_3},\ k' = \frac{g_{m3}}{C_3}, \tag{5.7c}$$

are related to the gain of each stage through (5.6). Finally, the center frequency, and Q of each stage are:

$$\omega_0 = \sqrt{\frac{G_{m1}G_{m3}}{C_1C_2}} = \sqrt{\frac{G_{m4}G_{m6}}{C_3C_4}}, \qquad Q = \sqrt{\frac{G_{m1}G_{m3}C_2}{G_{m2}^2C_1}} = \sqrt{\frac{G_{m4}G_{m6}C_4}{G_{m2}^2C_3}} \tag{5.8}$$

The system was simulated to be stable, with a 68º phase margin.

5.1.2 - Assigning of the gain for each stage.

To reduce the input referred noise to a minimum in a 2-stage amplifier, as much gain as possible should be assigned to the first stage. Then, according to (5.6), the transconductor G_{m3} should be as low as possible. The overall filter gain is the product of the gain of each stage. So, if most of the gain is assigned to the preamplifier, as a byproduct we can concentrate on the offset reduction in the second stage rather than on the gain.

5.1.3 - Area minimization and the selection of the capacitors.

In some works regarding integrated filters occupying a large silicon area, how to size capacitors and resistors (or transconductors) in order to minimize the joint occupied area (i.e. see ref [18]) is discussed. For example, one can investigate, provided there is a given time constant $\tau = C/G_m$, what is the optimum (G_m, C) pair in terms of area. We will show that a good and simple approach, is simply to assign as much area as possible for the capacitor. Let us start the analysis considering only transistor gate area. The transistor intrinsic cut-off frequency [20,50] is written:

$$f_T = \frac{g_m}{\pi C'_{ox}.W.L} \qquad \text{so} \qquad W.L = \frac{g_m}{\pi C'_{ox}.f_T} \tag{5.9}$$

where g_m is the transistor gate transconductance, and W,L, its width and length. Considering the time constant obtained with a single transistor and a double poly capacitor C, the total occupied silicon area is (assuming that the double poly capacitance per unit area $C'_{poly} \approx C'_{ox}$):

$$A_{Total} = \frac{C}{C'_{poly}} + \frac{g_m}{\pi C'_{ox} f_T} \approx \frac{C}{C'_{poly}}\left[1 + \frac{1}{\pi \tau f_T}\right] \tag{5.10}$$

However, the usual design criterion is that product $\tau.f_T$ must be much greater than one for the transistor to operated under normal conditions, avoiding non-quasistatic effects. If $\tau.f_T$ is close to one the transistor self-capacitance should be taken into account, and the circuit presents a distributed parameter problem[3]. Moreover, it is clear from Tables 4.1-4.3, and 4.5, that the total area of an OTA is several times greater that the transistor gate area, also an OTA contains several transistors, which increase optimization complexity.

Summarizing, an area optimization is a complex problem and will probably lead to transistor gate areas several times smaller than capacitors. We propose as a rule of thumb the assignment of as much area as possible to capacitors in order to make the transistor gate capacitance negligible in comparison to capacitors, in the design of very large time constants. In this way the filter transfer function is independent of the OTA design at transistor level thus allowing a simple filter design. Nonetheless, because the area of an OTA is several times greater than the sum of its transistor gate areas, the OTA will probably occupy a total area close to, or greater than, the capacitor area. This fact has been observed in the design of the current bandpass filter.

5.2 DESIGN METHODOLOGY.

In this section, a simple 4-step design methodology is presented for the bandpass filter amplifier. The methodology is based on the above-discussed issues, and can be easily adapted to other G_m-C filters. The design process is as follows:

1st. - Identify the critical circuit elements, and determine their value if possible. In the filter of Fig.5.1 these are:

- G_{m1} is the input transconductor and will determine the input referred noise. The efficient low-noise G_{m1}=110nS presented in section 3.5 is used at the preamplifier input.
- G_{m3} must be an extremely low transconductance OTA, as low as possible according to (5.6) to increase the preamplifiers gain G_1. Also, it should show a reduced offset because G_{m3}-C_1 forms the DC cancellation loop of the preamplifier. According to the discussion

[3] It will not be discussed if is possible to realize the circuit using $\tau.f_T$ close to one. Nonetheless design is clearly more complex, while the performance may be affected.

in section 4.3.2 regarding the minimum transconductance which can be obtained using series-parallel current division, a conservative 35pS value is chosen for G_{m3}. The gain G_1=46.4 is now fixed.

- G_{m6} closes the final DC cancellation loop so the offset at the output of the bandpass filter-amplifier is the input referred offset of G_{m6}. It is the most critical OTA because -in addition to low offset- it requires a wide linear range due to its ±500mV maximum input signal, and an extremely low transconductance to provide the required gain G_2≈8.5 of the output stage. According to (5.6) G_{m6}/C_3 ≈0.35.

2nd. - Assign as much area as possible to capacitors.

According to the discussion in section 5.1.3, capacitors should be as large as possible while respecting the total area budget. Particularly, a large capacitor C_3 will relax restrictions on G_{m6} regarding its low transconductance, so the design of this OTA can be better oriented to low offset and linearity. A 250pF C_3 capacitor was chosen, and 50pF capacitors are chosen for C_2 and C_4.

3rd. - Fix the value of the remaining elements, and estimate the required input linear range of each OTA.

At this point, all capacitors, and G_{m1}, G_{m3}, G_{m5}, are fixed. G_{m2}, G_{m4}, G_{m6}, are determined with equations (5.7a), (5.7b). Also, it is possible to estimate, the maximum signal amplitude on each node of the filter: at the output the required linear range is the overall gain G=400 multiplied by the maximum possible input signal of 1.2mV [4] which results in ±500mV; at the output of the preamplifier the required linear range is G_1 multiplied by the maximum possible input signal resulting in only ±60-70mV; at the input of G_{m1} the required linear range is only the maximum possible input plus the ±3.5mV offset due to gravity. Even though ±70mV are enough in theory, the required linear range has been increased to ±150mV at the output of the preamplifier stage because:

- a low transconductance such as G_{m3} may present a large offset of tens of mV [5] that should be added to the required linear range;
- the 1.2mV maximum input signal may be greater for a more sensitive accelerometer;
- it did not seem difficult to increase a bit the linear range of the OTAs connected to the output of the preamplifier.

Due to difficulties at circuit level, it was not possible to extend -based on the same considerations- the required linear range at the node V_{Out2} , which remained at ±500mV. In the circuit of Fig.5.1 the required linear ranges on each node of the bandpass-amplifier are indicated.

4th. - Based on their specified transconductance and linear range, design the OTAs at transistor level. Fine-tune the design to reuse the different layout blocks as much as possible.

Given the required transconductance and linear range for each OTA, it is easy to design them using the methodology of chapter 4. In fact, G_{m2} to G_{m6} design was presented in

[4] See Table 1.1

[5] Although it has been demonstrated in chapter 4 -from both theory and measurements- that the input referred offset of G_{m3} is constrained to a few mV, the design of the filter was prior planified.

section 4.4. A very important issue to highlight in order to minimize the design time and effort, is to place particular emphasis on the reuse of as many layout blocks as possible. The series-parallel current division technique allows us to do so, because widely different OTAs are obtained by using the same input differential pair and current mirrors, simply by changing their connection scheme. In our example, since their required linear range is the same, G_{m2}, G_{m3}, G_{m4}, use instances of the same input differential pair cell while the current division factor is 72:1 in the case of G_{m2}, 4900:1 in the case of G_{m3}, 8:1 in the case of G_{m4}. A further layout optimization is obtained for G_{m5}, G_{m6}, which share the same linearized differential pair, but use different output current mirrors. The circuit schematic of the combined OTAs is shown in annex E and the symbol in Fig.4.17 represents them. This structure is possible because the inputs of both OTAs are connected to V_{out2} and V_{Bias} in Fig.5.1. However, the sign of the input is the opposite on each OTA so the output mirrors are toggled to provide the adequate sign of the output current in each case. In the case of G_{m6}, G_{m5}, the output of a 70nS linearized pair was divided by means of series-parallel current mirrors, by 784 and 28 respectively. Of course this input stage sharing may have been applied also to $G_{m2,3}$ but in this case the benefit in area is not so great.

Finally, an extra simplification in the design follows if the bias currents of the OTAs are carefully selected so that all of them can be derived from the same reference. The required bias currents for G_{m1} to G_{m5-6} are 7nA, 42nA, 42nA, 42nA, 21nA, which are 1/3, 1, 1, 1, 1/2 of the reference bias current I_{Ref} = 42nA, respectively. The bias block, generating all the necessary bias currents from I_{Ref}, is also obtained using series-parallel current mirrors allowing this way a efficient scaled replication of I_{Ref} , in terms of area, and mismatch offset[6]. A schematic of the block is shown in annex E.

The resulting values for the circuit elements after the adjustment of the design, are shown in Fig.5.1. The comparative table 4.5 shows either measured or estimated transconductance, noise, offset, power consumption, and occupied area of each OTA. The measurements were obtained from isolated test transconductors. C_2, C_3, C_4, are double poly capacitors.

Finally, at the output of each stage (V_{Out1}, V_{Out2}), unity gain buffers are placed for test purposes to drive the integrated circuit output pads (see Fig.5.4). In order to make the buffers as transparent as possible for the filter, their input are CMOS gates, and they are independently powered.

5.3 MEASUREMENTS.

The above described bandpass filter-amplifier was fabricated in a standard 0.8µm CMOS technology, and tested. Fig.5.3 shows a microphotograph of the circuit obtaines using an optical microscope and a CCD camera. Fig.5.4 shows the expected and measured overall transfer function of the filter. The center frequency was measured at 1.8Hz. The simple circuit in Fig.5.5 was used to simulate the accelerometer output, using an external function generator because a calibrated movement generator was not available. The voltage divider

[6] See section 4.2.

R_A-R_B allows to comfortably simulate input voltages from a few µV to a few mV, using a standard function generator.

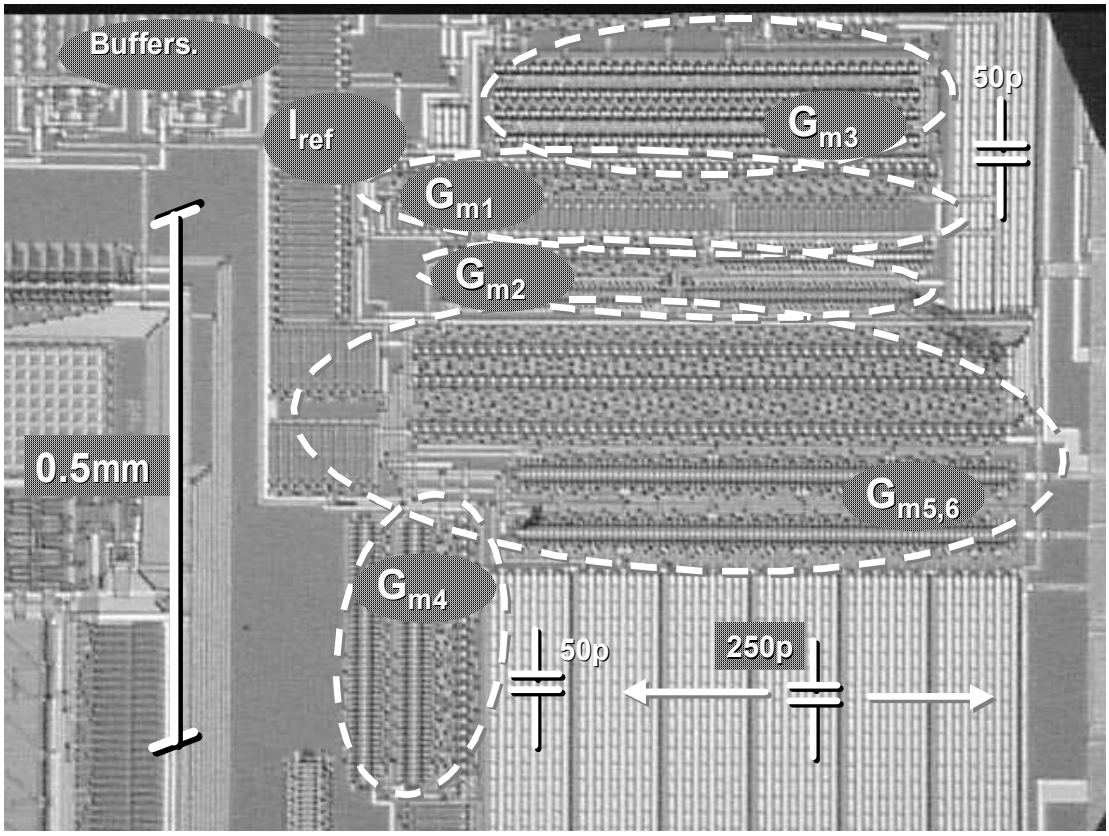

Figure 5.3: A microphotograph of the fabricated IC, indicating OTAs, capacitors, the position of the output buffers, and bias current generation circuit.

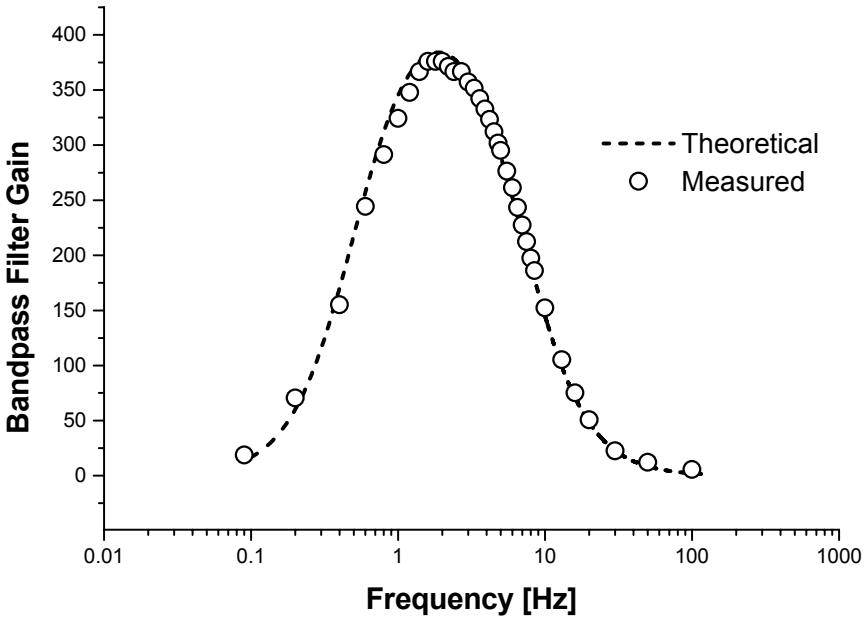

Figure 5.4: Estimated and measured total bandpass filter response.

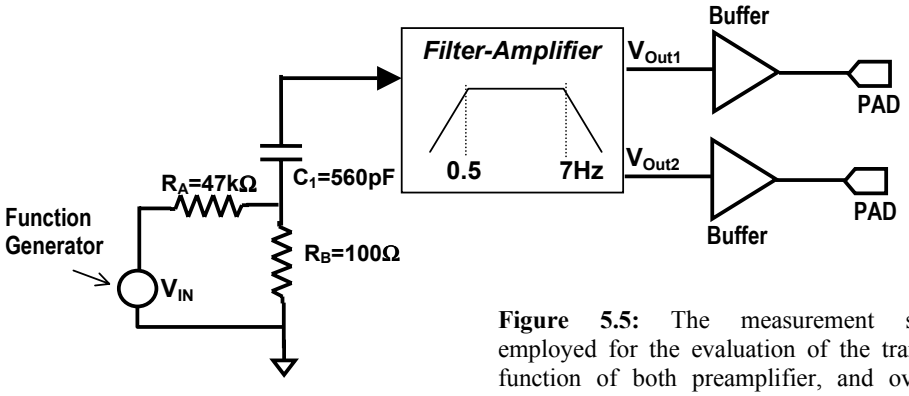

Figure 5.5: The measurement setup employed for the evaluation of the transfer function of both preamplifier, and overall filter transfer function.

In Fig.5.6 the transfer function of the preamplifier stage is shown. A high degree of agreement is observed in both plots between the measured and the expected transfer function. [7]

[7] An evaluation of the impact of technology parameters spread is examined in section 5.4.

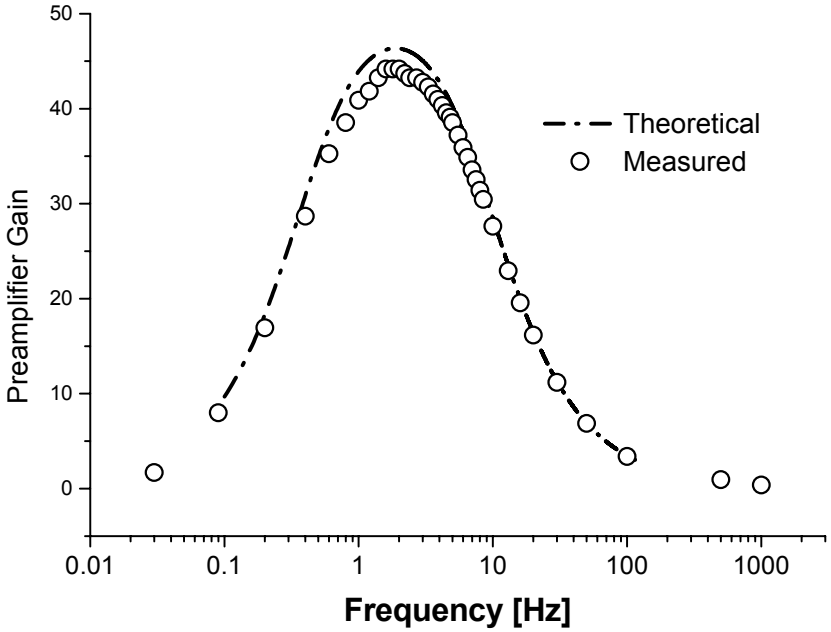

Figure 5.6: Estimated and measured preamplifier transfer function.

The measured total current consumption of the bandpass filter-amplifier was 229nA, in accordance to the estimated 233nA. 233nA result from the sum of the current consumption of each OTA on Table 4.5 plus additional 42nA from the external current reference. Noise measurements are shown and discussed in section 5.3.1 while offset characterization was not performed. The reason is that unfortunately, the output buffers are non offset-optimized. So the 6.8mV offset measurements for G_{m6} from Table 4.4, were taken as the bandpass offset estimation.

After the evaluation of the transfer function, the 12M1A piezoelectric accelerometer was connected to the circuit to carry out a qualitative -but very helpful from the application perspective- performance evaluation. In the plot of Fig.5.7 the time response of the bandpass filter-amplifier, while moving up and down the circuit board with the accelerometer is shown. It is important to remark that these measurements are very clean, demonstrating that coupling noise is not relevant despite the high impedance node of the sensor. The measurements in Figs.5.4, 5.6 and 5.7, were obtained with the circuit contained in a large open aluminum box, which is a noisier environment than a self-contained titanium casing as used in pacemakers. Although a model for coupling noise was not developed, an observation of the output of the filter under different conditions (inside-outside the aluminum box, and turning on-and-off different electrical equipment close to the circuit) allows us to conclude that the filter topology, with a 30GΩ equivalent OTA providing the DC bias for the sensor, is adequate for use in pacemakers.

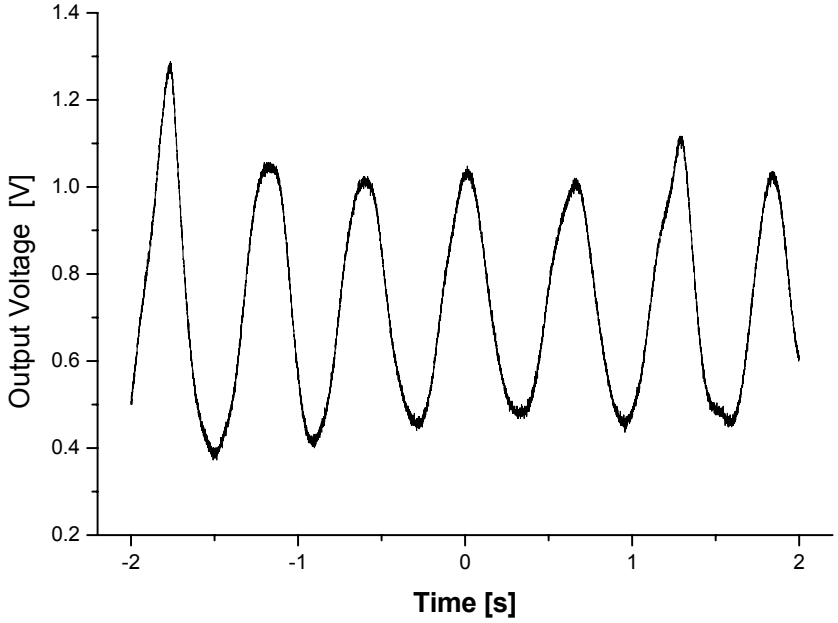

Figure 5.7: Time response of the physical activity sensing circuit (bandpass filter only) with the 12M1A piezoelectric accelerometer connected, while shaking the circuit board at aproximately 2Hz.

Finally, the accelerometer connected to the filter-amplifier, with the addition of an external full-wave rectifier and 15s time averaging[8], was mounted into a battery-powered closed container to do a field test of the activity sensing system. The idea is to carry the circuit, strapped at chest level, while doing different physical activities to check if it is capable of distinguishing between them. The output voltage was registered with the aid of a small pocket multimeter. The results are summarized in Table 5.1. The measurements seem adequate for the inclusion of the circuit in a high performance rate adaptive pacemaker.

Physical Activity	System Output
Sleeping	0 mV
Working on a Computer	30 mV
Walking (slow)	44 mV
Walking (normal)	86 mV
Walking (fast)	210 mV
Climbing up stairs	95 mV
Going down stairs	82 mV
Climbing up stairs (fast)	200 mV
Running (10km/h)	423 mV

Table 5.1: Output of the complete activity sensing circuit, under different physical activities and situations. The output reference is the output voltage of the system quiet on a table. This value is near 10mV higher than V_{Bias}.

[8] In comparison to the signal chain of Fig.1.1, the integration time was increased to comfortably measure the system output while doing different physical activities.

5.3.1 Noise analysis and measurements.

Because most gain was assigned to the input, the preamplifier stage is critical in terms of noise. The PSD of the input referred noise voltage in the preamplifier stage is:

$$S_{vn}(f) = \frac{S_{G_{m1}}(f) + S_{G_{m2}}(f)}{G_{m1}^2} + \frac{S_{G_{m3}}(f)}{(j\omega C_1)^2} \tag{5.11}$$

where $S_{G_{m1}}(f), S_{G_{m2}}(f), S_{G_{m3}}(f)$, are the noise current PSD of each OTA. Examining (5.11) it is possible to assume that noise is essentially determined by the input OTA G_{m1}. In Fig.5.8, the result of a noise analysis that represents the noise contribution at the preamplifier output of each G_{m1}, G_{m2}, G_{m3} is shown. As expected, in the passband from 0.5 to 7Hz, the noise introduced by G_{m1} dominates.

The relevant magnitude to register is the equivalent input noise voltage in the band of interest, considering the 2-stage amplifier. However, what is possible to measure is the output noise. The total input noise voltage can then be computed through dividing this value by the maximum gain in the bandpass. The measured output noise voltage was $0.82mV_{rms}$, which correspond to $2.1\mu V_{rms}$ equivalent input noise. This value seems too low. To check the result we estimated the equivalent input referred noise using the previously measured input noise voltage $S_{VG_{m1}}(f)$ of G_{m1} in section 3.5 (Fig.3.18). Assuming that the only noise source in our circuit is G_{m1}, the output noise is calculated using (see section D.1):

$$V_{out\_rms} = \sqrt{\int_0^{\infty} |H(f)|^2 . S_{VG_{m1}}(f) . df} \tag{5.12}$$

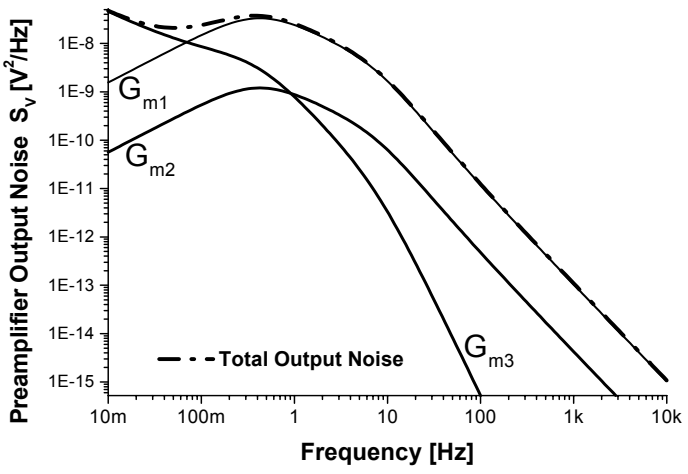

Figure 5.8: Estimated noise contribution of each OTA to the total output noise of the preamplifier stage.

where $H(f)$ is the second order bandpass-filter amplifier transfer function. The result is that one should expect a $1.3mV_{rms}$ at the output. Thus an equivalent noise voltage less that the expected value has been measured. There are several reasons that may explain the difference: an inadequate estimation of $S_{VG_{m1}}(f)$ and/or G_{m1} transconductance, a poor estimation of the N_{ot} parameter for flicker noise estimation.

5.4 DISPERSION ANALYSIS.

In spite of the fact that the application does not require fine tuning, and also that the integrated circuits measured in two different fabrication batches[9] were shown to have a transfer function very close to the specified one, it is necessary to estimate how much the spread in the technology parameters affect the transfer function of the bandpass-amplifier. The IC manufacturer specifies the capacitance per unit area of the poly1-poly2 capacitors we are employing in the filter, and the transconductance of a given typical transistor with certain tolerance. Fluctuations from the specified values in both cases may affect the center frequency, Gain, and Q of our filter. The gain may be software-corrected at the pacemaker microcontroller, while the center frequency and Q should not vary too much. From the datasheet of the target CMOS process, poly1-poly2 capacitance per unit area, is expected to spread ±8% around a 1.77fF/μm^2 typical value. On the other hand, an approximately ±25% spread was observed simulating the gate transconductance g_m of a single PMOS transistor in moderate inversion, using three different BSIM3v3 models provided by the manufacturer (typical, worst case slow, worst case fast). This spread was assumed for the transconductance of the OTAs.

Using (5.8), a worst case analysis concludes that the center frequency is between 1.4Hz, and 2.5Hz. But both transconductances and capacitors are correlated; for example if the thin oxide thickness increases, the poly1-poly2 capacitance per unit area decreases, as does the transconductance of a given transistor because its gate oxide thickness decreases. Although it will not be discussed, probably the boundaries for the center frequency have been over-estimated. However, prior to incorporating this motion estimation circuit into a pacemaker, it should be discussed with the manufacturer, whether this spread of the center frequency affects the case study from the application perspective.

If required, a possible mechanism to adjust the center frequency uses the bias current. Varying the 42nA typical I_{Ref} current - from which all the bias currents of the OTAs are derived - from 21nA to 63nA, the center frequency of the filter was measured as being displaced from 1.4Hz to 2.6Hz. If required, I_{Ref} can be adjusted with the aid of an external resistor, probably having the same value for all the integrated circuits fabricated in the same batch.

5.5 RECTIFIER AND 3s TIME AVERAGING.

In addition to the bandpass amplifier, it is necessary to design a rectifier block, and 3 seconds averaging to complete the required signal chain for the activity sensing circuit[10]. Although the problem has not been extensively studied, here we propose a solution using the same circuit blocks previously employed in the bandpass amplifier. A wide input range, 3-second average circuit can be simply obtained using G_{m6}, and a 260pF capacitor, as depicted

[9] For example, the measurements in [102] correspond to a different fabrication run than those presented in this chapter.

[10] See Fig.1.1 in chapter 1. Strictly the specification refers to the output of the circuit, as the average of the absolute value of the acceleration in the last 3 seconds.

in Fig.5.9(a). Also, if a 0.33Hz control signal $V_{control}$ is provided, a resettable integrator as in Fig.5.9(b) is obtained[11].

In Fig.5.10 the proposed rectifier/averaging scheme is shown. It is composed of a modified G_{m6} transconductor, which incorporates a second output branch toggling the connections of the mirrors so the output current at both output branches have the same modulus but opposite sign. A comparator with the aid of two MOS switches, selects which of the outputs will be the effective output of the transconductor. Thus, the modified OTA, comparator, and switches act as a voltage to current rectifier providing an output $I_{out} = |G_m . V_{in}|$, this rectifying OTA will be referred to as G_{mR}. In the plot of Fig.5.11, the simulated transfer function -output current vs. input voltage- of the circuit is shown. This plot is clearly associated to a rectifier. The comparator used for the simulation is simply G_{m1} with the addition of 2 cascaded inverters at the output. This OTA was chosen due to its low noise, offset, and power consumption. Finally, if the output of the rectifier is connected to an integrating capacitor C_{int}, a magnitude proportional to the average of the absolute value of the input signal is obtained. In the simulation of Fig.5.12, the output of the integrator is shown, for a 400mV amplitude, 5Hz-frequency sine wave input signal. If a discharge switch is shunted with C_{int} and closed every 3 seconds, the scheme of Fig.5.9(b) is obtained. The integrating capacitor may be reduced to increase the output swing of the integrator. The scheme of Fig.5.9(a) cannot be realized with G_{mR} because its negative input is no longer connected to V_{Bias}. Instead, a scheme like the one in Fig.1.6 may be employed to realize a rectifier + 0.33Hz lowpass filter. In this case G_{mR} substitutes G_{m1} on Fig.1.6. But this circuit is a less area efficient solution than the resettable integrator because it incorporates a second highly linear, very low transconductance OTA.

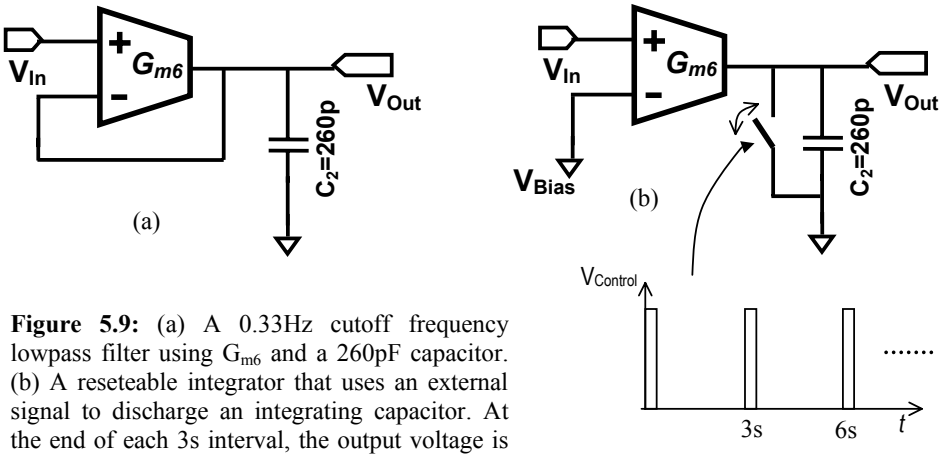

Figure 5.9: (a) A 0.33Hz cutoff frequency lowpass filter using G_{m6} and a 260pF capacitor. (b) A reseteable integrator that uses an external signal to discharge an integrating capacitor. At the end of each 3s interval, the output voltage is $V_{Out} = \frac{G_{m6}}{C_{\text{int}}} \int_{t-3s}^{t} V_{in}.dt$.

[11] Note: a circuit performing the integration $V_{out} = \int_{t}^{t+3s} V_{in}(t).dt$ can not be realized with lumped elements but a low pass filter with a cutoff frequency a 0.33Hz is a good approximation [109]. To provide the exact V_{in} integration in the last 3 seconds, a control signal should provide an integration-start and integration-end indication. After integration-end, the output is read and the integrating capacitor may be discharged waitng for the start of next integration cycle.

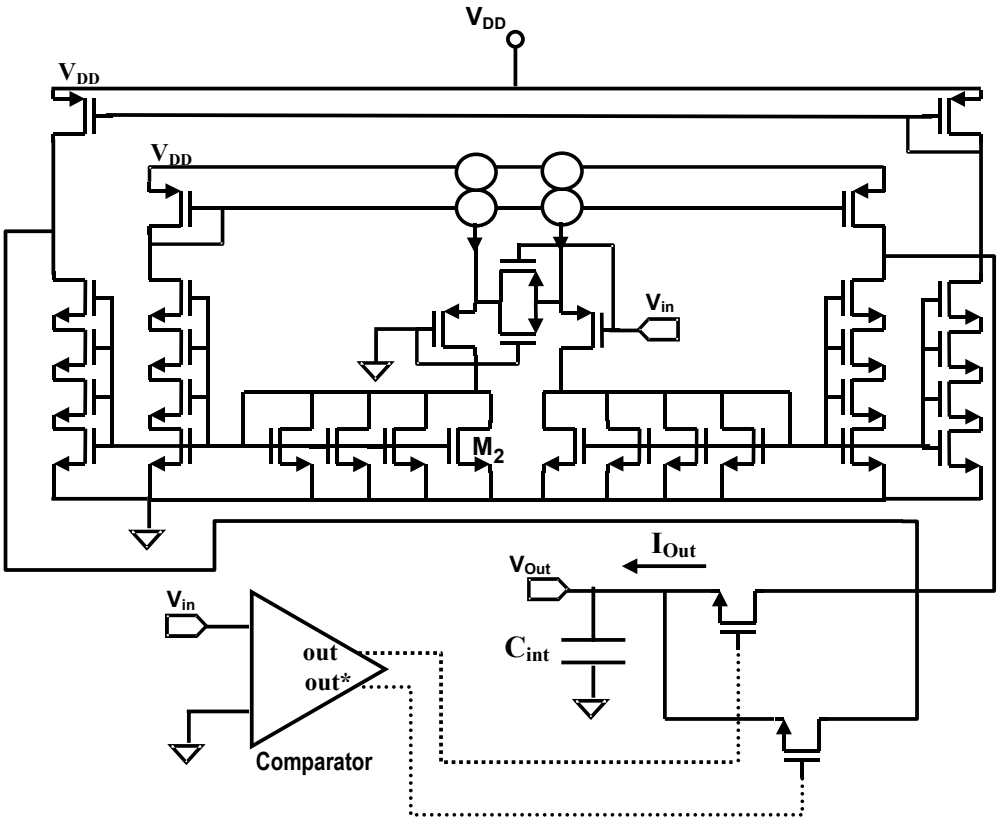

Figure 5.10: The proposed scheme for a rectifier-tranconductor connected to an integrating capacitor. It is based on a series-parallel OTA similar to G_{m6} with dual output of equal modulus but different sign. A comparator depending on the sign of the input determines which of the two output currents charges the capacitor. The output current of the rectifying OTA is $I_{out} = |G_m . V_{in}|$.

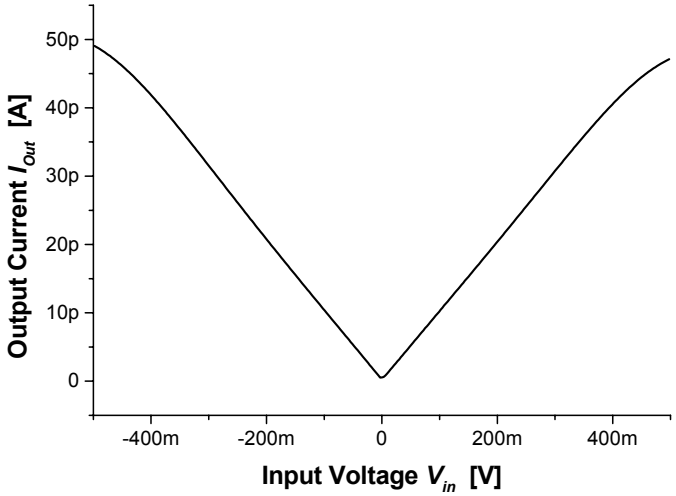

Figure 5.11: Simulated transference of the rectifiyng OTA $G_{mR.}$

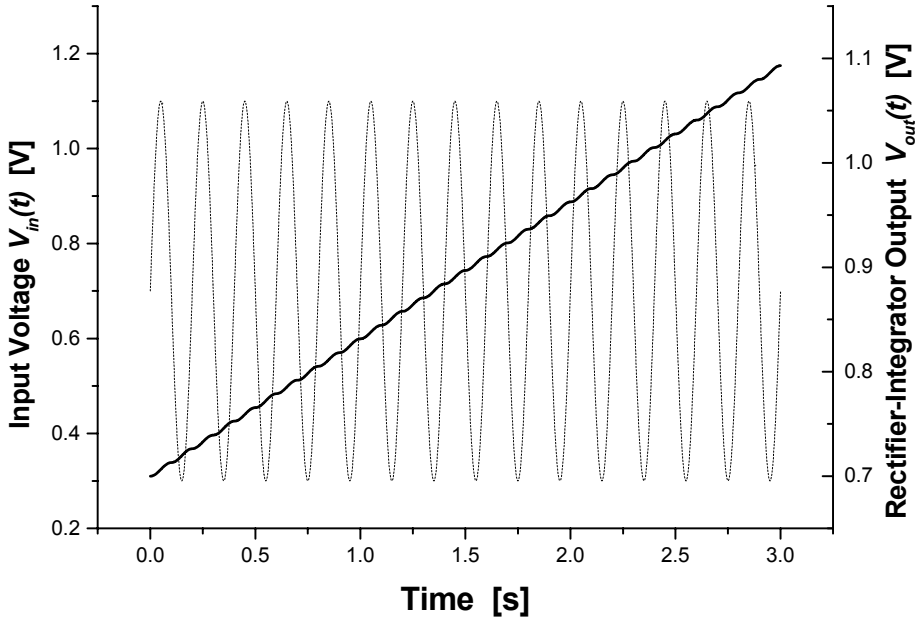

Figure 5.12: Simulated output in a 3s period, of the rectifier-time-average of Fig.5.10, when applying a $400mV_{pp}$ input signal. Bias voltage V_{Bias} is 700mV, and the integrating capacitor is assumed to be discharged at the beginning. A 200pF C_{int} was used, the rectifying OTA is the previously described G_{mR} OTA, while the comparator is G_{m1}. The expected $V_{out} = V_{Bias} + \frac{G_{mR}}{C_{\text{int}}} \int_0^3 |V_{in}| dt$ is observed at the end of the 3s period.

5.6 CONCLUSIONS.

The complete design methodology for a fully integrated G_m-C, 0.5-7Hz, CMOS bandpass filter-amplifier has been presented. Large time constants were obtained using series-parallel division of current in symmetrical OTAs to achieve low transconductances with an extended linear range. The measured and predicted performance of the filter resulted in a very good solution in terms of current consumption, noise, offset, and occupied area. The design methodology for this filter can be easily extended to other micropower filters with low cutoff frequencies, often found in implantable medical electronics.

The filter was fabricated and tested. In Table 5.2 several estimated and measured characteristics for the filter are shown . Its low input referred noise, and power consumption should be highlighted. In addition, the complete accelerometer-based activity sensing system was tested while realizing different physical activities, and in different environments, showing that it is suitable for incorporation in modern rate adaptive pacemakers.

A key aspect of the described family of G_m-C filters is the ability to re-use previously drawn layout blocks, which allows a fast, and accurate design. By simply changing series-parallel division factors and connections, widely different OTAs can be obtained. For example, a rectifier and 3-second time averaging stage, to complete the required signal processing for the activity sensing circuit described in chapter 1, was designed using some of the circuit

blocks employed in the bandpass filter. Rectifier and time average stages consume only 70nA, and occupy an area of 0.4 mm^2. A comparative analysis of the complete physical activity sensing circuit and other circuits with close specifications is discussed below.

0.5-7Hz Bandpass filter amplifier data

Specification	Value
Bandpass Frequency	2nd order 0.5-7Hz
Gain	390[a]
Input noise	2.1μV_{rms}[a]
Operating Voltage	2.0 - 2.8 V
Current Consumption	230nA[b]
Occupied Area	0.78mm^2
Input referred Offset	18μV[c]

[a] measured
[b] measured/estimated
[c] estimated according to measured G_{m6} offset.

Table 5.2: Bandpass filter-amplifier characteristics.

5.6.1 Performance comparison.

In Tables 5.3 to 5.7 the main characteristics of several micro-power filters are summarized. The first table relates to the activity sensing circuit here presented, including bandpass amplifier, and rectifier-time average stage. Table 5.4 presents data from the first design of an activity sensing circuit [10] using continuous-time techniques but requiring a large number of external components. Table 5.5 contains the information relatated to a switched-capacitor filter, rectifier, and time averaging used for the same specified system but using a piezoresistive accelerometer [30]. The three circuits were designed at the GME as different approaches to the same problem. The G_m-C filter using series-parallel current division demonstrated a considerable reduction in power consumption and input noise in comparison to previous implementations of the circuit. It also uses no external elements, and the occupied area has been reduced but the circuits in Tables 5.4,5.5 were fabricated in a 2.4μm technology.

Tables 5.6, 5.7 contain information about two filters - which are intended to form part of biomedical devices - and have a set of specifications close to those of the physical activity sensing circuit. The first is a 2.4Hz low pass filter, presented by Solis Bustos et al [43] using combined continuous-time techniques. The circuit is compact in area while implementing a high order transfer function with a 60-dB dynamic range performance. This filter requires more power consumption and input noise is higher in comparison to the filter in Table 5.3. The reason for this is probably the use of capacitor scaling, and partial current cancellation OTAs. The data in Table 5.7 correspond to a low-power front end for a pacemaker atrial sensing channel presented by L.Lentola et al [27]. It is a bandpass filter-amplifier centered at 110Hz, with several special characteristics. The circuit combines a continuous-time preamplifier-antialiasing stage at the input, followed by a 3rd order switched capacitor stage.

4 external components are used in the filter[12] which also takes advantage of high resistivity poly layers to implement MΩs resistors in the preamplifier. The resulting circuit is very compact in area, with a very low power consumption and an extremely low input referred noise if we take into account that the bandpass of this filter is approximately 9 times that of the filter in table 5.2. This further noise reduction is possible in this case due to the reduced flicker noise at the much higher frequency bandpass.

An overall conclusion is that the system here presented improves the performance of the previously designed activity sensing circuits in the GME [10,30]. Its performance is also comparable to other high-end modern filters with close specifications [27,43]. The main advantage of G_m-C filters is that they are extremely simple allowing a reduced power consumption and noise. Finally, series-parallel OTAs also allow the implementation of G_m-C filters with a reduced mismatch offset. However, there are not enough elements to include offset in this final comparative analysis.

Circuit Description.	Technique	Discrete Components	Input Noise	Gain	Current Consumption	Supply Voltage	Area [mm²]
0.5-7Hz 2nd.order bandpass + rectifier + time averaging.	G_m-C using series-parallel current division OTAs	no	2-4μV_{rms}	400	300nA	2-2.8V	1.2

Table 5.3 Characteristics of the circuit fabricated in this study, in a standard 0.8μm CMOS technology, for the signal conditioning of a piezoelectric accelerometer.

Circuit Description.	Technique	Discrete Components	Input Noise	Gain	Current Consumption	Supply Voltage	Area [mm²]
0.5-7Hz 1st order bandpass + rectifier + time averaging.	Continuous-time filter using combined techniques	10	18μV_{rms}	2900	3μA[a]	2-2.8V	1.82

Table 5.4 Characteristics of the circuit fabricated for the first pacemaker ASIC prototype, in a standard 2.4μm CMOS technology, for the signal conditioning of a piezoresistive accelerometer [10].
[a] 500nA transducer consumption

Circuit Description.	Technique	Discrete Components	Input Noise	Gain	Current Consumption	Supply Voltage	Area [mm²]
0.5-7Hz 1st order bandpass + rectifier	Switched Capacitors	2 for time averaging	n.a.	510	2.8μA[b]	2-2.8V	9

Table 5.5 Characteristics of the circuit fabricated using switched capacitors, in a standard 2.4μm CMOS technology, for the signal conditioning of a piezoresistive accelerometer [30].
[b] 2μA transducer consumption

[12] But the use of at least 2 external components is mandatory in atrial sensing channel for safety purposes.

Circuit Description.	Technique	Discrete Components	Input Noise	Gain	Current Consumption	Supply Voltage	Area [mm^2]
Sixth order, 2.4Hz lowpass filter.	G_m-C using special OTAs and scaled capacitors.	no	<50μV_{rms}	0.3	3.3μA	3V	1

Table 5.6 Characteristics of the lowpass filter presented in [43] for biological applications, fabricated in a standard 0.8μm CMOS technology.

Circuit Description.	Technique	Discrete Components	Input Noise	Gain	Current Consumption	Supply Voltage	Area [mm^2]
3rd. Order bandpass filter around 110Hz	Switched Capacitors & Continuous-time preamp.	4	6.9μV_{rms}	50-750	1μA	2-2.8V	1.9

Table 5.7 Characteristics of the pacemaker atrial sensing channel presented in [27] for biological applications, fabricated in a 0.8μm CMOS - with high resistivity poly layer option - technology.

Chapter 6:

Conclusions, Contributions, and Future Research.

This thesis has dealt with techniques aimed at the design of efficient very low frequency G_m-C integrated filters in CMOS technology. Attention was focused on a micropower, low-noise circuit for the signal conditioning of a piezoelectric accelerometer for application in rate adaptive pacemakers. The case study was shown to be a very challenging application for the designer, an interesting case from both the academic and industrial point of views.

At the beginning, a comparison between several circuit alternatives for very low frequency filters able to be incorporated in biomedical implantable devices was presented. Advantages and limitations of several techniques have been identified. Series-parallel current division applied to standard symmetrical OTAs was then employed as the key technique for the integration of large time constants while preserving a reduced noise, offset, area, and power consumption. Finally, the specified signal conditioning circuit, a 0.5-7Hz bandpass amplifier, with a G=390 gain was designed, fabricated, and tested. The circuit occupies $0.8mm^2$ in a standard 0.8µm CMOS technology, shows only $2.1\mu V_{rms}$ input referred noise, 6.9mV output referred offset, and consumes only 270nA with a 2-2.8V power supply voltage. The performance of this circuit has improved on that of previous implementations of the same system [10][30]. In particular, no discrete elements are required.

The technique of using series-parallel current division in OTAs allowed the implementation of efficient G_m-C filters offering a very good trade-off solution concerning offset, noise, power consumption, and occupied area. But also the design methodology is simple, and in particular a easy reutilization of layout blocks is possible. Consequently, the development of circuits is fast and efficient. However, in using this technique it is necessary to deal in some cases, with a large amount of series-stacked transistors biased with a few pico-Amperes, which is not a common situation in analog circuit design. Due to this special condition, a research study was required on transistor modeling and design at transistor and circuit levels. Two aspects were central in this thesis:

- The study, selection, and development of adequate models representing flicker noise, and mismatch offset in MOS transistors.
- The development of design methodologies for OTAs, and G_m-C filters, to be easily extended to other circuits in the same range of applications.

Particular emphasis was placed not only on developing accurate expressions, but also on simplifications in order to conciliate them with the simplicity required for design. We hope that the design methodologies, and design experience, as well as the transistor models here

presented may constitute a valuable contribution to the scientific community, and a useful set of tools for the integrated circuit analog designer.

6.1 MAIN CONTRIBUTIONS

The case study presented several challenges, at transistor model level, at transistor level design, and at circuit level design. A research study was required at all three levels.

Concerning transistor modeling, the main contributions are:

- Series-parallel association consistency of noise models was defined.
- Comparison of several noise models for analog circuit design, particularly from the series-parallel association perspective, was presented.
- A new simple, consistent, one-equation–all-regions physics-based model for the flicker noise in long channel MOS transistors was formulated.
- Flicker and thermal noise, which validate the new model and allowed technology characterization, were measured.
- A new simple, consistent, one-equation –all-regions model for mismatch in long channel MOS transistors was formulated. The correlation owing to their analogous origin, between flicker noise and mismatch offset, was shown.

Concerning transistor level design, the main contributions are:

- Evaluation of the offset impact in non-unitary current mirrors using series-parallel association of transistors. Demonstration, from both theory and measurements, that mismatch offset is reduced when this technique is applied to current mirrors with a large copy factor.
- Derivation of a simple expression for the linear range of a MOS differential pair in terms of the inversion coefficient.

At circuit level, the main contributions are:

- Extremely low transconductance OTAs with extended linear range using series-parallel current division were designed. The design and test of OTAs up to 33pS, equivalent to 30GΩ resistors, and up to ±500mV linear range, was shown, and a design methodology for this family of transconductors was presented.
- Series-parallel current division OTAs, even with extremely low transconductance, were demonstrated to show a low input offset.
- A 0.5-7Hz, G≅400 gain bandpass filter amplifier, with low input referred noise and offset, consuming only 300nA current was designed, fabricated, and tested. A design methodology was also established.
- The possibility to bias a piezoelectric accelerometer with a transconductance equivalent to a 30GΩ resistor was demonstrated.
- A time-average and rectifier based on G_m-C cells used in the bandpass filter were designed. Consequently, the benefits in terms of reutilization of the design technique previously presented were proved.

6.2 FUTURE RESEARCH PROSPECTS.

Most of this study deals with the application of series-parallel association of transistors to analog circuit design, and its related design tools, methodologies, and models. Due to the good results obtained in the activity sensing circuit, it would be worthwhile to extend the technique and design methodology to other circuits. A first option would be cardiac sensing channels -also required in pacemakers-, which are 100Hz centered bandpass filter-amplifiers.

Series-parallel association of transistors has been shown to be an extremely powerful technique, applicable not only to OTAs, but also, for example to current sources Although the benefits of series-parallel association of transistors in current mirrors have been demonstrated here, designers do not often use such architecture probably due to the lack of adequate models representing series transistor association behavior. The extension of this technique to different situations could be subject for future studies.

In the field of flicker noise, it is still necessary to compliment measurements. Flicker noise measurements under various bias conditions are difficult, and time demanding, so the set of measurements presented here -although consistent- is still limited, particularly for the characterization of PMOS transistors in the target technology. The group of measurements should be extended to short channel transistors, and also to situations like elevated source-to-drain voltages. The new flicker noise model does not take into account small geometry effects in its present form. We opted to preserve its simplicity, thus allowing the model to accurately predict, with a single parameter to adjust, noise in long channel transistors, common in analog design.

Finally, it should be stated that the design methodologies of this study are based on the ACM transistor model, which easily allows the representation of several transistor parameters in terms of the inversion coefficient. An exploration of the design space then becomes simple. Based on our experience there are several future research prospects. First, to incorporate the ACM model in the design methodology of other families of circuits. Second, to integrate all the algorithms here developed, in a single computer aided tool for the design of G_m-C filters. This tool may receive as an input the desired transfer function specifications, it may have a bank of available layout blocks, and would automatically synthesize a desired filter. In addition, it should be pointed out that series-parallel association of transistor seems particularly suitable for an automatic layout generation tool; but the implementation and optimization of such algorithms in a computer would constitute a different research study.

6.3 PUBLICATIONS.

Some of the results presented in this study, have been considered of enough interest to communicate them to the scientific community in the field of microelectronics. At present, the list of published/accepted papers is:

Journal Papers:

- Arnaud and C. Galup-Montoro, "A compact model for flicker noise in MOS transistors for analog circuit design", *IEEE Trans. Electron Devices*, vol. 50, no.8, pp. 1815-1818, August 2003.
- A.Arnaud, C.Galup-Montoro, "Pico-A/V range CMOS transconductors using series-parallel current division", *Electronics Letters*, v. 39, n. 18, p.1295-12, September 2003.

Conferences:

- Arnaud and C. Galup-Montoro, "*A fully integrated 0.5 -7 hz cmos bandpass amplifier*", - Accepted for pub.- IEEE Int.Symp. on Circuits and Systems (ISCAS - 2004) Vancouver-Canada.
- R.Fiorelli, A.Arnaud, C.Galup-Montoro, "*Series-parallel association of transistors for the reduction of random offset in non-unity gain current mirrors*" - Accepted for pub.- IEEE Int.Symp. on Circuits and Systems (ISCAS - 2004) Vancouver-Canada.
- H. Klimach, A. Arnaud, M. C. Schneider, C. Galup-Montoro*, "Consistent model for drain current mismatch in mosfets using the carrier number fluctuation theory*", - Accepted for pub.- IEEE Int.Symp. on Circuits and Systems (ISCAS - 2004) Vancouver-Canada.
- C.Galup-Montoro, M. C. Schneider, A. Arnaud and H. Klimach, "*Self-consistent dc, ac, noise and mismatch models of the mosfet*" Invited paper, 2004 Workshop on Compact Modeling, Boston - March 2004.
- A.Arnaud, C.Galup-Montoro, "*Simple noise formulas for MOS analog design*", IEEE Int.Symp. on Circuits and Systems (ISCAS), vol.1, pp.189-192, May 2003.
- P.Aguirre, A.Arnaud, "*Diseño de un filtro pasabandas para amplificador chopper para bajo ruido y micro-consumo*", Proc.VIII Workshop Iberchip - Guadalajara, México – March 2002. ISBN 970-93260-0-7.
- Arnaud, Carlos Galup-Montoro,*"Simple, continuous and consistent physics based model for flicker noise in MOS transistors"*, Proc.VIII Workshop Iberchip - Guadalajara, México – March 2002. ISBN 970-93260-0-7

The following papers have been submitted and are in revision process:

- A.Arnaud, C.Galup-Montoro, "*Consistent Noise Models for Analysis and Design of CMOS Circuits*" submited to IEEE Trans.on Circuits and Systems I.

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Annex A:

Derivatives of the Function $f(i_0)$

The derivatives of the function $f(i_0)$ used in the estimation of the linear range in a differential pair are:

$$f(i_o) = n\phi_t \left[\sqrt{1+\frac{i_b+i_o}{2}} - \sqrt{1+\frac{i_b-i_o}{2}} + Ln\left(\sqrt{1+\frac{i_b+i_o}{2}} - 1 \right) - Ln\left(\sqrt{1+\frac{i_b-i_o}{2}} - 1 \right) \right] \quad \text{(A.1)}$$

$$f'(i_o) = \frac{n\phi_t}{4} \left[\frac{1}{\left(\sqrt{1+\frac{i_b+i_o}{2}} - 1 \right)} + \frac{1}{\left(\sqrt{1+\frac{i_b-i_o}{2}} - 1 \right)} \right] \quad \text{(A.2)}$$

$$f''(i_o) = \frac{-n\phi_t}{16} \left[\frac{1}{\sqrt{1+\frac{i_b+i_o}{2}} \cdot \left(\sqrt{1+\frac{i_b+i_o}{2}} - 1 \right)^2} - \frac{1}{\sqrt{1+\frac{i_b-i_o}{2}} \cdot \left(\sqrt{1+\frac{i_b-i_o}{2}} - 1 \right)^2} \right] \quad \text{(A.3)}$$

$$f'''(i_o) = \frac{n\phi_t}{64} \left[\frac{3 \cdot \sqrt{1+\frac{i_b+i_o}{2}} - 1}{\left(\sqrt{1+\frac{i_b+i_o}{2}} \cdot \left(\sqrt{1+\frac{i_b+i_o}{2}} - 1 \right) \right)^3} - \frac{3 \cdot \sqrt{1+\frac{i_b-i_o}{2}} - 1}{\left(\sqrt{1+\frac{i_b-i_o}{2}} \cdot \left(\sqrt{1+\frac{i_b-i_o}{2}} - 1 \right) \right)^3} \right] \quad \text{(A.4)}$$

Annex B:

The Trapping-Detrapping Mechanism of MOS Channel Carriers by Localized States (Traps) Inside the Oxide, in the Perpective of Flicker Noise.

- **Physical Related Parameters.**
- **Deduction of the PSD of the process.**

It is well accepted that the sources of low frequency noise in MOSFETs are mainly carrier number and mobility fluctuations due to random trapping – detrapping of carriers in energy states inside the oxide, near the surface of the semiconductor. In this annex this mechanism will be examined in detail. To begin, let us consider a MOS transistor, and a small channel element of differential area ΔA as in Fig.B.1(a-b). Defects at the surface and inside the oxide generate localized states known as traps, that may be occupied by carriers from the channel. Electrons (holes) in the channel may tunnel to, and back from, these traps in a random process thus generating a noise current. Consider also a small volume ΔV inside the oxide as in Fig.B.1(c): $\Delta V = W.\Delta x.\Delta z$.

The following notation is introduced:

- N' [m^{-2}], Q_I' [C/m^{-2}], will denote respectively, the carrier number density, and channel charge density, in the channel element ΔA ($Q_I' = q.N'$).
- N'_A [m^{-2}] will denote the number of occupied traps per unit area in the whole oxide volume above the channel element ΔA. The relation between N' and N'_A is given by the r coefficient of eq.(3.12).
- E_t is the energy level at wich the trap is located.
- N_t [$eV^{-1}.m^{-3}$] is the number of traps per unit volume inside ΔV (at a distance z from the oxide surface), and for a small energy interval $E \le E_t \le E + \Delta E$
- N_V' [$eV^{-}1.m^{-3}$] is the volume density of occupied traps inside ΔV, and for a small energy interval $E \le E_t \le E + \Delta E$
- f_t is the probability for a single trap to be occupied. Using the Fermi-Dirac distribution: $f_t(E = E_t) = \dfrac{1}{1 + e^{\frac{E_t - E_F}{k_B T}}}$, E_F is the Fermi level of the system.

As discussed in chapter 3, once the PSD $S_{\delta N'}(f)$ of the time variations in N' is obtained, it is possible to calculate the flicker noise current of the transistor with an adequate integration procedure. Prior to this, there is a step to find, with physical arguments as will be shown in section B.2, an expression for the PSD of variations in N'_V:

$$S_{\delta N_V'}(f) = \frac{1}{\Delta V}.N_t.f_t.(1-f_t).\frac{4\tau}{1+(2\pi f)^2\tau^2}.\Delta E \tag{B.1}$$

Therefore, to obtain the PSD $S_{\delta N'_A}(f)$ for variations in N'_A, it is necessary to integrate (B.1) in the energy and in the z coordinate. Using the previously defined notation with $\Delta E \to 0$:

$$N'_A = \int_0^{t_{ox}} \int_{-\infty}^{\infty} N'_V .dE.dz \tag{B.2}$$

where t_{ox} is the oxide thickness. It follows:

$$S_{\delta N'}(f) = \frac{r^2}{\Delta A} \int_0^{t_{ox}} \int_{-\infty}^{\infty} N_t(z,E).f_t.(1-f_t).\frac{4\tau(z,E)}{1+(2\pi f)^2\tau(z,E)^2}.dE.dz \tag{B.3a}$$

$$S_{\delta N'}(f) \cong \frac{1}{\Delta A} r^2 N_t kT\lambda.\frac{1}{f} \tag{B.3b}$$

In section B.1 some physical aspects of the trapping-detrapping mechanism are presented, while eq.(B.1) is explicitly deduced using statistical considerations in section B.2. In section B.3, it is demonstrated that using classical approximations the integration of (B.3a) leads to the usual *1/f* noise form: $S_{\delta N'}(f) = K/f^{\gamma}$ as in (B.3b), with γ=1. Finally, in section B.3 a brief discussion of how a non-uniform trap distribution inside the oxide results in a γ exponent for flicker noise slightly different to 1, is presented.

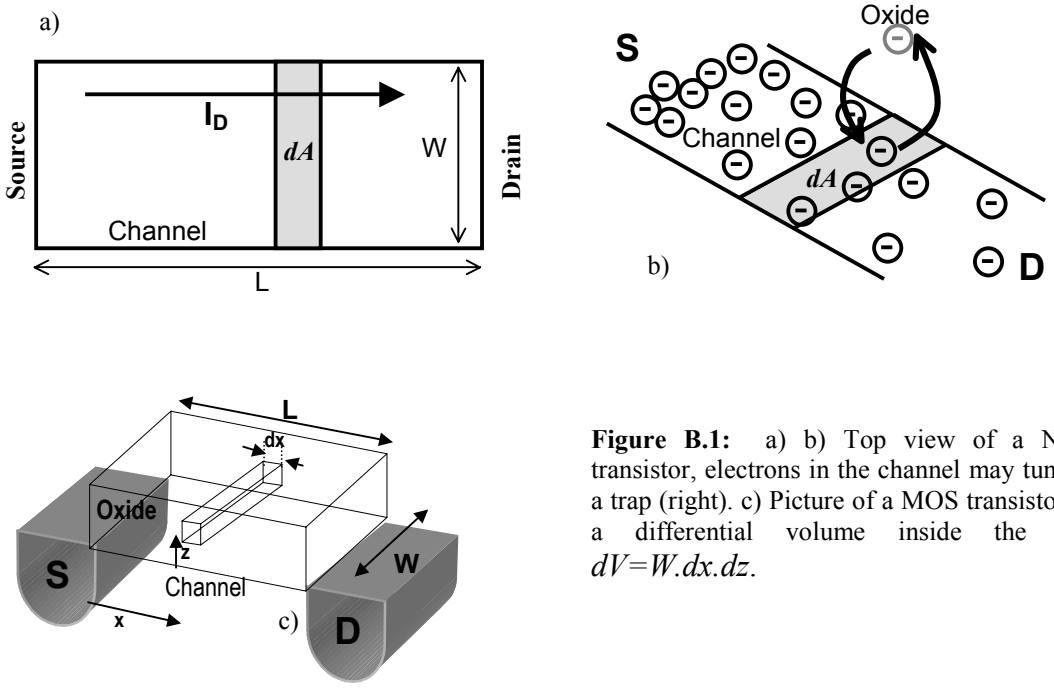


Figure B.1: a) b) Top view of a NMOS transistor, electrons in the channel may tunnel to a trap (right). c) Picture of a MOS transistor, and a differential volume inside the oxide $dV=W.dx.dz$.

B.1 THE CARRIER CAPTURE-EMISSION PROCESS.

In Fig.B.2, a typical diagram of the energy bands, in terms of the distance *z* to the surface, of a silicon-oxide interface is shown. Conduction and valence bands are bent near the boundaries of silicon and an electron in the conduction band is obstructed by a potential barrier U_o from reaching the oxide. Inside the oxide a 'trap' with an energy E_t is also shown. The trap is modeled as a space-localized state, a narrow potential hole with a characteristic energy E_t, where a electron can be held. The exact form of the potential hole is unknown and it will probably look like the potential of the hydrogen atom [103,104], but the narrow-rectangular hole approximation will be held because it is simple. Independently of the shape of the trap, E_t refers to the characteristic energy of its lower energy state. Despite a potential barrier U_o, electrons in the channel next the oxide surface (in a NMOS transistor) may tunnel to, and back from, the traps inside the oxide. From now on, the example of the NMOS transistor will be employed, but the analysis can be extended to holes in a PMOS device without further considerations.

When an electron is captured, its place in the conduction band is occupied by another electron either from the substrate or from the neighboring regions in the channel, the latter contributing to the noise current[1]. Noise current is also influenced because trapped electrons affect channel mobility due to the scattering effect [104]. Thus, trapping theory explain both channel carrier number, and channel mobility fluctuations, the two main effects contributing to flicker noise according to recent studies on this field.

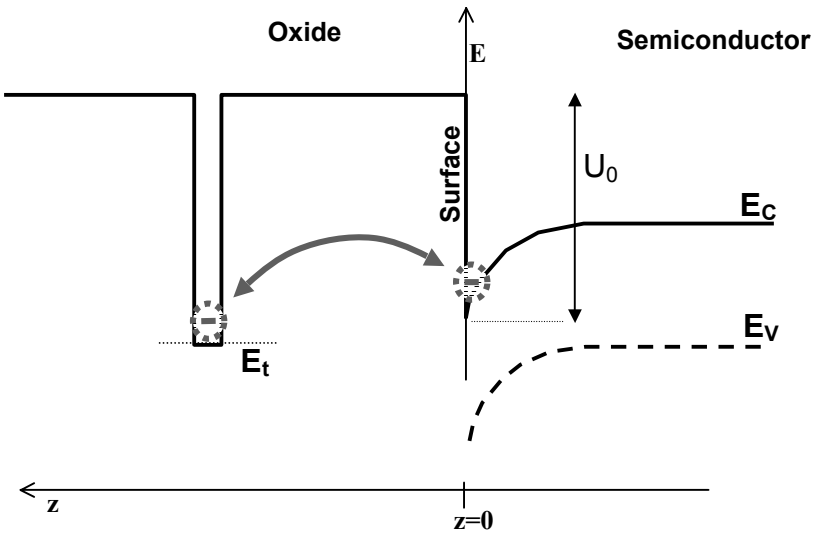


Figure B.2: A scheme showing the bended boundaries of the conduction and valence band near the surface of a semiconductor-oxide interfase. There is also shown a trap with energy E_t inside the oxide, and a electron that sees a potential barrier U_o to the oxide. The electron may tunnel to, and back from, the trap.

[1] So, not every electron that is trapped or released contributes a charge in the noise current.

B.2 PSD OF THE NUMBER OF OCCUPIED TRAPS: (I) $S_{\delta N_V^{'}}$

To find the PSD of a random variable i.e. $N_V^{'}$, it is necessary to compute its autocorrelation ([105] or see annex D):

$$\Re(s) = \overline{\delta N_V^{'}(t).\delta N_V^{'}(t-s)} \tag{B.4}$$

There will be occupied traps that may release their electron with a probability e_0, and empty traps that may capture an electron from the channel with a probability c_0. To compute (B.4) the Shockley-Read-Hall (SRH) statistics, as suggested in [78], is employed. As in the classical deduction of Poisson distribution [106] pp.115, the basic hypothesis is that in a differential time interval dt, individual traps may capture or release a single electron in a memoryless process. Occupied traps may be emptied with a probability $e_0.dt$, and empty traps may be occupied with a probability $(c_0 n_S).dt$. n_S is the electron density in the channel: the denser is the electron population in the conduction band, the more likely it is that an electron would tunnel to the empty trap. Given an initial $N_V^{'}$ density of occupied traps, their expected variation in the time interval *dt* is written using SRH:

$$dN_V^{'} = \left[c_0 n_S \left(N_t - N_V^{'}\right) - e_0 N_V^{'}\right]dt \tag{B.5}$$

$\left(N_t - N_V^{'}\right)$ is the number of empty traps per unit volume. At equilibrium, the average $N_V^{'}$ must be kept constant so the average number of captured and released electrons should be the same:

$$c_0 n_S (1 - f_t) - e_0 f_t = 0 \tag{B.6}$$

$$\frac{e_0}{c_0} = \frac{n_S (1 - f_t)}{f_t} = n_1 \tag{B.7}$$

The electron density at the conduction band is calculated [103]:

$$n_S = n_i . e^{\frac{E_f - E_i}{kT}} \tag{B.8}$$

Where E_i, n_i are the Fermi level, and the carrier concentration, respectively, in an intrinsic semiconductor crystal. It follows (B.7),(B.8):

$$n_1 = n_i e^{\frac{E_t - E_i}{kT}} \tag{B.9}$$

But $N_V^{'}$ is not at equilibrium in (B.5); $N_{Veq}^{'} = f_t N_t$ denotes the equilibrium value, which suffers variations: $N_V^{'} = N_{Veq}^{'} + \delta N_V^{'}$. If variations of n_S with $N_V^{'}$ are neglected, one can use (B.6) in (B.5):

$$\frac{d\left(\delta N_V^{'}\right)}{dt} = -\left(c_0.n_S + e_0\right)\delta N_V^{'} \tag{B.10}$$

(B.10) is a first order differential equation with the solution:

$$\delta N_V^{'} = \delta N_V^{'}\Big|_{t=0}.e^{\frac{-|t|}{\tau}} \tag{B.11}$$

where

$$\tau = \frac{1}{c_0\left(n_s + n_1\right)} \tag{B.12}$$

Note that $\delta N_V^{'}$ is a random variable, the value expressed in (B.11) is its expected value over time. $\delta N_V^{'}\Big|_{t=0}$ is an arbitrary known initial condition. Note also that (B.10) is solved in the time interval $t>0$; the absolute value in (B.11) was introduced due to symmetry. To find the autocorrelation of the process it is necessary to integrate in all possible $\delta N_V^{'}$ taking into account their probability $p(\delta N_V^{'})$:

$$\Re(s) = \int_{-\infty}^{\infty} \delta N_V^{'}.p(\delta N_V^{'}).\delta N_V^{'}.e^{-\frac{|s|}{\tau}}.d\delta N_V^{'} = e^{-\frac{|s|}{\tau}}.\overline{\delta N_V^{'\,2}} \tag{B.13}$$

The variance of $\delta N_V^{'}$ is known since $N_V^{'}.\Delta V.\Delta E$ is a binomial distribution (there are $N_t.\Delta V.\Delta E$ traps being occupied or empty):

$$\overline{\delta N_V^{'\,2}} = \frac{N_t.\Delta E.f_t\left(1-f_t\right)}{\Delta V} \tag{B.14}$$

Eq.(B.14) is presented in both [79,80]. Consequently, the exponential nature of the autocorrelation has been demonstrated:

$$\Re_{\Delta N_V^{'}}(s) = \frac{1}{\Delta V} N_t f_t\left(1-f_t\right)\Delta E.e^{-\frac{|s|}{\tau}} \tag{B.15}$$

To find the PSD $S_{\delta N_V^{'}}(w)$ it is necessary to Fourier transform (B.15) (unilateral PSD):

$$S_{\delta N_V^{'}}(w) = 2.\Im(\Re(s)) = \frac{1}{\Delta V} N_t f_t (1-f_t)\Delta E \frac{4\tau}{1+w^2\tau^2} \tag{B.16}$$

Thus, (B.1) has been demonstrated.

B.2.1 The τ constant.

If the energy of the electron in the channel is negligible compared with the potential barrier U_0 , its wave function Ψ_A inside the oxide is expressed [103,107]:

$$\psi_A(z) \propto e^{\frac{-z}{\lambda}}, \qquad \lambda = \left(\frac{\sqrt{2m^* U_0}}{h} \right)^{-1} \tag{B.17}$$

where m^*, h, λ, are respectively the effective mass of the electron, Planck's constant, and the tunneling constant. The wave function ψ_B of an electron in the trap is unknown. To calculate c_0, the probability of an electron at the surface being trapped by a single trap, complex calculations involving ψ_A, ψ_B , and interaction potentials (essentially phonons in the lattice [107]) are required. Since $\psi_A(z)$ behaves approximately constant in the region of the trap and its neighborhood where the calculation takes place (see Fig.B.3), it is possible to write:

$$c_0(z) = c.e^{-2z/\lambda} \tag{B.18}$$

where c is an adjustment constant, and using (B.13):

$$\tau(z) = \frac{1}{c(n_S + n_1)}.e^{-2z/\lambda} = \tau_s.e^{-2z/\lambda} \tag{B.19}$$

This is a simplified model because τ_S may depend on the trap energy and also on the average energy of the electrons in the channel.

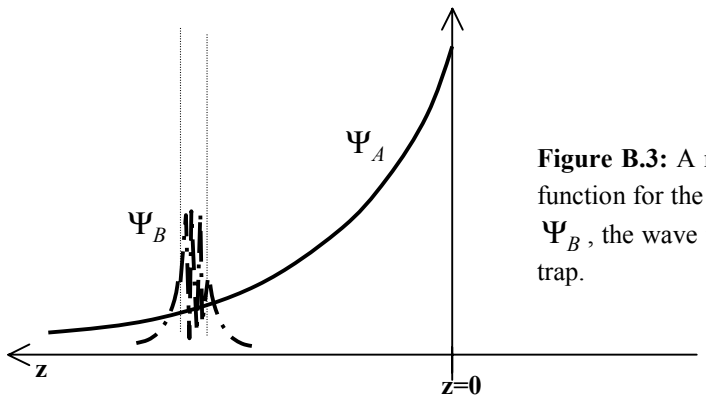


Figure B.3: A rough plot of Ψ_A , the wave function for the electron inside the oxide and Ψ_B , the wave function of an electron in the trap.

B.3 CLASSICAL APPROXIMATIONS TO COMPUTE THE PSD $S_{\delta N'_A}$ OF N'_A.

It is still necessary to integrate (B.1) in the *z* coordinate and in the energy.

$$S_{\Delta N_A}(w) = \frac{1}{\Delta A}\int_{E_C}^{E_V}\int_{0}^{t_{ox}} N_t f_t(1-f_t)\frac{4\tau}{1+w^2\tau^2}.dz.dE \tag{B.20}$$

There is little to say on (B.20) without extra hypotheses because both N_t, τ depend on the energy and the distance: $N_t = N_t(z,E), \quad \tau = \tau(z,E)$. Note that the integration boundaries in (B.20) are E_C , E_V instead of $\pm\infty$ as in (B.2). This is a classical approximation that is easily proved considering that the product $N_t f_t(1-f_t)$ is sharply peaked. But, also from a physical point of view, consider an electron that gains extra energy interacting with a phonon and could tunnel to a trap with an energy $E \geq E_C$. This electron will encounter in the conduction band a sea of states with such an energy and it is very unlikely that it would jump to the trap. Moreover, the probability of an electron tunneling to a trap is negligible outside the energy gap where it competes with a continuous of energy empty states at conduction ($E \geq E_C$) or valence band ($E \leq E_V$).

Classical approximations to solve (B.20) suppose that τ depends only on the distance z, and N_t, f_t on the energy. With the former hypothesis is possible to integrate (B.20) in the distance:

$$\int_{0}^{tox}\frac{\tau}{1+\omega^2\tau^2}dz = \frac{\lambda}{\omega}\left(tan^{-1}(\omega\tau(t_{ox})) - tan^{-1}(\omega\tau(0))\right) \cong \frac{\lambda}{4f} \tag{B.21}$$

The last approximation in (B.21) is due to the high dispersion in τ values (i.e. take m^* = mass of a free electron, t_{ox}=20Å, U_0=4eV $\Rightarrow$ $\tau_{max}/\tau_{min} = 10^{17}$) and (B.21) ends with the classical *1/f* dependence for flicker noise. Note that this dependence is not affected by τ_s value or other parameters in the channel.

The integration in the energy of (B.20) can be carried out with a probability balance as in (B.6), but generalized to both electrons and holes. It can be demonstrated with a balance at equilibrium ([107] pp.499) that:

$$f_t = \frac{p_1 + n_s}{n_s + p_s + n_1 + p_1} \tag{B.22}$$

where p_s, p_1 are the equivalent to (B.8), (B.9) for holes:

$$p_S = n_i.e^{\frac{E_i - E_f}{kT}} \qquad , \qquad p_1 = n_i e^{\frac{E_t - E_i}{kT}} \tag{B.23}$$

For the NMOS example $n_s >> p_s$ so it is possible to rewrite:

$$f_t(1-f_t) = \frac{p_1 p_s + n_1^2 + n_s p_s}{(p_s + n_1 + p_1)^2} \tag{B.24}$$

Using (B.23), (B.24) and the variable exchange $dE = kT\frac{du}{u}$ it is possible to integrate (B.20) in the energy, fixing the energy level $E = 0$ at the border of the valence band and integrating up to ∞ for simplicity:

$$\int_0^{\infty} N_t f_t(1-f_t).dE \approx N_t kT\left[1 - 2\left(\frac{n_i}{n_s} - \frac{p_s}{n_i}\right)\frac{E_i - F_n}{kT}\right] \approx N_t kT \tag{B.25}$$

The simplified result is thus:

$$S_{N_A'} = \frac{1}{\Delta A} N_t kT\lambda . \frac{1}{f} = \frac{N_{ot}}{\Delta A} . \frac{1}{f} \tag{B.26}$$

$N_{ot} = N_t kT\lambda$ in (B.26) is the equivalent density of oxide traps traps, defined as in reference [82]. N_{ot} will be a technology parameter to adjust.

B.4 THE VALUE OF THE CONSTANT γ:

It is a known fact that the constant γ in eq.(3.9) is not exactly 1. Variations in γ are attributed to a non-uniform distribution of traps inside the oxide. The spatial distribution of traps affects (B.20) but at this stage τ will still be considered as depending only on *z*. Re-writing (B.20):

$$S_{\Delta N_A'}(w) = \frac{1}{\Delta A}\int_0^{t_{ox}} \eta(z).\frac{4\tau}{1+w^2\tau^2}.dz \tag{B.27}$$

The function $\eta(z)$ contains variations of $N_t f_t(1-f_t)$ integrated in the energy. N_t may vary with *z* but f_t, in principle, is only a function of the energy (because the Fermi level is the same for the electron system). In [85], F. Berz shows that an exponential distribution for $N_t(z)$ preserves the model in (3.9) for flicker noise and leads to γ≠1 when integrating (B.27). But there are few complimentary studies on this topic.

To evaluate the influence in γ of a non-uniform trap distribution along the oxide, some simulations were performed for the following cases: A) $\eta(z)$ constant; B) $\eta(z)$ positive exponential ; C) $\eta(z)$ linear; D) $\eta(z)$ negative exponential. The plots for $\eta(z)$ are presented in Fig.B.4. In Fig.B.5 the result of the numerical integration on (B.27) is shown at several frequencies. The picture demonstrates that the model in (3.9) is still valid for A, B, C, D

with different γ coefficients. For decreasing distributions of $\eta(z)$ profile, the result is γ>1, while for increasing distributions in $\eta(z)$, the result is γ<1.

In the plot of Fig.B.6, the adjusted values of γ for the different measurement sets presented in chapter 3 on flicker noise are shown. For each point in Fig.B.6, *K*, γ were adjusted using (3.9). In spite of the fact that there is a considerable experimental error, the measurements validate that γ=1 is a good estimation.

Although it is a reasonable hypothesis to suppose that there would be a high concentration of traps near the surface of the oxide (decreasing distribution); from the measurements presented in Fig.B.6 as well as several measurements that have been previously reported, it is not possible to conclude whether γ usually takes values greater or smaller than 1. The result presented in [108], where the surface of silicon is cleaned with hydrogen-ammonium to reduce defects in the surface and thus noise, is very suggestive. Not only a flicker noise reduction is reported, but also γ decreases and the noise PSD becomes less regular.

A more detailed analysis is not the aim in this presentation, but simulations should consider:

- the trap distribution not only in space but also in energy $N_t(z,E)$
- the dependence of τ_s in (B.19) with *z,E,* because c, n_1 are not constants.

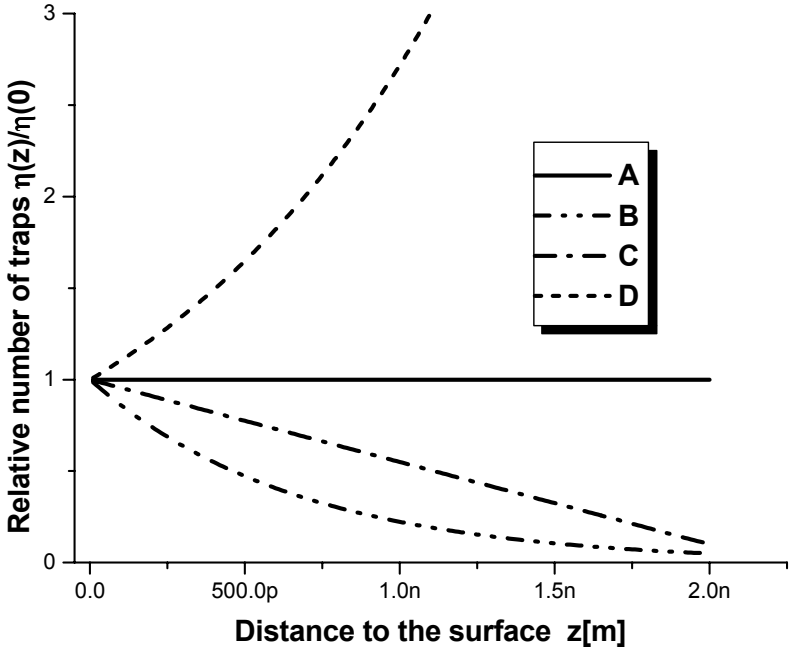


Figure B.4: The diferent profiles of the función η(z) used to compute the frequency dependence of the PSD $\Delta N_{V'}(f)$.

A - $\eta = Constant$

B - growing exponential $\eta(z) = \eta_0 . e^{z/\alpha}$

C - linear $\eta(z) = \eta_0 . (1 + \alpha z)$

D - decreasing exponential $\eta(z) = \eta_0 . e^{-z/\alpha}$

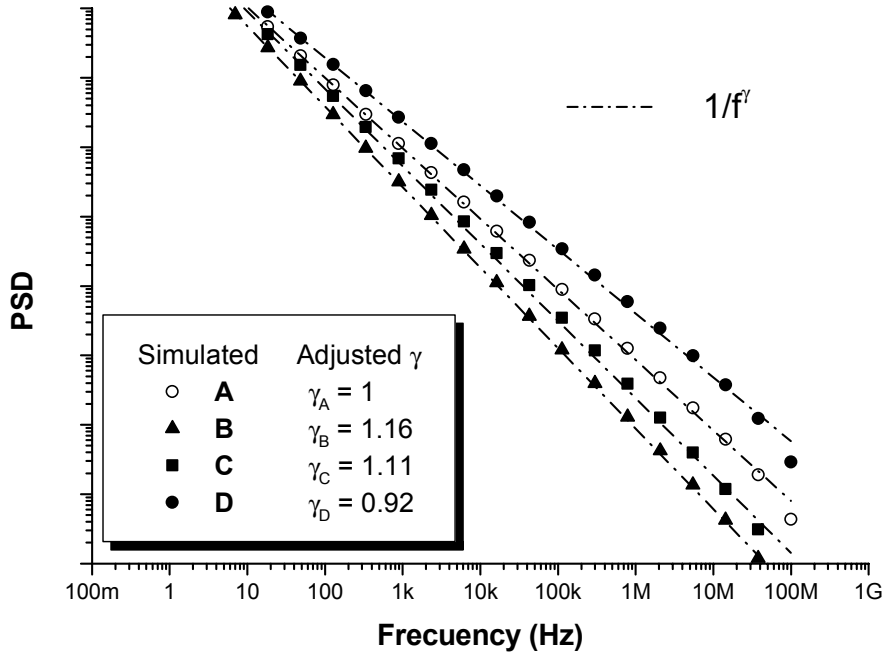


Figure B.5: The result of the integration of (B.27) at several frequencies, using the η profiles of Fig.B.4. The relationship $PSD \propto \frac{1}{f^{\gamma}}$ is approximately valid in al cases. Note that decreasing profiles η(z) lead to γ>1.

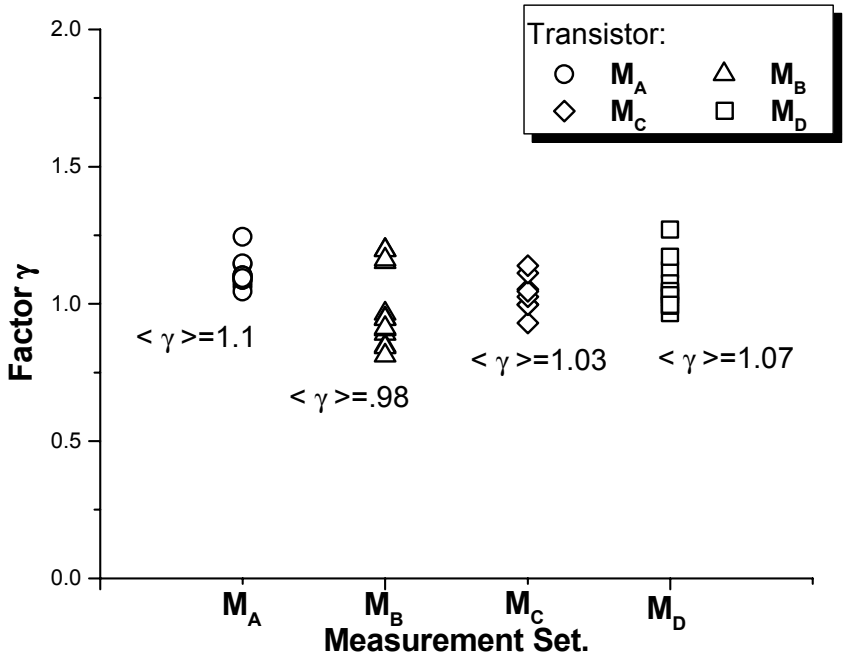


Figure B.6: Experimetal distribution of γ factor when procesing different measurements of chapter 3 adjusting $\gamma \neq 1$. $\mathbf{M_A}$,$\mathbf{M_C}$ is for the same NMOS, W/L=200/16, saturated ($\mathbf{M_A}$ - Fig.3.8), linear region ($\mathbf{M_C}$ - Fig.3.9). $\mathbf{M_B}$ is a saturated PMOS W/L=200/16 (Fig.3.11). $\mathbf{M_D}$ is a saturated NMOS, W/L=40/12 (Fig.3.12).

Annex C:

Consistent Model for Drain Current Mismatch in MOSFETS Using the Carrier Number Fluctuation Theory.

This annex shows how the extension of the simple model for the MOSFET channel of section 3.2 allows the derivation of a consistent mismatch model. The formal equivalence of mismatch and low frequency noise models for the MOS transistor in all operating regions will be derived in this section. This equivalence comes from the fact that space-fluctuations in the channel cause mismatch, in the same way as time-fluctuations produce flicker noise.

Existing mismatch models use either simple drain current models limited to a specific operating region [60,61,63-65] as in eq.(2.18) or complex expressions [66] like that of BSIM. In general, however, the applicability of DC current models to characterize mismatch is not questioned. The effect of the random parameters on the drain current is quantified using the DC model of the transistor. As pointed out in [64, 65] there is a fundamental flaw in this approach that results in inconsistent modeling of matching. In effect, mismatch models implicitly assume that the actual values of the lumped model parameters can be obtained integrating the position-dependent distributed models over the areas of the channel region of the device, e.g., for the threshold voltage V_T

$$V_T = \frac{1}{WL} \iint_{channel-area} V_T(x,y)dxdy \tag{C.1}$$

where W and L are the width and the length of the transistor, respectively. As analyzed in [64,65], the application of (C.1) to series or parallel association of transistors leads to an inconsistent model of matching owing to the nonlinear nature of MOSFETs. Consequently, the simple consideration of random fluctuations in the lumped parameters of the DC current model is not appropriate to develop matching models and new formulas must be derived from basic principles. The formalism needed to model matching is already available in low frequency noise modeling in chapter 3.

The fluctuation of the drain current around its nominal value presented in eq.(3.11) is the sum of the contributions of local fluctuations along the channel, whatever their origin. (3.11) is valid with wide generality, and (3.13) can be re-written:

$$i_{\Delta A} = I_D \frac{\Delta Q_I'}{Q_I'} \tag{C.2}$$

For mismatch calculation, we consider local fluctuations in the threshold voltage that affect the local charge density and thus produce current variations from the ideal value. From UCCM, eq.(2.3), one can readily derive the relation between local charge density and threshold voltage fluctuations:

$$\Delta Q_I' = C_{ox}' \frac{Q_I'}{Q_I' - nC_{ox}'\varphi_t} \Delta V_T \ . \tag{C.3}$$

The variance $\overline{\Delta V_T^2}$ of the local fluctuation of the threshold voltage ΔV_T is calculated from the conventional expression of (2.18):

$$\overline{\Delta V_T^2} = \sigma_{VT}^2 = \frac{A_{VT}^2}{W\Delta x} \ . \tag{C.4}$$

Using (C.2), (C.3), and (C.4) we calculate $(i_{\Delta A})^2$ and, inserting the resultant $(i_{\Delta A})^2$ into (3.11), we obtain the expression of $\overline{\Delta I_D^2}$. With the aid of (2.2), the integration along the channel length in (3.11) changes into an integration on the channel charge density:

$$\sigma_{I_D}^2 = \overline{\Delta I_D{}^2} = \frac{\mu C_{ox}' I_D A_{VT}^2}{nL^2} \int_{Q_{IS}'}^{Q_{ID}'} \frac{1}{nC_{OX}'\phi_t - Q_I'} dQ_I' \ . \tag{C.5}$$

(C.5) is equivalent to (3.15b). Assuming, as in [71], Poisson statistics for the depletion charge fluctuation, then

$$A_{VT}^2 = \frac{q^2}{C_{ox}'{}^2}\left(N.x_D\right) = \frac{q^2}{C_{ox}'{}^2} N_{oi} \tag{C.6}$$

where N_{oi} is the average number of impurities per unit volume in the depletion region, x_D is the depletion depth, and $N_{oi}=N.x_D$ is the effective number of impurities per unit area in the depletion layer. Finally, using (C.6) and integrating (C.5) from source to drain results in:

$$\frac{\sigma_{I_D}^2}{I_D^2} = \frac{q^2 N_{oi}\mu}{L^2 nC_{ox}' I_D} ln\left(\frac{nC_{ox}'\varphi_t - Q_{IS}'}{nC_{ox}'\varphi_t - Q_{ID}'}\right) \tag{C.7}$$

The result in (C.7) is essentially the same as that derived for flicker noise in MOS transistors in chapter 3 (eq.(3.16)). This is because mismatch is a “DC noise” and the physical origin of both mismatch and flicker noise is fluctuation of either fixed charges or localized states along the channel. Considerations for flicker noise can be immediately extended to mismatch. Particularly the analysis of (C.7) in terms of the inversion level of the transistor is analogous to eqs.(3.19) to (3.23). Therefore, (2.18) is a good estimation of (C.7) as the empirical noise model in (3.23) is a good approximation of the physical based model in (3.16).

Annex D:

Noise and Offset Calculation in OTAs with(without) Series-Parallel Current Division.

In this annex, exact noise and offset expressions are deduced for OTAs like those presented in chapter 4. Also, some basic concepts for dealing with noise in electronic circuits are presented firstly. This noise basics revision would help to understand not only noise calculations in this annex, but also some theoretical deductions previously presented.

Note: OTA noise and offset calculations are referred on each case to a picture defining transistor names. In all cases for a given transistor M_X, I_{DX}, g_{mX}, $(WL)_X$, β_X, will denote its drain current, gate transconductance, gate area or current factor respectively.

D.1 NOISE BASICS

A noise voltage is a random signal $v_n(t)$ that usually is present in electronic systems. The rms value of the noise is defined:

$$v_{n_{rms}} = \sqrt{\overline{v_n^2}} = \left[\frac{1}{T}\int_0^T v_n(t)^2\,dt\right]^{1/2}, \tag{D.1}$$

where T is a suitable averaging time. Noise is not a deterministic signal. It is a stochastic process, so to deal with it in the frequency domain is necessary to work with its Power Spectral Density (PSD). For a given signal, the PSD is equal to the energy contained in between a frequency f and $f+df$. If in a random signal $n(t)$, its autocorrelation $\Re_n(\tau)$ is known, it is possible to calculate its PSD, $S_n(f)$:

$$S_n(f) = \left|\Im(\Re_n(\tau))\right| \tag{D.2}$$

where $\Im(\,)$ stands for Fourier-transform. The autocorrelation is defined:

$$\Re_n(\tau) = \langle n(t), n(t+\tau)\rangle \tag{D.3}$$

$\langle ... \rangle$ denotes statistical average of the product of the quantity inside. For noise voltage, the units of its PSD $S_{vn}(f)$ are then $\frac{V^2}{Hz}$, but usually the noise is described with the root spectral

density $v_n(f) = \sqrt{S_n(f)}$ with units $\frac{V}{\sqrt{Hz}}$. It is easy to demonstrate that the average noise voltage defined in eq.(D.1) can be expressed in terms of the PSD:

$$\overline{v_n^2} = \int_{-\infty}^{\infty} S_n(f).df = \int_{-\infty}^{\infty} (v_n(f))^2.df \,. \tag{D.4}$$

Noise current as usually handled in MOS design (see Fig.3.1) is defined analogous to (D.1): $\overline{i_n^2} = \int_{-\infty}^{\infty} i_n(f)^2.df$, and in this case the units are $\frac{A^2}{Hz}$ and $\frac{A}{\sqrt{Hz}}$ for the PSD and root spectral density respectively.

In the literature usually the PSD is given in two ways, unilateral or bilateral. The former is defined only for frequency *f* between 0 to infinity and the latter is defined for the whole frequency range. For the case of unilateral PSD integral in (D.4), and any other integration of the PSD, should change lower limits from -∞ to 0. Since $v_n(t)$ is a real signal, $S_{vn}(f)$ is symmetrical in the bilateral case with half the value of the unilateral PSD for the same frequency.

Adding noise sources.

It is easy to demonstrate that if several independent noise sources with voltage values v_{n_i} are summed, the total noise voltage v_{n_tot} results:

$$v_{n\_tot} = \sqrt{\sum_i \overline{v}_{n\_i}^2} \tag{D.5}$$

In the case of correlated sources, a correlation term multiplying crossed products $v_{n\_i}.v_{n\_j}$ should be added on eq.(D.5) but this is not a usual practice in the electronic design where noise sources are always supposed to be independent.

Filtering noise.

If a noisy signal is passed trough a linear system with a transfer function *H*(*f*), the resulting PSD in the output is calculated:

$$S_o(f) = S_i(f).\left|H(f)\right|^2 \tag{D.6}$$

As an example, consider a white noise source with a constant power spectral density S_w (bilateral PSD) that is filtered with a single pole low-pass filter. The total noise in the output will be:

$$\overline{v}_n^2 = \int_{-\infty}^{\infty} S_w.\left|\frac{1}{1+jf/f_p}\right|^2 df = S_w.\int_{-\infty}^{\infty} \frac{1}{1+(f/f_p)^2} df = S_w.\pi.f_p \tag{D.7}$$

This equation is usually expressed like $v_n^2 = 2.S_w.\Delta f$, where Δf is the *noise bandwidth*, that is not the same as the commonly used –3dB bandwidth in amplifiers. The noise bandwidth is the frequency span of a rectangular shaped power gain curve, equal in area to the actual power gain versus frequency curve:

$$\Delta f = \frac{1}{H_{MAX}} \int_0^\infty H(f).df \tag{D.8}$$

D.2 NOISE IN A STANDARD SYMMETRICAL OTA.

The total input referred noise in a classical symmetrical OTA with a copy factor B in the output branch as in Fig.D.1 can be calculated summing both thermal and flicker noise contribution, from eq.(3.31) (unilateral PSD):

$$\begin{aligned} \bar{v}_{n\_Tot}^2 = {} & \frac{4nk_BT(f_2-f_1)}{g_{m1}}.\left(1+\left(1+\frac{1}{B}\right)\frac{g_{m2}}{g_{m1}}+\frac{1}{B^2}\frac{g_{m3}}{g_{m1}}\right)+ \\ & +\frac{2nk_BTLn(f_2/f_1)}{N^*C_{ox}^{'}}\left(\frac{N_{otP}}{(WL)_1}+\frac{N_{otN}\left(1+\frac{1}{B}\right)}{(WL)_2}.\frac{g_{m2}^2}{g_{m1}^2}+\frac{N_{otP}}{(WL)_3B^2}.\frac{g_{m3}^2}{g_{m1}^2}\right) \end{aligned} \tag{D.9}$$

In (D.9) noise has been integrated in the band of interest from f_1 to f_2. It is more clear to see the impact of each transistor in noise, using the gate transconductance to drain current ratio:

$$\begin{aligned} \bar{v}_{n\_Tot}^2 = {} & \frac{4nk_BT(f_2-f_1)}{g_{m1}}.\left(1+\left(1+\frac{1}{B}\right)\frac{(g_m/I_D)_2}{(g_m/I_D)_1}+\frac{1}{B}\frac{(g_m/I_D)_3}{(g_m/I_D)_1}\right)+ \\ & +\frac{2nk_BTLn(f_2/f_1)}{N^*C_{ox}^{'}}\left(\frac{N_{otP}}{(WL)_1}+\frac{N_{otN}\left(1+\frac{1}{B}\right)}{(WL)_2}.\left(\frac{(g_m/I_D)_2}{(g_m/I_D)_1}\right)^2+\frac{N_{otP}}{(WL)_3}.\left(\frac{(g_m/I_D)_3}{(g_m/I_D)_1}\right)^2\right) \end{aligned} \tag{D.10}$$

Note that (D10) is still valid for a copy factor B<1. In the case of a standard symmetrical OTA where *B*=1, (D.10) reduces to:

$$\bar{v}_{n\_Tot}^2 = \frac{4nk_BT(f_2-f_1)}{g_{m1}}.\left(1+2\frac{g_{m2}}{g_{m1}}+\frac{g_{m3}}{g_{m1}}\right)+\frac{2nk_BTLn(f_2/f_1)}{N^*C_{ox}^{'}}\left(\frac{N_{otP}}{(WL)_1}+\frac{2N_{otN}}{(WL)_2}.\frac{g_{m2}^2}{g_{m1}^2}+\frac{N_{otP}}{(WL)_3}.\frac{g_{m3}^2}{g_{m1}^2}\right) \tag{D.11}$$

Note in (D.10), (D.11) that if M_1 is in weak inversion while M_2, M_3, are in strong inversion, both flicker[1] and thermal noise can be approximated by that of the two transistors in the input pair. In example thermal noise result

$$\bar{v}_{n\_w}^2 \approx \frac{4nk_BT(f_2 - f_1)}{g_{m1}} \tag{D.12}$$

Expression (D.12) is exactly the thermal noise of an equivalent resistor $R_{eq}=1/g_{m1}$, multiplied by the slope factor n. Thus concerning thermal noise, an OTA may be as near efficient as a resistor. This result will be extended on next section to series-parallel division OTAs.

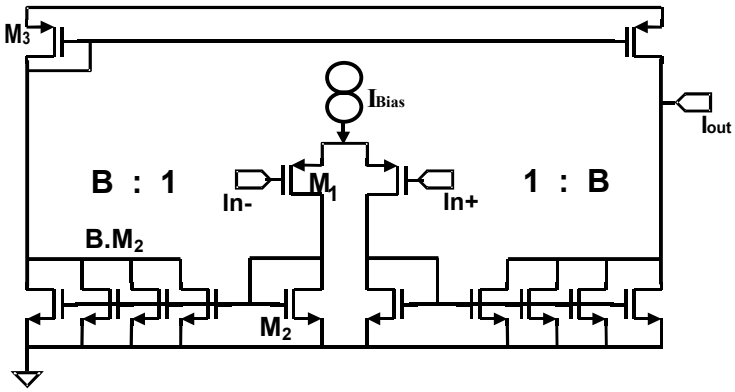


Figure D.1: Classical symmetrical OTA with copy factor B.

D.3 INPUT NOISE IN A SYMMETRICAL OTA WITH SERIES-PARALLEL CURRENT DIVISION.

Owing to simplicity, in this section flicker noise and thermal noise are calculated separately.

D.3.1 Thermal Noise.

For the OTA in Fig.4.9 using series-parallel current division, the total transconductance is $G_m = \frac{g_{m1}}{N^2}$. The following gate-transconductance-to-drain-current ratios are defined for M_1, M'_2, M''_2, M_3: $\Lambda_1 = \frac{g_{m1}}{I_{D1}}$, $\Lambda'_2 = \frac{g_{m2'}}{I_{D2'}}$, $\Lambda''_2 = \frac{g_{m2''}}{I_{D2''}}$, $\Lambda_3 = \frac{g_{m3}}{I_{D3}}$.

The total amount of thermal noise at the input, result from the sum of the contribution of each transistor M_1, M_2', M_2'', M_3 thermal noise calculated as in (3.31):

[1] Assuming similar gate areas.

$$\bar{v}_{n\_Tot}^2 = \frac{4nk_BT(f_2 - f_1)}{g_{m1}} \cdot \left(1 + \frac{g_{m2}^{'}}{g_{m1}} + N^4 \frac{g_{m2}^{''}}{g_{m1}} + N^4 \frac{g_{m3}}{g_{m1}} \right) \tag{D.13}$$

$$\bar{v}_{n\_Tot}^2 = \frac{4nk_BT(f_2 - f_1)}{g_{m1}} \cdot \left(1 + \frac{\Lambda_2^{'}}{\Lambda_1} + N^2 \frac{\Lambda_2^{''}}{\Lambda_1} + N^2 \frac{\Lambda_3}{\Lambda_1} \right) \tag{D.14}$$

Assuming that $N^2 >> 1$, that $M_2^{''}, M_3$ are in weak inversion, and using the expression in 2.16 for Λ it is possible to approximate (D.14) with the simple expression.

$$\bar{v}_{n\_Tot}^2 \approx \frac{4nk_BT(f_2 - f_1)}{G_m} \eta \tag{D.15}$$

where the factor $\eta = \left(\sqrt{1 + i_{f1}} + 1 \right)$. Note how similar is the expression in (D.15) to that in (D.12). The η factor indicates the excess noise if the differential input pair is biased in moderate or strong inversion to enhance its linear range[2].

D.3.2 Flicker Noise.

In-band input referred flicker noise in the circuit of Fig.4.9 can be also calculated summing the contribution of each transistor from (3.31):

$$\bar{v}_{n\_Tot}^2 = \frac{2nk_BTLn(f_2/f_1)}{N^* C_{ox}^{'}} \left(\frac{N_{otP}}{(WL)_1} + \frac{N_{otN}}{N(WL)_2} \cdot \frac{g_{m2}^{'\,2}}{g_{m1}^2} + \frac{N_{otN} \cdot N^4}{N(WL)_2} \cdot \frac{g_{m2}^{''\,2}}{g_{m1}^2} + \frac{N_{otP} \cdot N^4}{(WL)_3} \cdot \frac{g_{m3}^2}{g_{m1}^2} \right) \tag{D.16}$$

$$\bar{v}_{n\_Tot}^2 = \frac{2nk_BTLn(f_2/f_1)}{N^* C_{ox}^{'}} \left(\frac{N_{otP}}{(WL)_1} + \frac{N_{otN}}{N(WL)_2} \cdot \frac{\Lambda_2^{'2}}{\Lambda_1^2} + \frac{N_{otN} \cdot N^2}{N(WL)_2} \cdot \frac{\Lambda_2^{''2}}{\Lambda_1^2} + \frac{N_{otP} \cdot N^2}{(WL)_3} \cdot \frac{\Lambda_3^2}{\Lambda_1^2} \right) \tag{D.17}$$

Assuming that $N^2 >> 1$, that $M_2^{''}, M_3$ are in weak inversion, and using the expression in (2.16) for Λ:

$$\bar{v}_{n\_Tot}^2 \approx \frac{2nk_BTLn(f_2/f_1)}{N^* C_{ox}^{'}} \left[\frac{N_{otP}}{(WL)_1} + \eta^2 \left(\frac{2N_{otN}}{N(WL)_2} + \frac{N_{otP}}{(WL)_3} \right) \right] \tag{D.18}$$

(D.18) is a simple expression for input referred flicker noise in series-parallel current division OTAs. Note that the η factor is related also in this case, to the excess noise in comparison to a standard symmetrical OTA in (D.11). Equations from (D.13) to (D.18) can

[2] See chapter 4.

be extended to a generic series-parallel current division as in Fig.4.5, with the aid of (4.21), (4.22). Also noise analysis can be extended with a result close to that in (D.15), (D.18), to a linearized OTA like the one in Fig.D.2.

D.4 OFFSET IN A OTA USING SERIES-PARALLEL CURRENT DIVISION.

In this section, mismatch offset estimation in OTAs is presented. Calculations are based on the analysis of fluctuations $\left(\sigma^2_{V_T}\right)_X, \left(\sigma^2_\beta/\beta^2\right)_X$, in the threshold voltage and current factor of each M_X transistor in a circuit. However no mismatch model will be assumed for these fluctuations that can be either substituted for example by the simple model in (2.18).

The expected input referred offset in the circuit of Fig.4.9 can be calculated summing the mismatch contribution of each transistor. Current mismatch of the input pair M_1, and current mirror M_3 transistors are calculated as in (2.19) and then converted to input referred voltage. Eq.(4.17) is used to estimate the mismatch offset contribution of the series-parallel division mirrors.

$$\sigma^2_{V_{in}} = \overbrace{2\left[\left(\sigma^2_{V_T}\right)_1 + \frac{1}{\Lambda_1^2}\left(\frac{\sigma^2_\beta}{\beta^2}\right)_1\right]}^{\text{offset contribution of } M_1 \text{ transistors}} + \overbrace{4\frac{I^2_{D1}}{N.g^2_{m1}}\left[\Lambda''^2_2\left(\sigma^2_{V_T}\right)_2 + \left(\frac{\sigma^2_\beta}{\beta^2}\right)_2\right]}^{\text{offset contribution of series-parallel current mirrors.}} + \overbrace{2\frac{I^2_{D1}}{g^2_{m1}}\left[\Lambda^2_3\left(\sigma^2_{V_T}\right)_2 + \left(\frac{\sigma^2_\beta}{\beta^2}\right)_2\right]}^{\text{offset contribution of } M_3 \text{ mirror transistors.}} \tag{D.19}$$

To complete offset study, it is necessary to extend (D.19) to OTAs with a linearized input pair. The effective transconductance g_{m_eff} of a linearized differential pair like in Fig.D.2 is calculated with a small signal analysis, assuming that transistors M_4 operate in the linear region behaving each as a resistor $2R$.

$$g_{m\_eff} = \frac{g_{m1}}{1 + n g_{m1} R} \tag{D.20}$$

The resulting transconductance of the OTA is $G_m = \frac{g_{m\_eff}}{N^2}$. Since at null input, ideally there is no voltage drop across M_4 (V_{Sa}=V_{Sb} in Fig.D.2), M_4 transistor fluctuations do not contribute to offset. To calculate the contribution to input referred offset of M_1 transistors, it is necessary to estimate the effect of fluctuations in threshold voltage $\Delta V_{T1a}, \Delta V_{T1b}$, and current factor $\Delta\beta_{1a}, \Delta\beta_{1b}$, in M_{1a} and M_{1b} transistors. These fluctuations, as well as variations in the source voltage of both transistors, produce fluctuations $\Delta I_a, \Delta I_b$, on their drain currents. With a first order analysis close to that in (2.19):

$$\Delta I_a = -g_{m1}\Delta V_{T1a} + \frac{I_{D1}}{\beta_1}\Delta\beta_{1a} + n.g_{m1}\Delta V_{Sa} \tag{D.21}$$

$$\Delta I_b = -g_{m1}\Delta V_{T1b} + \frac{I_{D1}}{\beta_1}\Delta\beta_{1b} + n.g_{m1}\Delta V_{Sb} \tag{D.22}$$

Subtracting (D.21)-(D.22), and using that $\Delta I_a - \Delta I_b = -\left(\frac{\Delta V_{S1} - \Delta V_{S1}}{R}\right)$ result:

$$\Delta I_a - \Delta I_b = -g_{m1}\left(\Delta V_{T1} - \Delta V_{T2}\right) + \frac{I_{D1}}{\beta_1}\left(\Delta\beta_{1_a} - \Delta\beta_{1_b}\right) - n.g_m R\left(\Delta I_a - \Delta I_b\right) \tag{D.23}$$

Assuming as usual that fluctuations are non-correlated:

$$\sigma^2_{I_a - I_b} = \frac{2}{1 + n g_{m1} R}\left[g^2_{m1}\left(\sigma^2_{V_T}\right)_1 + I^2_{D1}\left(\frac{\sigma^2_\beta}{\beta^2}\right)_1 \right] \tag{D.24}$$

Note that when dividing (D.24) by $g_{m\_eff}^2$ to calculate the input referred mismatch offset voltage contribution of the linearized pair result

$$\sigma^2_{V_{in}pair} = 2\left[\left(\sigma^2_{V_T}\right)_1 + \frac{I^2_{D1}}{g^2_{m1}}\left(\frac{\sigma^2_\beta}{\beta^2}\right)_1 \right], \tag{D.25}$$

that is exactly the same offset contribution than the case of a standard differential input pair in (D.19). The only excess offset term when using a linearized pair, is given by the mismatch between the bias currents of M_{1a}, M_{1b}.[3]

To calculate the input referred offset in the circuit of Fig.D.2, terms should be summed as in (D.19). Terms are similar however:
- g_{m_eff} substitutes g_{m1} in the denominator in the second and third terms of (D.19) [3].
- A fourth term related to the mismatch introduced by biasing transistors M_5 that should be included.
The resulting estimated mismatch offset is:

$$\begin{aligned}\sigma^2_{V_{in}} = 2\left[\left(\sigma^2_{V_T}\right)_1 + \frac{1}{\Lambda_1^2}\left(\frac{\sigma^2_\beta}{\beta^2}\right)_1 \right] + 4\frac{I^2_{D1}}{N.g^2_{m\_eff}}\left[\Lambda''^2_2\left(\sigma^2_{V_T}\right)_2 + \left(\frac{\sigma^2_\beta}{\beta^2}\right)_2 \right] + ... \\ ... + 2\frac{I^2_{D1}}{g^2_{m\_eff}}\left[\Lambda^2_3\left(\sigma^2_{V_T}\right)_2 + \left(\frac{\sigma^2_\beta}{\beta^2}\right)_2 \right] + 2\left[\frac{g^2_{m5}}{g^2_{m\_eff}}\left(\sigma^2_{V_T}\right)_5 + \frac{I^2_{D5}}{g^2_{m\_eff}}\left(\frac{\sigma^2_\beta}{\beta^2}\right)_5 \right]\end{aligned} \tag{D.26}$$

[3] Of course there is also an excess offset at the input because the effective transconductance of the differential pair has been reduced when dividing current offset contribution of mirrors.

It should be pointed that expressions (D.19), (D.26), can be extended to generic series-parallel current division as in Fig.4.5. These generic expressions were used to estimate offset in the fabricated OTAs in table 4.4.

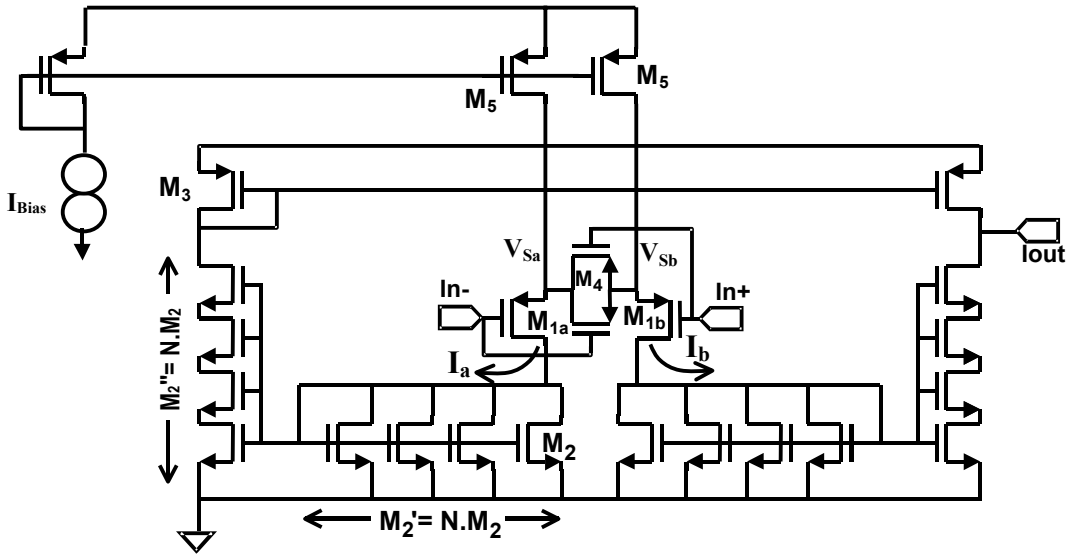
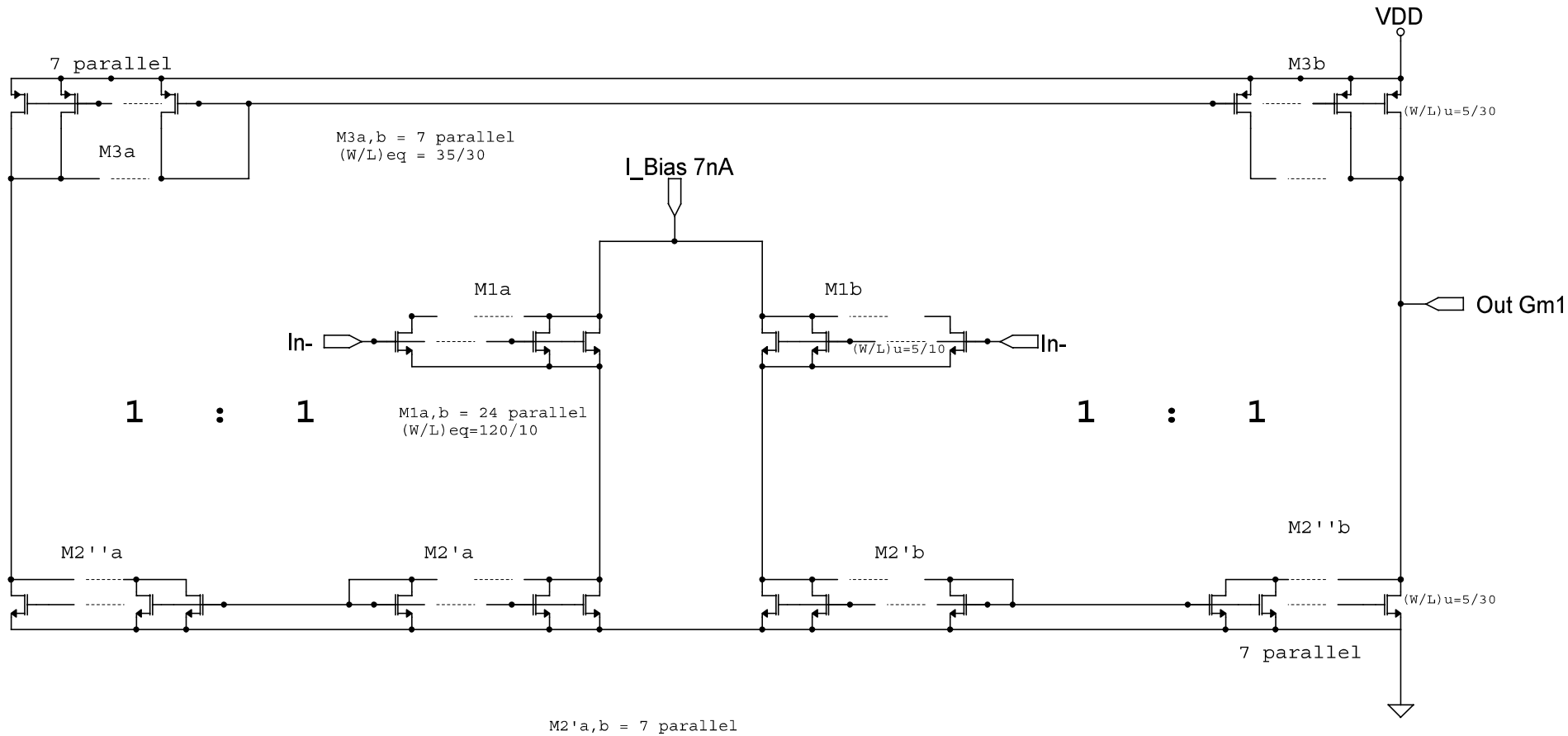


Figure D.2: Series-parallel current division OTA with linearized input, showing the biasing transistors M_5.

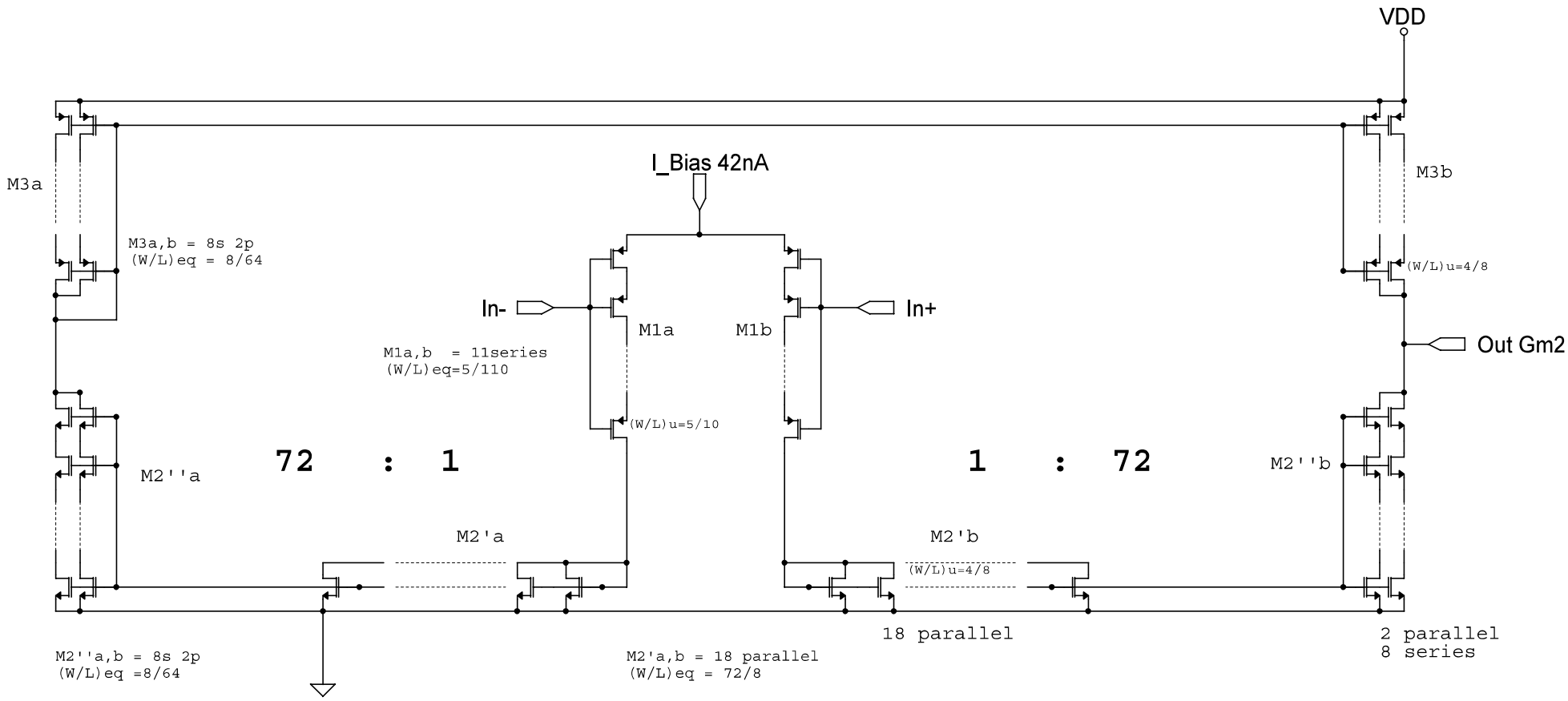
Annex E:

Circuit Schematics

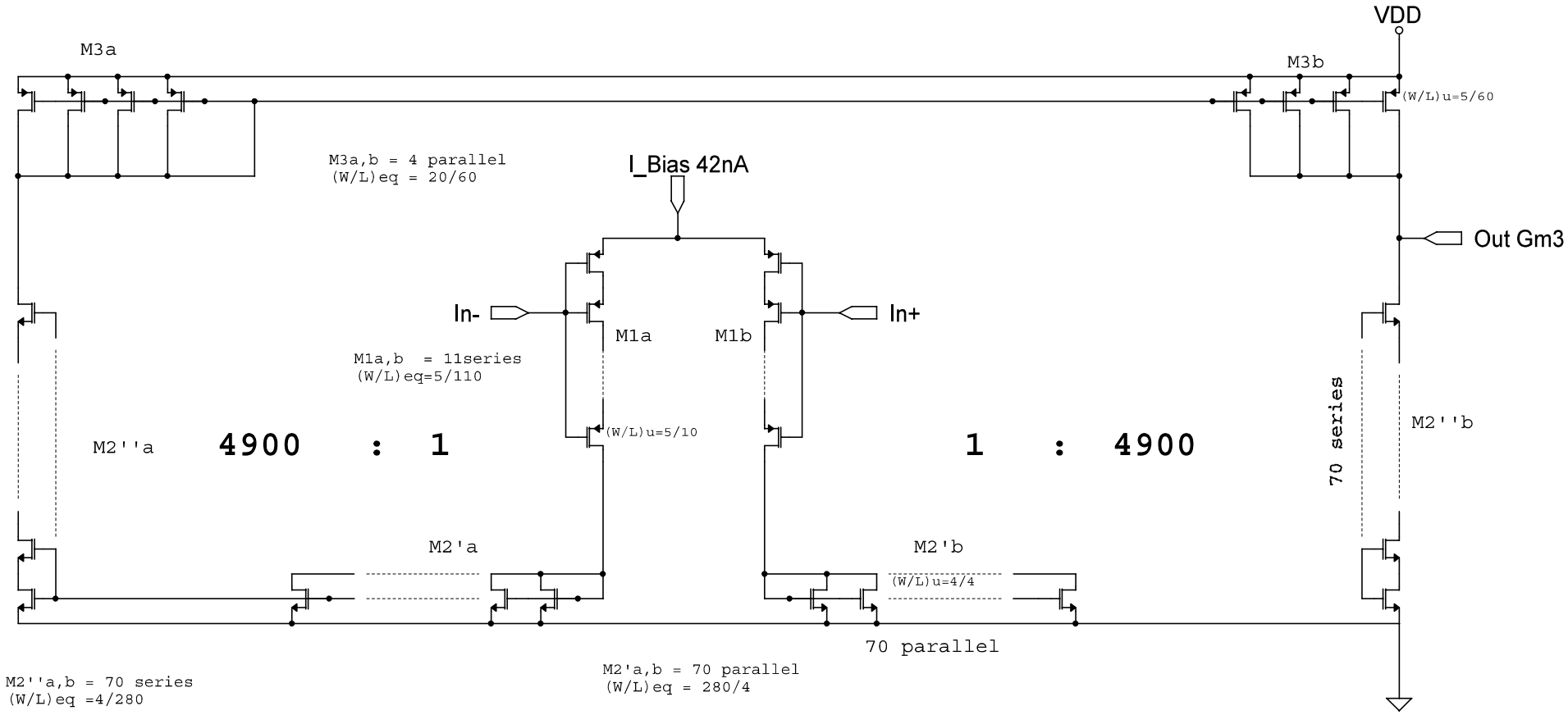
In this annex, circuit schematics are shown for each of the OTAs that compose the bandpass filter-amplifier of Fig.5.1 as well as bias current generation block.



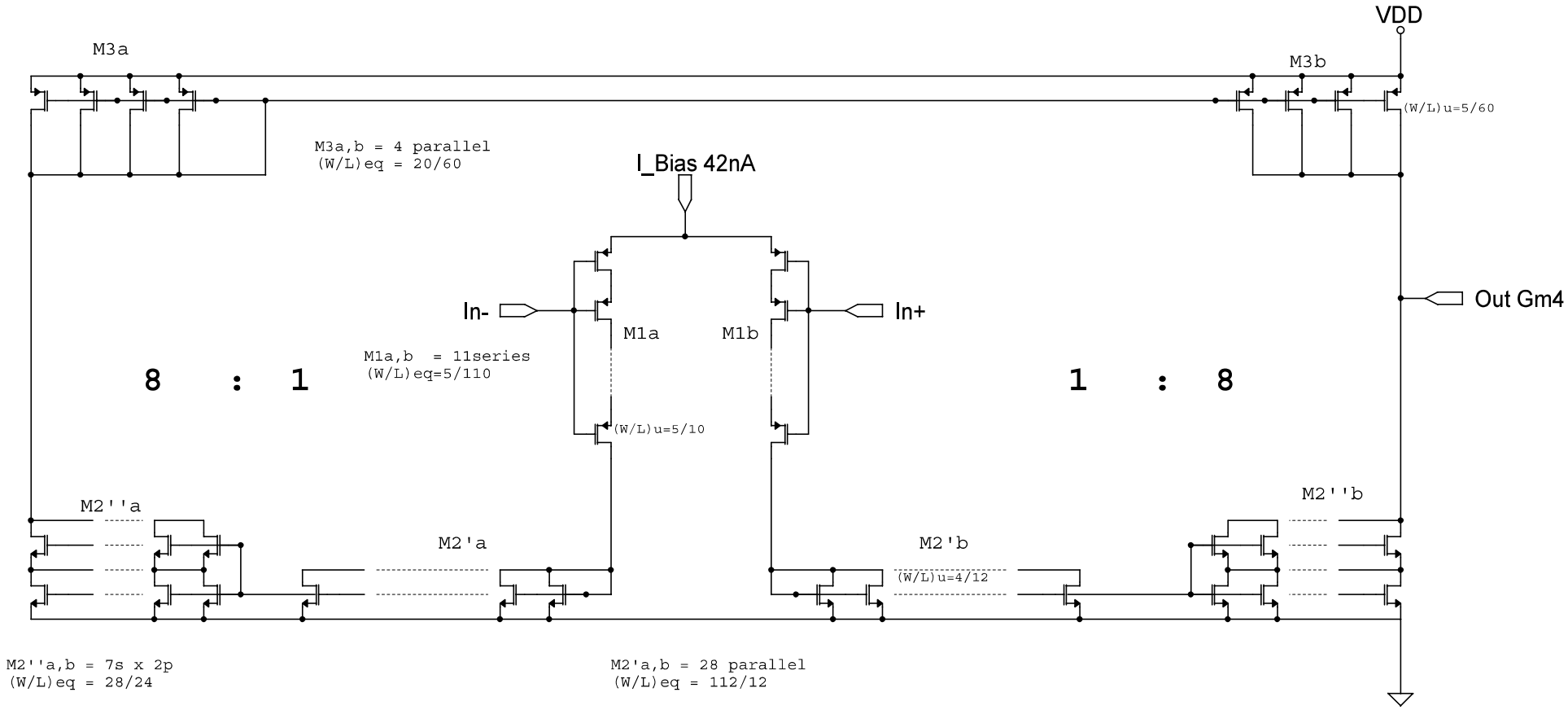
Gm1 Schematic.



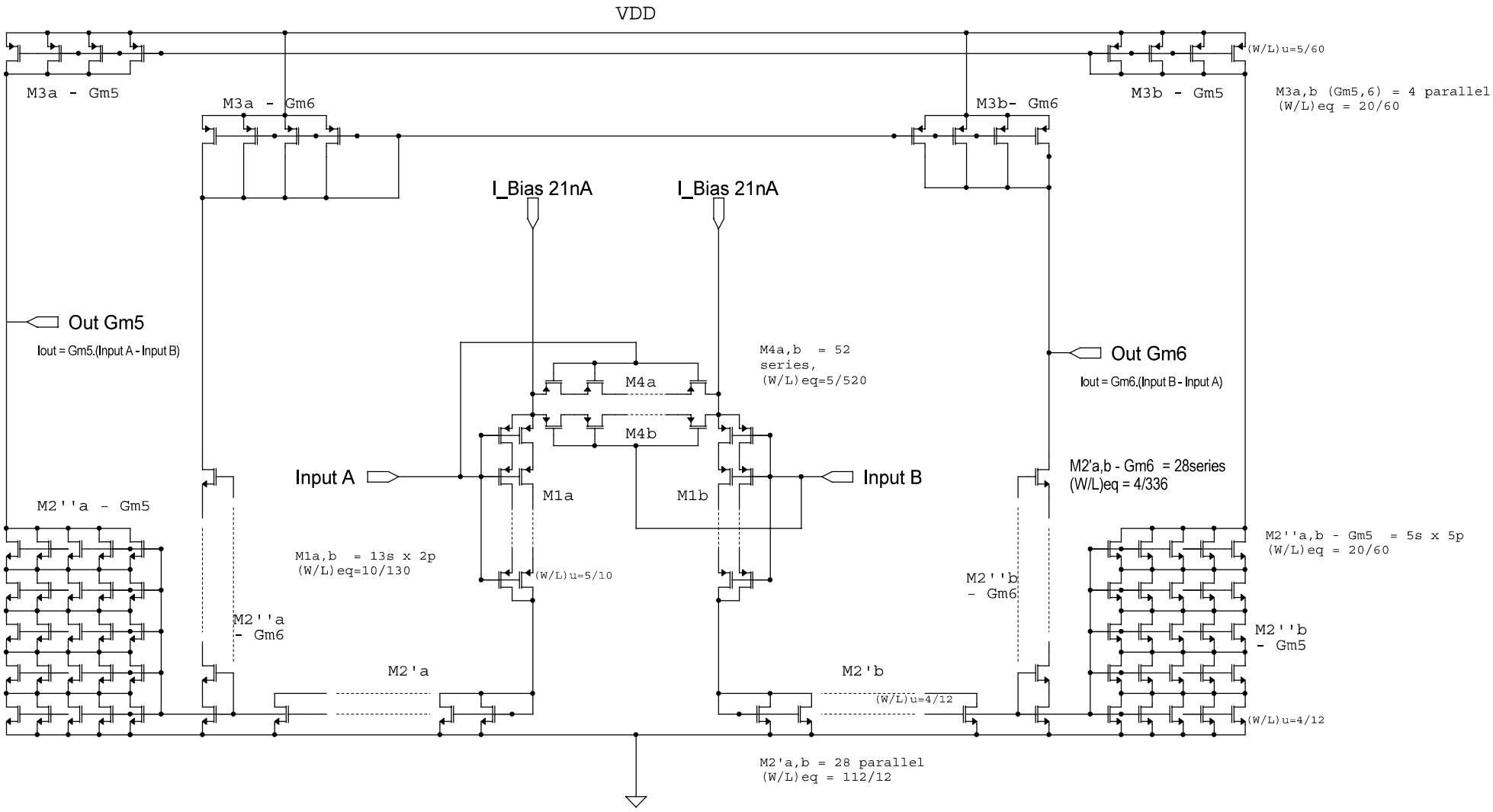
Gm2 Schematic.



Gm3 Schematic.

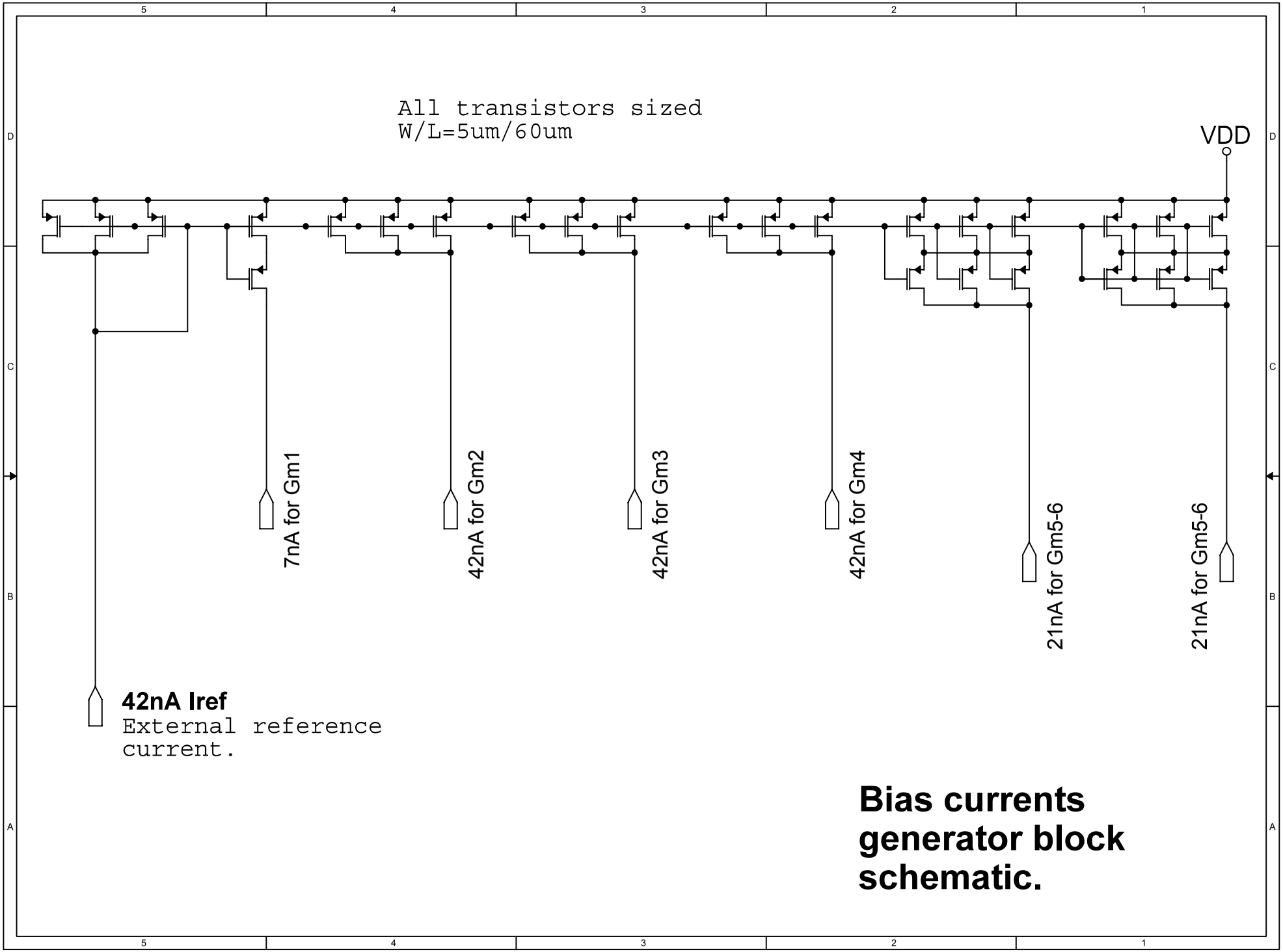


Gm4 Schematic.



Gm5,6 Schematic.

For extra details refer to Table 4.3.


All transistors sized
W/L=5um/60um
VDD
7nA for Gm1
42nA for Gm2
42nA for Gm3
42nA for Gm4
21nA for Gm5-6
21nA for Gm5-6
42nA Iref
External reference current.
Bias currents generator block schematic.