Low Power CMOS RF Amplifiers for Short Range Wireless Links:

A Design Tool and its Application.

By

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Abstract

This thesis is mainly focused on the implementation of low-power integrated power amplifier. The main keywords are; tool for CMOS design, wireless short range devices and low current consumption.

A tool that explores the design space of basic RF circuit blocks is presented. The tool takes advantage of the application of a MOS transistor model continuous (ACM model) in all inversion levels (weak to strong inversion). The performance of the circuit is analyzed in the I_D-g_m/I_D plane and our tool shows the existence of an inversion level that provides an optimum in the power consumption for a given voltage gain and frequency.

Examples are presented showing comparison of the performance of different technologies and circuits' architectures as well as we will show that the evaluation of the effect of parasitic elements can be easily done. The tools estimations are checked against simulations using the foundry provided BSIM3v3 model showing very good agreement.

Finally, the tool is tested in the design of two power amplifiers at 910 MHz in 0.35µm CMOS technology where one of them was designed for wireless short distance devices. Additionally, characterization and experimental results for these amplifiers are presented.

Resumen

Esta tesis esta orientada hacia la implementación de amplificadores de potencia de bajo consumo. Las palabras claves son: herramienta para diseño de circuitos CMOS, dispositivos para enlaces inalámbricos de corto alcance y bajo consumo de corriente.

Se presentará la herramienta que explora el espacio de diseño de circuitos de RF aplicando un modelo continuo de transistor MOS (modelo ACM) válido en todas las regiones de inversión (inversión débil a fuerte). El desempeño del circuito es analizado en el plano I_D-g_m/I_D y este método junto con la herramienta muestra la existencia de un nivel de inversión óptimo que garantiza un óptimo de consumo de potencia para una ganancia de voltaje y a una frecuencia de operación dada.

Son presentados ejemplos que comparan el desempeño de diferentes tecnologías y arquitecturas de circuitos así como también se mostrará que la evaluación de los efectos parásitos es fácilmente realizable.
El desempeño de la herramienta fue probado con simulaciones usando el modelo de transistor MOS BSIM3v3 suministrado por el fabricante, con el cual se ha verificado una buena correlación

Finalmente, la herramienta es probada en el diseño de dos amplificadores de potencia funcionando a 910MHz en tecnología CMOS 0.35µm, el cual uno de ellos es diseñado para formar parte de dispositivos para enlaces inalámbricos de corta distancia.
Adicionalmente, la caracterización y resultados experimentales obtenidos de estos amplificadores son presentados.

Table of Contents

Abstract..... 3
Table of Contents..... 4
Acknowledgements..... 7

CHAPTER 1 ..... **8**
Introduction

1.1 Motivation and Research Goals..... 8
1.2 Thesis Organization..... 9
1.3 References..... 10

CHAPTER 2 ..... **11**
The Wireless Link & Power Transmission Issues

2.1- Radio Design Considerations..... 11
2.1.1 Frequency Bands and Data Rates..... 12
2.1.2 Channel Model and Range..... 13
2.1.3 Radio System Parameters (Sensitivity and Dynamic Range)..... 16
2.2- Key Topic of CMOS RF Power Amplifier..... 18
2.2.1 Linearity..... 20
2.2.2 Efficiency..... 21
2.2.3 Filtering and Matching 22
2.3- References..... 25

CHAPTER 3 ..... **27**
MOS Transistor Model for RF IC Design

3.1 Background 27
3.1.1 The ACM Model..... 30
3.1.2 The g_m/I_D ratio..... 31
3.1.3 Non Quasi-Static Boundary..... 32
3.2 Tool Modelling Approach 35
3.3 Two Port Network Models..... 38
3.3.1 Transformations to study others architectures..... 39
3.4 References..... 41

CHAPTER 4 ..... **43**
Tool for RF CMOS Design

4.1 Design Exploration Process 43
4.2 Matlab Exploration Tool 44
4.2.1 Formalism..... 44
4.2.2 Example1..... 45
4.2.3 Example 2..... 47
4.2.4 Example 3..... 48
4.3 Tool User Interface 50
4.4 Design Examples..... 55
4.4.1 Optimum Amplifier Stage..... 55

4.4.2 Power Amplifier of a low power short range transmitter..... 57
4.4.2.1- Calculus…….. 61
4.5 References…… 63

CHAPTER 5..... 64
Layout and Experimental Results

5.1 Layout ……..... 64
5.2 Test Setup ……..... 65
5.3 Optimum Amplifier Stage .....……..... 66
5.3.1 Measurement and Simulation Conditions …… 68
5.4 Power amplifier of a low power short range transmitter..... 71
5.4.1 Measurement and Simulation Conditions…… 73
5.6 References ……..... 75

CHAPTER 6..... 76
Conclusion

6.1 Conclusions……... 76
6.1.1 Performance ……... 76
6.1 Future Work…… 77

Appendix A……..... 78
Introduction to Volterra Series & Effects of Nonlinearity

A.1 Volterra Series Representation…… 78
A.2 Output from Volterra Kernels…….. 80
A.3 Applicability of Volterra Series……... 81
A.4 The Harmonic Input Method……... 81
A.4 Gain Compression……... 83
A.5 References ……... 84

Appendix B…… 85
Power Series Expansion of The Drain Current

B.1 Nonlinearity coefficients …… 85

Appendix C…… 88
Analytic Solution of the Optima

C.1 Formalism…… 88
C.2 Algorithm……..... 89
C.3 Cardana's solution…….... 92
C.4 Variations due to the load impedance…….. 92

Appendix D……..... 94
Bond wires and Bond Pads

D.1 Bond Pads ……..... 94
D.2 Bond Wires…….. 97

D.3 Guard Ring……..... 97

Appendix E……..... 99
Non Quasi-static Frequency Boundary

E.1 Relationships Between f_{NQS} and f_T……..... 99
E.2 Effect of the slope factor n…….. 100

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Chapter 1

Introduction

Chapter Overview - *In this chapter, an introduction with motivations and objectives of this thesis are presented. In addition with this, design goals for the project are discussed to provide a context for this research.*

1.1- Motivations and Research Goals

Nowadays, the development of low-cost, low-power radiofrequency (RF) devices grows up rapidly, and those systems are characterized by short range links (usually below 100m) and reduced power consumption (since the devices are powered with batteries). However, these applications have a few systems challenges to resolve from current consumption point of view.

In this way, the Microelectronic Team has started a development task toward the issue Wireless Sensor Network and having strong experience to develop low power devices, this thesis has focus on reuse these ideas and past experience to explore their possible applicability in the RF field.

It is known that optimum power consumption of analog circuits can be reached in the moderate inversion region [1], where is obtained a good trade-off between a high g_m/I_D and a non-excessive transistor size (translated to medium parasitic capacitances values). Traditionally the operation at this optimum was restricted to low frequency applications, since the transconductance values required for operation at RF implied currents that, in order to operate in moderate inversion, lead to enormous transistor sizes.

These big transistors would imply high parasitic capacitances that would jeopardize the advantage of an increased g_m/I_D ratio in moderate inversion. However, what is "low" frequency and "high" frequency is technology dependent. Particularly, in current deep sub micron technologies, the reduction of parasitic capacitances and the increase of the current drive by the increase of the gate oxide capacitance per unit area, make that RF frequencies are, in fact, "low" frequency. This idea, that this work exploits, has been also advanced in works such as [2,3,4].

The design of RF devices involves a tradeoff of several performance parameters such as linearity, distortion, gain power, gain voltage and current consumption. In this work we present a design tool oriented toward CMOS RF devices. It is a tool which can be used either to design amplifiers, obtaining an optimum design and showing the trade off between amplifier's gain and power consumption, or to evaluate the performance of a particular technology at a desired frequency.
The core of the tool estimator of RF analog CMOS circuits' behaviour is based in the MOS transistor model ACM [4] and the tool engine is based on MATLAB

With this tool it has been checked the good performance of a 0.35µm technology at 910MHz and it has been designed two power amplifier prototypes, showing optimum behaviour from current consumption point of view One of these amplifiers was made in order to boost up power from a VCO used as core device which conform a node of a wireless sensor network.

Finally, it is important to underline that some results presented in this work have been also reported in the following arbitrates conferences:

- L.Barboni , R.Fiorelli, F.Silveira *"A Tool for Design Exploration and Power Optimization of CMOS RF Circuits Blocks "* Paper presented to ISCAS 2006 –Island of Kos -Greece

- L.Barboni , R.Fiorelli, F.Silveira *"Design and power optimization of CMOS RF Blocks operating in the moderate inversion region*" 18th SBCCI. - September 2005 - Florianopolis, Brazil.

- L.Barboni ,R.Fiorelli, F.Silveira *"Diseño de Bloques de RF de Bajo Consumo en Inversión Débil y Moderada"* XI IBERCHIP Workshop – Marzo 2005

1.2-THESIS ORGANIZATION

This thesis consists of six chapters as follows:

Chapter 1 – Introduction

Chapter Overview - In this chapter, an introduction with motivations and objectives of this thesis are presented. In addition with this, design goals for the project are discussed to provide a context for this research

Chapter 2 – The Wireless Link & Power Transmission Issues

Chapter Overview - In order to understand the wireless link behaviour and what will influence link performance; this chapter covers some fundamentals issues related to the wireless system design.
A challenge for wireless sensor network is energy. Designing systems with long lifetimes will be necessary due to the energy resources available will be limited and replacing batteries is not a practical option. Therefore, to reduce energy consumption, we should investigate some fundamentals of the transmission path and the trade off between environmental factor, output power and maximum useful range.
Finally, this chapter ends by including a review of RF power amplifier class A,B and C because when we consider battery-operated devices, the power efficiency of the amplifier is definitely a main concern.

Chapter 3 - MOS Transistor Model for RF IC Design

Chapter Overview – Modeling of devices is a key step into design processes because without good models, it becomes difficult to analyze and predict circuit behaviour. The purpose of this chapter is to study a compact high-frequency MOSFET model and how it could be implemented in our tool. The model used for the MOS transistor is the ACM model which was presented by Galup-Montoro et al. [4] and as we will see throughout this chapter, this model has desirable characteristics from the designer point of view.

Chapter 4 - Tool for CMOS RF Design

Chapter Overview – This chapter begins with an overview of the tool developed as main goal of this work, which can be used to design amplifiers obtaining an optimum from current consumption point of view and showing the trade off between amplifier's gain and power consumption as well as to evaluate the performance of a particular technology at a desired frequency.
At the end, two different circuits are presented as design examples implemented in order to validate the results of against simulations and measurements

Chapter 5 - Layout and Experimental Results

Chapter Overview - This chapter describes the layout of the circuits and presents the results obtained from measuring prototypes. Performance of each power amplifiers is characterized as well as simulations of the synthesized circuits are presented.

Chapter 6 - Conclusions

Chapter Overview - Conclusions and ideas for future research are presented.

Furthermore, we present five appendices as follow:

Appendix A - Introduction to Volterra Series & Effects of Nonlinearity

Appendix B - Power Series Expansion of the Drain Current

Appendix C - Analytic Solution of the Optima

Appendix D - Bond Wires, Bond Pads & Guard Rings

Appendix E- Non Quasi-static Frequency Boundary

1.3- REFERENCES

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Chapter 2

The Wireless Link & Power Transmission Issues

Chapter Overview – *In order to understand the wireless link behaviour and what will influence link performance, this chapter covers some fundamentals issues related to the wireless system design.*
A challenge for wireless sensor network is energy. Designing systems with long lifetime will be necessary due to the energy resources available will be limited and replacing batteries is not a practical option. Therefore, to reduce energy consumption, we should investigate some fundamentals of the transmission path and the trade off between environmental factor, output power and maximum useful range.
Finally, this chapter ends by including a review of RF power amplifier class A,B and C because when we consider battery-operated devices, the power efficiency of the amplifier is definitely a main concern.

2.1- RADIO DESIGN CONSIDERATIONS

A model of a wireless link is shown in Figure 2.1. It includes a transmitter with antenna (whose antenna's gain is G_{Tx}), a transmission path with multipath phenomenon caused by reflection, diffraction and scattering, (path loss PL(dB)) and finally, the receiver with antenna (whose antenna's gain is G_{Rx}).
The antenna transforms the power delivered from the power amplifier into electromagnetic energy which radiates to the receiver. Therefore, to reduce energy consumption, we should investigate some fundamentals of the transmission path and the tradeoff between environmental factor, output power and maximum useful range of communication.

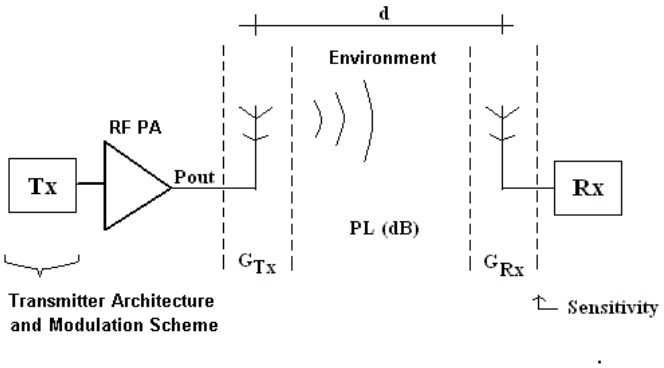

Figure 2.1: Description of a basic radio link model

In the traditional wireless link, the transmission distance is large (>100 m), so that the transmission energy is dominant in the total consumption energy. However, in many recently proposed wireless sensor network [1][2] the average distance between nodes is usually below 10m and it is characterized by low-power transmission (less than 10dBm)

In this situation many scenarios have been proposed for distributed wireless sensor network such as tracking, medical devices (patient monitoring), location sensing, machine-mounted sensing, climate control and much more. As a result, the growing demand in wireless sensor devices has created the necessity to research into energy-efficient protocols and architectures, which have been emerging and improving since years ago.

As an example, the IEEE Std. 802.15.4 [4][5] has a focus in wireless sensors and actuators for the industry in general in order to provide extremely low-power, low-rate and low-cost wireless connectivity. These features enable applications in the fields of industrial, agricultural, vehicular, residential and medical sensors.

In the next Table 2.1, we show a brief overview of the characteristics of the standard 802.15.4 compared with the standards Bluetooth and 802.11b.

	802.11b	Bluetooth™	Low Rate - 802.15.4
Useful Range	~100 m	~10 - 100 m	< 10 m
Data Rate	~2 - 11Mb/s	1Mb/s	< 0.25Mb/s
Power Consumption	Medium	Low	Ultra Low: The majority of IEEE Std. 802.15.4 devices are expected to operate with transmits power between -3dBm and 10dBm
Neighbours Distance	Larger	Smaller (<100m)(1)	Smallest (< 20 m) (1)

Table 2.1: The 802.15.4 allocation compared with others standards from wireless parameters point of view

(1) This range is strongly dependent on the environment (proximity of concrete wall, outdoor or indoor, etc.)

In the next section we present an overview of the features that characterize the standard 802.15.4.

2.1.1-Frequency Bands and Data Rates

The IEEE Std. 802.15.4 PHY (Physical Layer) are specified for operation in 27 channels. Channel 0 through 10 span frequencies from 868 MHz through 928MHz and upper band reside in frequencies from 2405MHz to 2480 MHz .More specifically:
-channel 0: 868-868.6 MHz
-channe1 1-10: 902-928 MHz (central frequency Fc = 906 + 2 (k – 1) in MHz, for k = 1, 2, ..., 10)
-channel 11-26: 2.4 -2.4835GHz

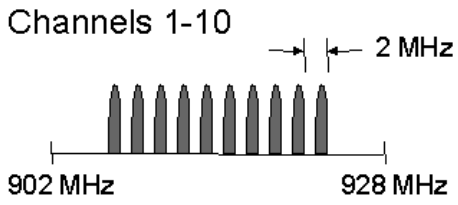

Figure 2.2: 915 MHz PHY Operating Frequency Bands

Due to the physical characteristics of each band and the regulations where they are used, the IEEE Std. 802.15.4 specifies different data rates and modulation. [4]
A detailed explanation of these parameters is shown in the next table.

Frequency (MHz)	Frequency Band (MHz)	Spreading Parameters		Data		
		Chip rate (1) (kchip/s)	Modulation	Bit Rate (kb/s)	Symbol rate (ksymbol/s)	Symbols
868/915	868-868.6	300	BPSK	20	20	Binary
	902-928	600	BPSK	40	40	Binary
2450	2400-2483.5	2000	O-QPSK	250	62.5	16-ary Orthogonal

Table 2.2: Frequency bands and data rates

(1) In direct sequence spread spectrum technologies such as CDMA and DSSS, it is the number of bits per second (chip per second) used in the spreading signal. The chip rate is usually several times the information bit rate.

Others 868MHz/ 915 MHz Band Specifications

- Spreading code is conformed by a 15-chip M-sequence. Chip modulation is based on BPSK at 0.6/0.3 Mchips/s (M-sequence is a technique like codes of Walsh for creating orthogonal sequences. It is often used due to it can be created using a shift register with M feedback –taps)
- Transmit Power: Capable of at least –3dBm. Typical 0 dBm
- Transmit Center Frequency Tolerance: ± 40 ppm
- Receiver Sensitivity: -92 dBm or better (1% Packet Error Rate)

As we can see, only a boundary of levels of delivered power from the antenna to the environment has been specified. Thus, each system designer has to have some fundamentals knowledge of the radio related parameters which influence overall system performance and how much output power should be specified for each application and range.

2.1.2-Channel Model and Range

The ratio of the power at a receiving antenna to the power at a transmitting antenna is given, in free space, by the Friis radio link model [5][6]:

$$\frac{P_R}{P_T} = G_T G_R \left(\frac{c}{4\pi f d} \right)^2 \tag{2.1}$$

Where:

P_R: power at the receiving antenna
P_T: power at the transmitting antenna
G_R,G_T are the power gains of receiving and transmitting antennas respectively
c: is the speed of light
d: distance between antennas
***f*:** frequency

This same equation can be expressed as a basic path loss PL(dB) in decibel form:

$$P_R - P_T = G_T + G_R - PL(dB) \tag{2.2}$$

Where:

$$PL(dB) = 32.44 + 20\log(d_{Km}) + 20\log(f_{MHz}) \tag{2.3}$$

Where the subindex indicates units. This notation will be applied in the rest of the chapter.

The antenna is included as the parameter antenna gain. This could be interpreted as the antenna's ability to transform output power into radiated energy. According with the bibliography [1], the antenna gain is generally proportional to physical size. The fundamental relation in antenna theory is:

$$G = \frac{4.\pi.A_f}{\lambda^2} \tag{2.4}$$

Where:
A_f : is the effective area
$\boldsymbol{\lambda}$: is the wavelength

For low power radio devices, the loop antenna etched on the PCB has a typical effective gain of approximated 20dB to -25dB [1]
To put things into perspective the effective area to achieve an antenna gain of 0dB is A_f =0.0086 m^2 (approximated 0.093m X 0.093m) for the 915MHz band (λ= 0.328m).
Most useful applications would be unpractical with such a large antenna and they are usually implemented with a much smaller antenna which has a gain below 0dB. Thus, it is important to underscore that the antenna actually introduces loss in the transmission budget and it depends on its size.

Although the designer must take care of the antenna selected because of its loss, it is mandatory to study first the useful range characterized by the path loss PL(dB) in order to take care how much energy should be employed to make a good transmission link.

IEEE Std. 802.15.4 specifies that lower frequency bands must be capable of correctly decoding a signal with an input power of –92 dBm (better sensitivity is not prohibited). As an example, for a transmitter rated at –3 dBm, the maximum free space range in approximately:

$$-92dBm-\left(-3dBm\right)=-89dB=-32.44-20\log\left(d_{Km}\right)-20\log\left(915\right)\Rightarrow d=735m \tag{2.5}$$

The value given by Friis radio link formula must be interpreted as the maximum possible received power where this range is for free space, isotropic antennas and perfect power match without interference. There are a number of factors that reduce this received power. These include impedance mismatch at either antenna, propagation effects leading to attenuation and in addition, multipath effect may cause partial cancellation of the received field, as well as the antenna gain would be a factor of attenuation.

A non ideal radio path cause signal attenuation at the receiver if the transmitted signal travels multiple path to the receive antenna. Different paths have different lengths and it may produce receiver signal out of phase, resulting signal attenuation. Moreover, fading appears due to moving object in the proximity of the radio device (people and machinery as example).For example, the wavelength at 915MHz is 0.328m, for this reason actually some short distance-movement in the environment could make fluctuations in the attenuation of the signal at the receiver in the time domain while the environment is moving around. It is better known as fast fading effect.

Multipath phenomenon is caused by reflection, diffraction and scattering that is characterized by a random behaviour. It is important to remark that another factor to take into account is the loss caused by environmental obstacles such as floor, walls, building and windows. The amount of loss depends heavily on the physical characteristic of the object. For ranges between 433MHz to 868MHz, according with the bibliography [1], the most typical losses are summarized in the next table:

Object causing path loss	Typical loss (dB)
Wall (indoor)	10-15
Wall (outdoor)	2-38
Floor	12-27
Windows	2-30

Table 2.3—Typical losses caused by transmission obstacles

Because of multiple factors cause attenuation, a better model than Friis general radio channel model must be introduced [7][8]. For a wide variety of channels, experimental measurements of the received power suggest a functional dependence for path loss given by:

$$P_{\text{Re}ceived}(dBm) = P_{Transmit}(dBm) - PL(dB) - P_{Shadowing}(dB) \tag{2.6}$$

Where the path loss component is given by:

$$PL(d) = 10\log\left(\left(\frac{4\pi f}{c}\right)^2 d^n\right) \tag{2.7}$$

n: range from 1.2 to 6 and it depends on the propagation environment, i.e., rural, urban and the type of construction material, type of interior and location within building. For example:
n=2: implies free space propagation (Friis model)
n=1.2: contrary to our intuition may suggest, values of *n* below than free space propagation (n=2) could be possible due to waveguide effects. It is a kind of waveguide created by concrete walls and flats in a build environment.
$\mathbf{P_{Shadowing}}$: is a zero mean log-normally distributed random variable with a standard deviation that depends on the environment between transmitter and receiver. This parameter must be estimated by taking measurements at the desired frequency and it is an empirical way to take into account all phenomena that can not be modeled by the equation (2.7)

In the figure 2.3 we compare the effects of the parameter *n* in the expression (2.7)

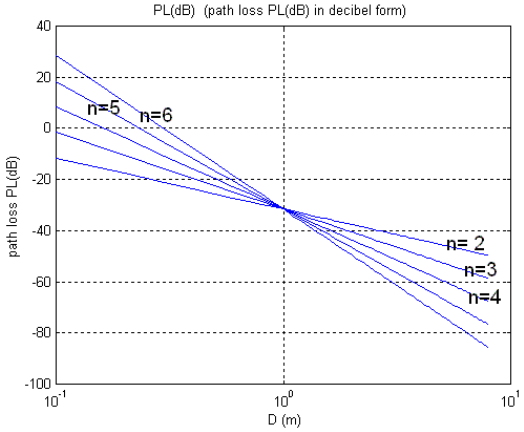

Figure 2.3: Path loss behaviour in decibel form at 915 MHz as function of the parameter *n*

Another expression of the family (2.6) and (2.7) to express the link loss suitable for Link Budget Analysis could be written as**:**

$$PL(d) = PL(do) + 10\,n\log\left(\frac{d}{do}\right) + X_\sigma \tag{2.8}$$

Where:

PL (d): is the path loss in dB at distance d
PL (do): is the know path loss at the reference distance do (it is measured at the frequency of interest)
n: is an exponent depending on the propagation environment. This parameter is very sensitive and range from 1.2 to 6 could be expected as we discussed previously.

$\mathbf{X_\sigma}$: is the variable representing uncertainty of the model or variance obtained due to the effect of shadowing, diffraction and scattering. A model that has often been used to explain variations of the signal amplitude in a multipath fading environments is the Lognormal Distribution.

Coming back to the IEEE Std. 802.15.4, the channel path loss is assumed as a class of the family model explained in (2.8), where the standard assume that 868/915MHz bands exhibit similar behaviour to 2.4GHz band. So that, according to the IEEE Std. 802.15.4, the losses can be expressed as follows:

$$PL(dB) = 40.2 + 20\log(d_m) \qquad \text{for } d_m < 8m \qquad (2.9)$$

$$PL(dB) = 58.5 + 33\log\left(\frac{d_m}{8m}\right) \qquad \text{for } d_m > 8m \qquad (2.10)$$

In the figure 2.4 we compare the difference between the free space path loss model (from equation 2.3) and the IEEE Std. 802.15.4 channel path loss model (represented by equations 2.9 and 2.10).

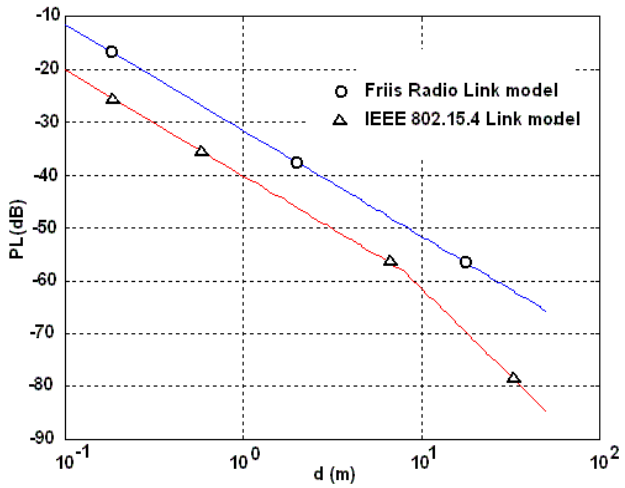

Figure 2.4: Path loss in decibels at 915 MHz

In the Table 2.4 we compare the PL(dB) estimated using different models @ 915MHz

D (m)	Free Space Path Loss (dB)	PL (dB) expression (2.7)			IEEE Std. 802.15. 4 Channel Path Loss (dB)
		n=3	n=4	n=5	
1	31.7	31.7	31.7	31.7	40.2
10	51.7	61.7	71.7	81.7	61.7
50	65.6	82.6	99.6	116.6	84.8

Table 2.4—PL(dB) estimated with different models.(@ 915MHz)

These models are simple and suitable for computer implementations because the environmental database is unnecessary, but, due to the model simplicity, great accuracy could not be expected. We can see the enormous dependency of the path loss with the environment. For this reason, it is important that we study some parameters that the systems must be capable to satisfy in order to maintain a good link budget in a worst case.

2.1.3-Radio System Parameters (Sensitivity and Dynamic Range)

We can see the power levels of the systems in the figure 2.5 (figure 4 in [1]), where the noise floor is the total average noise available at the input of the system.

Sensitivity is the minimum received power that results in a satisfactory BER (bit error rate, usually $1x10^{-3}$) that imply a satisfactory SNR_{min} in the receiver. The difference between received signal power and sensitivity is a margin also known as headroom. The headroom varies with time due to a number of factors such as path loss and antenna efficiency, as we discussed previously.

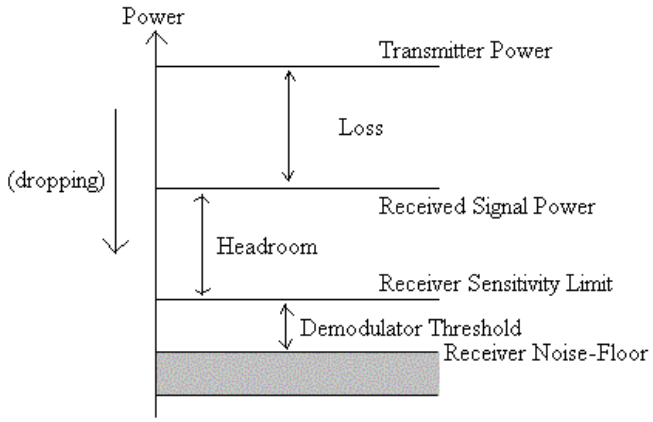

Figure 2.5: Transmission link budget

Another important parameter is the dynamic range which is defined as the maximum received power variation at the receiver input which results in a correct demodulated signal. In others words, this means that the signal of interest may vary between the sensitivity and the sensitivity limit plus the dynamic range.
Thus, the dynamic range requirements for the receiver are calculated by the maximum and minimum received signal levels experienced at the receiver.
To calculate the maximum signal, assume a minimum transmit-receive separation distance and no shadowing losses. The maximum received power is then given by:

$$P_{R,MAX}(dBm) = P_T(dBm) - PL(dB)\big|_{d\,\min} \tag{2.11}$$

Where $P_T(dBm)$ represents the power transmitted.
Conversely, to calculate the minimum received signal, we assume a maximum transmit-receive distance and a maximum of shadowing loss. The minimum received power is thus given by:

$$P_{R,MIN}(dBm) = P_T(dBm) - PL(dB)\big|_{d\,\max} - P_{Shadowing}(dB) \tag{2.12}$$

The worst-case shadowing loss $P_{Shadowing}(dB)$ (X_σ in equation 2.8) must be assumed according with [9], in a typical situation 10dB. It should be taken account in our link analysis.

The difference between these two values determines the dynamic range requirements for the receiver. This is:

$$DR = P_{R,MAX} - P_{R,MIN} \tag{2.13}$$

In the next Table 2.5 we compare the distance where the value of sensitivity specify in the IEEE Std. 802.15.4 (-92dBm) is achieved with different output power from -30dBm to 3dBm, at 915MHz and for two cases:

case A: without shadowing
case B : assuming 10dB of shadowing

For this estimation, we use the IEEE Std. 802.15. 4 Channel Path Loss.

Output Power (dBm)	-30	-20	-10	-1	0	1	2	3
Case A: D (m)	10.2	20.5	41.2	77.3	82.8	88.8	95.2	102.2
Case B: D (m)	3.9	10.2	20.5	38.5	41.2	44.2	47.4	50.8

Table 2.5—Distance (m) at 915MHz where the value of sensitivity -92dBm takes place as function of output power

2.2- KEY TOPICS of CMOS RF POWER AMPLIFIER

A power amplifier is a circuit for converting DC input power into a significant output power which is driven by an input low-level signal. Each application has its own requirements for frequency, bandwidth, load, power, efficiency and linearity, for this reason no single technique for power amplification or any single transmitter architecture is best for all applications. For instance, it is usual to employ architectures that concatenate progressively amplifiers to boost a low-level signal to the desired output power [10], as we can see in the next figure 2.6.

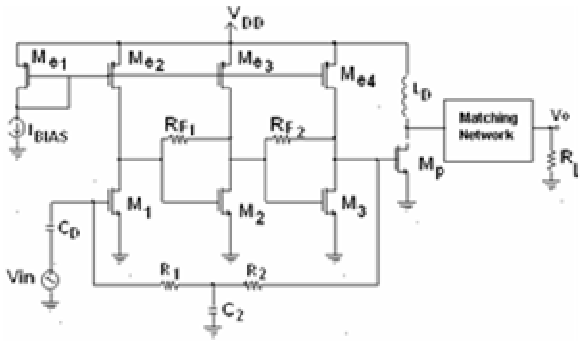

Figure 2.6: A four stage power amplifier (three preamplifiers and power amplifier Mp)

Before describing the tradeoff available to design efficient power amplifiers as we are going to discuss in the followings chapters we will first introduce a review of the architectures. Power amplifiers have different efficiencies depending on their operating conditions

With reference to Figure 2.7, the three most well known classes of power amplifier will be discussed briefly. These amplifiers are distinguished principally by bias conditions and in this general model, the power amplifier is loaded with a matching network which adapt the antenna impedance and into which the PA deliver the output power [13]

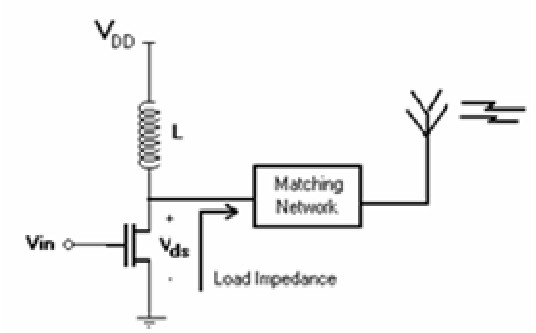

Figure 2.7: Simplified output stage of a power amplifier

Class A: The transistor of the amplifier is biased in order to be always current source so that the amplifier operates quasi-linearly. Consequently, the distortion will be small at the cost of large current consumption reducing the efficiency of the amplifier. This is because the amplifier consumes power when there is not output signal. For resistive load, the maximum efficiency theoretically obtainable is 50%. It is important to underscore that this value of efficiency represent an upper limit and there are additional losses. We can see the drain voltage and current waveform in the figure 2.9

Class B: The transistor is active only half of every cycle so that the amplifier increase the efficiency because but gross departure from linear operation results and a high Q resonator is mandatory in order to filter out the harmonic of the drain current , leaving a sinusoidal drain voltage as class A has. In addition with the Q resonator, in order to obtain an acceptable approximation to a sinusoidal output voltage, it should be mentioned that differential or push-pull configuration is often used. For resistive load, the maximum efficiency theoretically obtainable is 78.5%.We can see the drain voltage and current waveform in the figure 2.9

Class C: The transistor of the amplifier is biased to cause the transistor to conduct less than half the time. The conduction angle of the transistor is smaller than 180 degree. Consequently, the drain current consists of a periodic train of pulses and the amplifier behaves non linearly and the distortion levels are high. As the conduction angle shrinks toward zero, the efficiency approaches 100% but the output power also tends toward zero at the same time.
Mainly, the efficiency can be large, but at the cost of reduced power-handling capability, gain and linearity. We can see the drain voltage and current waveform in the figure 2.9

To summarize, we present the following table 2.6:

Class	Modes	Conduction Angle (%)	Output Power	Maximum Efficiency (%)	Voltage Gain	Linearity
A	Current Source	100	Moderate	50	Large	Good
B		50	Moderate	78.5	Moderate	Moderate
C		<50	Small	100	Small	Poor

Table 2.6: Summary of characteristics of power amplifier classes A,B and C [11]

And the following figures 2.8 and as well as 2.9 show operation point and current wave forms:

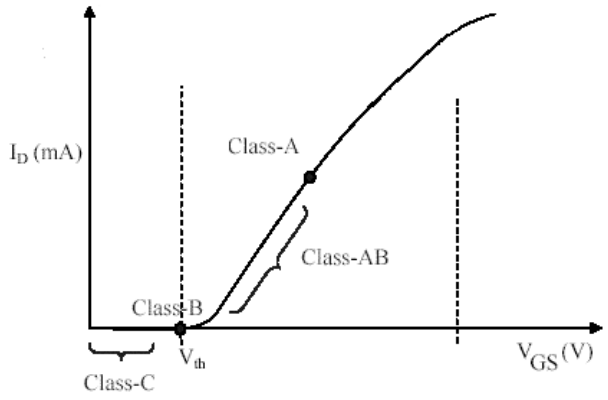

Figure 2.8: Operation point (bias), form figure 2.7 , of Class-A, AB, B and C amplifiers [11]

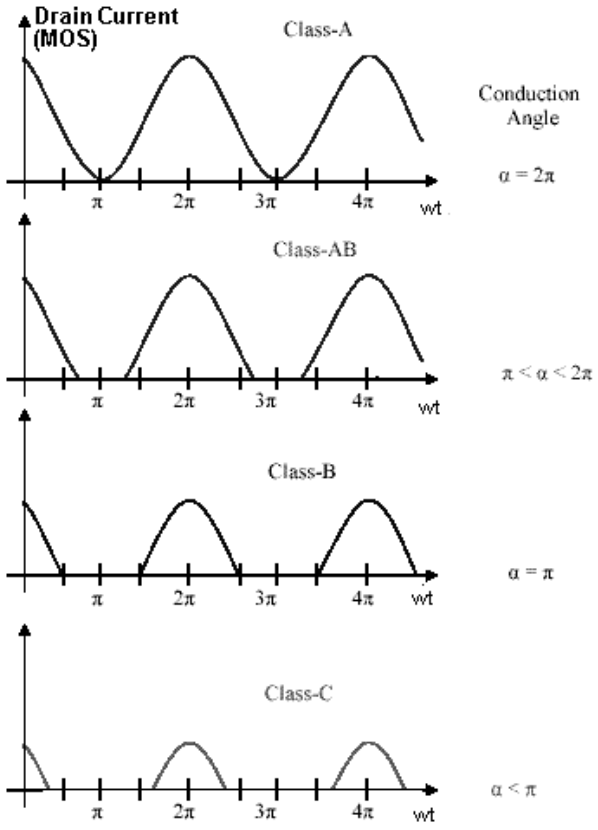

Figure 2.9: Conduction angle relations [11]

2.2.1 Linearity

The need for linear power amplifiers arises in many RF applications. Many systems use frequency or phase modulation techniques for which non linear amplification is allowed.
For example, PSK do not require linear amplification from the modulation technique point of view but classic PSK use abrupt phase transitions or equivalently rectangular data pulses that require linear PAs to minimize spectral regrowth. The resultant sinc-function spectrum spreads signal energy over a fairly wide band-width and it is unsatisfactory for relatively low rates and low power devices.

On the other hand, techniques based on amplitude modulation require linear amplifiers to prevent systems performance degradation from excessive intermodulation distortion.
Nonlinearities cause imperfect reproduction of the amplified signal, resulting in distortion and splatter into adjacent channels and errors in detection.

Moreover and unfortunately the linearity requirement restricts amplifiers to operate below the maximum output power capacity thereby reducing the operation efficiency.

For this reasons, the importance of quantifying linearity and efficiency of power amplifier has provoked a review of different method to simulate and measure distortion. In this way, we can say that linearity is characterized and measured by various techniques depending on the specific signal and application.

A summary of traditional method is presented.

- C/I (*carrier-to-intermodulation-ratio*)
- ACPR (*Adjacent Channel Power Ratio*)
- NPR (*Noise Power Ratio)*
- EVN *(Error Vector Magnitude)*

C/I (*carrier-to-intermodulation-ratio*)

The traditional measure of linearity is the carrier-to-intermodulation ratio (C/I). The PA is driven with two tones carriers of equal amplitudes and nonlinearities cause the generation of intermodulation products at frequencies corresponding to sums and differences of multiples of the carrier frequencies.
The amplitude of the third-order or maximum intermodulation distortion (IMD) is compared so that of the carriers to obtain the C/I

ACPR (*Adjacent Channel Power Ratio*)

Adjacent Channel Power Ratio (ACPR) characterizes how nonlinearity affects adjacent channels and it is widely used with modern shaped-pulse digital signals.
Basically, ACPR is the ratio of the power in a specified band outside the signal bandwidth to the power in the signal. In other words, this parameter defines the amount of power transmitted at a certain offset frequency, compared to the power transmitted in the channel of interest [14].

$$ACPR = \frac{P}{P(\Delta f)} \tag{2.14}$$

Where:
$P(\Delta f)$: Power transmitted at a certain offset frequency (normally the adjacent channel)
P : Power transmitted at the frequency of interest (channel)

NPR (*Noise-Power Ratio*)

It is a traditional method of measuring the linearity of PAs. The PA is driven with Gaussian noise with a notch in one segment of its spectrum. Nonlinearities cause power to appear in the notch and NPR is defined as the ratio of the notch power to the total signal.

EVM (*Error Vector Magnitude*)

Error Vector Magnitud (EVM) is a convenient measure of how nonlinearity interferes with the detection process in modern digital signals such as QPSK or QAM that are typically generated by modulating both I and Q sub carriers. In this way, EVM is defined as the distance between the desired and actual signal vectors.

2.2.2 Efficiency

Drain Efficiency

Efficiency is a critical factor for PA design. Three definitions of efficiency are commonly used.
Drain efficiency is the most common parameter to quantify efficiency and it is defined as the ratio of output power to DC input power

$$\eta_D = \frac{Pout}{P_{DC}} \tag{2.15}$$

In figure 2.10, we can see the behaviour of the drain efficiency that is realized for a particular conduction angle for which the output voltage swing is maximum.

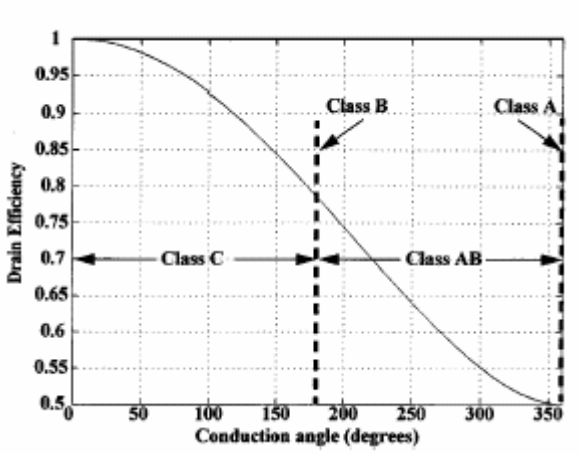

Figure 2.10: Drain efficiency versus conduction angle (load varied for maximum output voltage swing) [11]

The increased efficiency at a reduced conduction angle is achieved at the expense of decreased maximum power output. In the limit a class C PA would be achieved a drain efficiency approaching 100%, but the corresponding output power approaches zero.

Power Added Efficiency

Another measure of efficiency is the *Power Added Efficiency (PAE),* that incorporates the amount of power that is delivered to the input.

$$PAE = \frac{Pout - Pin}{P_{DC}} = \eta_D \left(1 - \frac{1}{G_P}\right) \tag{2.16}$$

Average Efficiency

Signal with time-varying (amplitude modulation) produce time-varying efficiencies. A useful measure of the performance is the average efficiency, which is defined as the ratio of the average output power to the average DC input power.

$$\eta_{AVG} = \frac{Pout_{AVG}}{Pin_{AVG}} = \frac{\int_0^\infty p(P_{out}) P_{out} . dP_{out}}{\int_0^\infty p(P_{out}) P_{DC}(P_{out}) . dP_{out}} \tag{2.19}$$

The average input and output power are found by integrating the product of their variation with amplitude and the probability-density function.

2.2.3 Filtering and Matching

Power amplifier usually employs a matching network between the output transistor and the load. In class A stage if the transistor behaves as an ideal current source, the matching network transform the impedance load in another desired value that usually has no reactive components.

In contrast with the assumption that the drain current and voltage could be assumed sinusoidal, in practice, the large signal operation in class A introduces some harmonics as class B and AB do.
For this reason, for each amplifier, the matching circuits have to include some filtering properties (high Q output tank) in addition with the impedance transformation properties in order to suppress harmonics.
Furthermore, we have studied class AB and B power amplifier with single ended load but another important technique that reduces higher harmonic is the differential output. The single ended to differential conversion as we show in the figure 2.11, reduce the distortion by cancelling even harmonics.

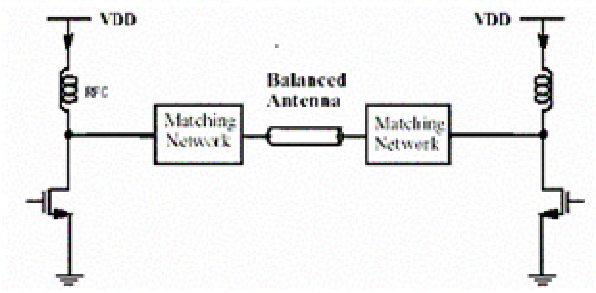

Figure 2.11: Balanced output

Another important topic to underline is related to the maximum power transmission. It does not correspond with the maximum efficiency because if we match according with the maximum power transmission theorem, the power delivered to the load has the same value that is dissipated in the output impedance of the system, reducing the efficiency to 50% from the maximum.
The maximum power transmission theorem show that the power delivered by a voltage source to the load impedance takes maximum value when $Z_o = Z_{load}^*$, where Z_o is the source voltage output impedance and Z_{load} is the load impedance.
This theorem is used when the efficiency is not an important parameter or is not constrained, in comparison with the fact that usually a power amplifier is designed to deliver a specified amount of power into a load with the highest possible efficiency [13].
For example, in a class B stage amplifier, matching network has to be designed in order to get the maximum output voltage swing because it makes the maximum efficiency could be achievable and we do not design in function of the maximum power transmission theorem. For instance, we present the procedure to design a class B amplifier output stage given by the bibliography [13].
Following the notation and the explanation that uses the reference [13], we reproduce the next example:

In a class B amplifier, we assume that the drain current is sinusoidal for one half cycle.

$$i_D = i_o \sin(\omega t) \quad for \quad i_D > 0 \tag{2.16}$$

We find the fundamental component of the drain current:

$$i_{fund} = \frac{2}{T}\int_0^{T/2} i_o \sin(\omega t)\sin(\omega t)dt = \frac{i_o}{2} \tag{2.17}$$

Then, multiply the fundamental current by the load resistance we have the fundamental output voltage:

$$V_o = \frac{i_o}{2} R \sin(\omega t) \tag{2.18}$$

And the output power:

$$P_o = \frac{V_o^2}{2R} \tag{2.19}$$

And the DC power consumed by the DC voltage source is:

$$P_{DC} = 2\frac{V_{DD}^2}{\pi R} \tag{2.20}$$

If the maximum value of the output amplitude is V_{DD} , then the maximum output power delivered to the load resistance is:

$$P_{o\ MAX} = \frac{V_{DD}^2}{2R} \tag{2.21}$$

To conclude:

$$\eta_{MAX} = \frac{P_{o\ MAX}}{P_{DC}} = \frac{\pi}{4} \approx 0.785 \tag{2.22}$$

If the output power delivered to the load resistance R_L is given or specified value P_L , then, the value of the resistance load that maximize the efficiency is given from (2.21)

$$R_{optima} = \frac{V_{DD}^2}{2P_L} \tag{2.23}$$

Finally, we need to develop a network that transforms the resistance from R_L to R_{optima} . After that, we present a numerical example. Let us assume:

- $R_L = 50\ \Omega$
- $V_{DD} = 3V$
- frequency = 910MHz
- P_o=11.69 mW → from (2.23) $R_{optima} = 385\ \Omega$

Thus, the network must transform R_L to R_{optima} as it is shown in the following figure 2.12:
(The software used to create the matching network is SMITH V.191 [15])

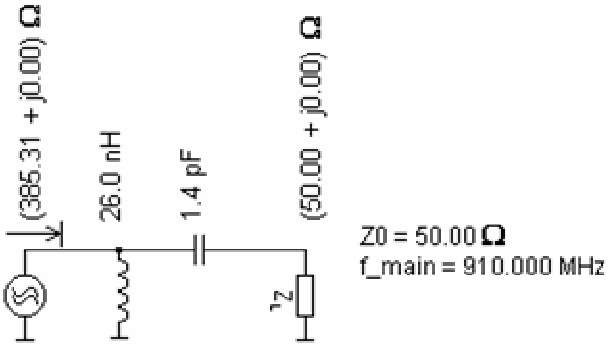

Figure 2.12: Adaptation network of the example

Finally, our amplifier would be schematized in the following figure 2.13:

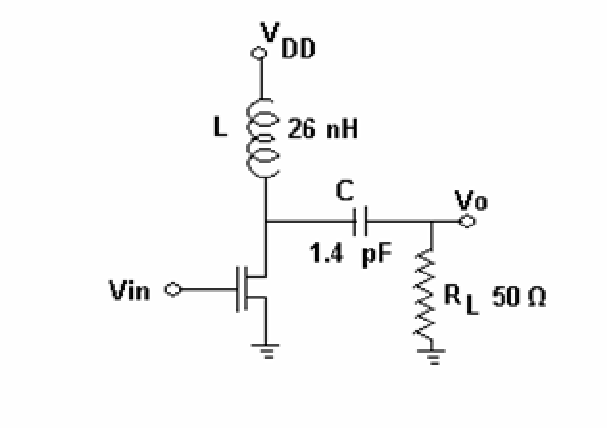

Figure 2.13: Final amplifier of the example

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Chapter 3

MOS Transistor Model for RF IC Design

Chapter Overview – *Modelling of devices is a key step into design processes because without good models, it becomes difficult to analyze and predict circuit behaviour. The purpose of this chapter is to study a compact high-frequency MOSFET model and how it could be implemented in our tool. The model used for the MOS transistor is the ACM model which was presented by Galup-Montoro et al. [3] and as we will see throughout this chapter, this model has desirable characteristics from the designer point of view.*

3.1 BACKGROUND

Design of very-high-frequency circuits is often done by using the so-called "y-parameters" [1][2]. In this section we will first show the general form of this model in order to apply it to the MOS transistor in our tool. First we consider a device that is driven by bias and small –signal voltages at each terminal as shown in Figure 3.1.The effect of each voltage terminal on each current terminal, in the sinusoidal state and using phasor representation are summarized in the followings equations [1]:

$$i_d = y_{dd}v_d + y_{dg}v_g + y_{db}v_b + y_{ds}v_s \tag{3.1}$$

$$i_g = y_{gd}v_d + y_{gg}v_g + y_{gb}v_b + y_{gs}v_s \tag{3.2}$$

$$i_b = y_{bd}v_d + y_{bg}v_g + y_{bb}v_b + y_{bs}v_s \tag{3.3}$$

$$i_s = y_{sd}v_d + y_{sg}v_g + y_{sb}v_b + y_{ss}v_s \tag{3.4}$$

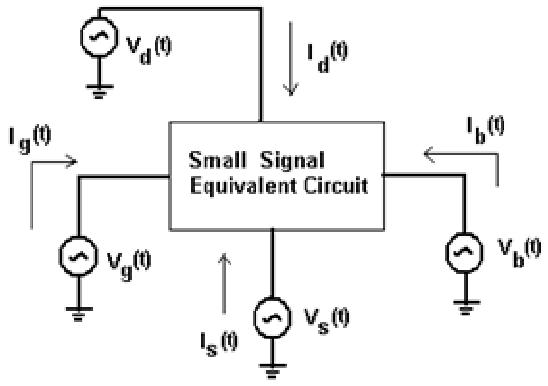

Figure 3.1 The small signal equivalent model terminals (admittance matrix representation)
(Figure adapted from [1], figure 9.13)

Where:
v_g and i_g: gate voltage and gate current
v_d and i_d: drain voltage and gate current
v_s and i_s: source voltage and gate current
v_b and i_b: bulk voltage and gate current

This definition of admittance parameters is standard in circuit theory and it is known as an admittance matrix representation. Assuming the bulk terminal as a potential reference, a fact verifiable directly by writing Kirchoff's law is that this model would be represented as another three ports, three current y-parameter. It could be rewritten in the same form that the bibliography [1] has done, as follows:

$$i_d = -y_{gd}v_{dg} - y_{sd}v_{ds} - y_{bd}v_{db} + y_m v_{gs} + y_{mb}v_{bs} \tag{3.5}$$

$$i_g = -y_{gd}v_{gd} - y_{gb}v_{gb} - y_{gs}v_{gs} \tag{3.6}$$

$$i_b = -y_{bd}v_{bd} - y_{gb}v_{bg} + y_{mx}v_{gb} - y_{bs}v_{bs} \tag{3.7}$$

(From [1], this correspond with equations 9.39a, 9.3.9b, 9.3.9c)

Where the following parameter were defined as:

$$y_m = y_{dg} - y_{gd} \tag{3.8}$$

$$y_{mb} = y_{db} - y_{bd} \tag{3.9}$$

$$y_{mx} = y_{bg} - y_{gb} \tag{3.10}$$

The above set of equations can be represented by the circuit of Figure 3.2. Each y_{gs}, y_{gd}, y_{sd}, y_{bs}, y_{bd}, y_m, y_{mb}, y_{mx} and y_{gb} are represented only symbolically for the moment. We will derive actual parameters and represent them in circuit form, in the following sections. At the moment, a four port fictitious device have been studied and figure 3.2 shows the configurations of y-parameter networks to represent equations (3.5) to (3.10).

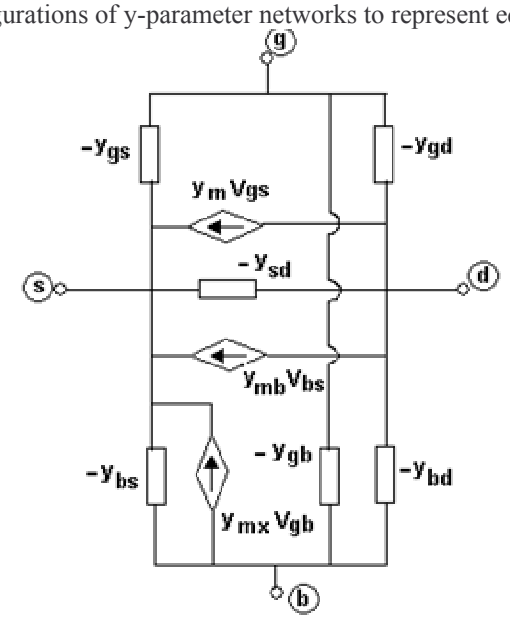

Figure 3.2 A general model for four terminal MOS transistor device according with equation (3.5 to 3.10) (Figure adapted from [1], figure 9.17)

Remember that the y- parameters for the moment have been represented only symbolically.

As a special case of this model is the simple quasi-static small-signal model of the intrinsic part of the MOS transistor that is shown in Figure 3.3, which has the same topology that has just shown in figure 3.2. This is the complete quasi static small signal model for the MOS transistor, where capacitance effects of the drain, source, substrate and gate has been taken into account.

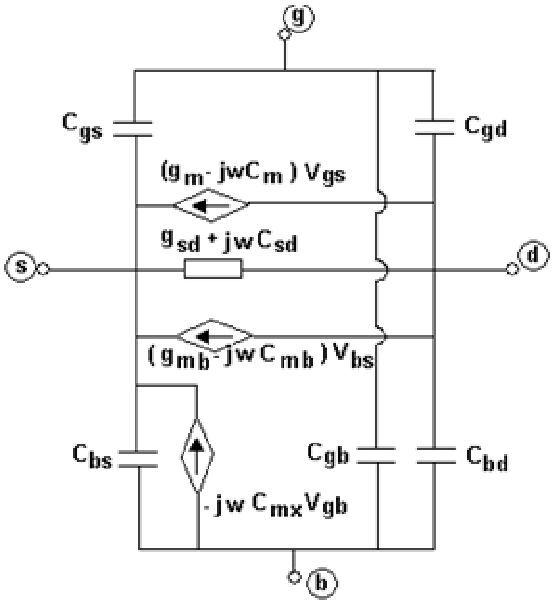

Figure 3.3 A simple quasi-static intrinsic small-signal model for the MOS transistor
(Figure adapted from [1], figure 9.5)

In order to define the quantities that match the physical model which has just been shown in the figure 3.2 with the figure 3.3, the following quantities have been defined in the literature [1];

$$-y_{gd} = j\omega C_{gd} \tag{3.11}$$

$$-y_{gs} = j\omega C_{gs} \tag{3.12}$$

$$-y_{bd} = j\omega C_{bd} \tag{3.13}$$

$$-y_{bs} = j\omega C_{bs} \tag{3.14}$$

$$-y_{gb} = j\omega C_{gb} \tag{3.15}$$

$$-y_{sd} = g_{sd} + j\omega C_{sd} \tag{3.16}$$

$$y_m = g_m - j\omega C_m \tag{3.17}$$

$$y_{mb} = g_{mb} - j\omega C_{mb} \tag{3.18}$$

$$y_{mx} = -j\omega C_{mx} \tag{3.19}$$

The equations (3.11) to (3.15) use five intrinsic capacitances: $C_{gd}, C_{gs}, C_{bd}, C_{bs}, C_{gb}$ and for equation (3.16) to (3.19) three transcapacitances and a capacitance have been used and included as: C_m, C_{mb}, C_{mx} and C_{sd}.

Then, the above relations require no less and no more than six intrinsic capacitances and three transcapacitances:

$$C_{gd}\ ,\ C_{gs}\ ,\ C_{\mathrm{bd}}\ ,C_{bs}\ ,\ C_{gb}\ ,C_m\ ,C_{mb}\ ,C_{mx}\ ,C_{sd} \tag{3.20}$$

To provide more feeling about the model, we can say that each capacitance and transcapacitance represents the effect of each terminal voltage called K, on each terminal current called L , where K and L can be Drain, Gate , Source or Bulk and it is not necessary a real capacitance.
For instance, we may have tendency to think of C_{gd} and C_{dg} as the capacitances of two terminal capacitors between drain and gate but such interpretation is not correct. The C_{gd} represents the effect of the drain on the gate and C_{dg} represents the effect of the gate on the drain in terms of charging currents.

On the other hand, usually C_{mx} is very small and will be unimportant in most practical cases and note also that in saturation some capacitances get value zero due to the drain voltage does not influence the device charges. That is expressed as:

$$C_{gd} = C_{bd} = 0 \tag{3.21}$$

As well as the capacitance:

$$C_{sd} = 0 \tag{3.22}$$

Finally, it is important to remark that the model that has been presented is a quasi-static model (QS), and is based on the hypothesis that the charge in the channel can reach the balance instantly after applying electrical stimulus. However, the limitation of the QS model is well known and it will be better explained in the next section

3.1.1 The ACM Model

In this work we use the model developed by Galup-Montoro et al. [3]. This model meets several requirements from the designer point of view and is referred as the ACM model from herein.
This model is useful for our thesis work because of:

- The model is single piece; it has accurate expressions and presents simple equations as function of the inversion level
- The model has a few parameters but just enough and those parameters are linked strongly with the device structure and fabrication process because the model is physically based
- In addition, the model conserves charge and it correctly represents all the regions of operation

Let us now resume the main expressions of the ACM model because they will be used throughout this work.
The MOSFET drain current is expressed as very simple functions of two components of drain current, namely, the forward and reverse saturation currents.

$$I_D = I_s\left(i_f - i_r\right) \tag{3.23}$$

Where $i_f\left(i_r\right)$ is the forward (reverse) normalized current and the normalization current is:

$$I_S = \frac{1}{2}\mu n C'_{ox} U_T^2 \frac{W}{L} \tag{3.24}$$

Where these parameters are:

- n : Is the *slope factor*, which is slightly dependent on the gate voltage, but it can be assumed constant for hand calculations and usually n takes value from 1.2 to 1.6 for bulk technology.
- μ : carriers mobility in the channel
- W, L : are the channel width and length respectively.
- C'_{ox} : oxide capacitance per unit area

- U_T: Thermal voltage

The forward normalized current i_f is also referred as the inversion factor since it indicates the inversion level of the MOSFET. As a rule of thumb, values greater than 100 characterize strong inversion and values below 1 characterize weak inversion. Values between 1 and 100 indicate moderate inversion.
The pinch-off voltage is defined as:

$$V_P = \frac{V_G - V_{TO}}{n} \tag{3.25}$$

Where every voltage is referred to the bulk voltage, and:

- V_G: is the gate voltage
- V_{TO}: is the threshold voltage when source voltage V_S, is zero.

The relationship between current and voltage is given by:

$$V_P - V_{S(D)} = U_T\left(\sqrt{1+i_{f(r)}} - 2 + Ln\left(\sqrt{1+i_{f(r)}} - 1\right)\right) \tag{3.26}$$

$V_{S(D)}$ is the source (drain) voltage.

Used with equation (3.25), we can estimate from this expression, the gate voltage in a forward saturated transistor as a function of the inversion level and the source voltage.

$$V_G = V_{TO} + nV_S + U_T\left(\sqrt{1+i_f} - 2 + Ln\left(\sqrt{1+i_f} - 1\right)\right) \tag{3.27}$$

Finally, as we have seen, six capacitances and three transcapacitances characterize the MOS transistor. The complete expressions for these capacitances can be found in reference [3]. Here we will only give an expression for the gate capacitance in the case of a forward saturated transistor with source voltage zero:

$$C_{gs(d)} = C_{ox}\frac{2}{3}\left(1 - \frac{1}{\sqrt{1+i_{f(r)}}}\right)\left(1 - \frac{1+i_{r(f)}}{\left(\sqrt{1+i_f} + \sqrt{1+i_r}\right)^2}\right) \tag{3.28}$$

$$C_{gb} = C_{bd} = \frac{n-1}{n}\left(C_{ox} - C_{gs} - C_{gd}\right) \tag{3.29}$$

3.1.2 The g_m/I_D ratio

The (g_m/I_D) ratio is a key parameter in the design methodologies presented in this work. The ACM model provides a simple expression for the (g_m/I_D) ratio in a forward saturated MOS transistor as a function of the inversion level:

$$\frac{g_m}{I_D} = \frac{1}{nU_T}\frac{2}{\sqrt{1+i_f}+1} \tag{3.30}$$

The methodology based on g_m/I_D ratio considers the relationships between the transconductance over drain current ratio and the normalized drain current, this relationship can be seen in Figure 3.4 where the three regions, strong, moderate and weak inversion, are shown.
This methodology is very useful because it gives us an accurate indication of the device operation region as well as provides the expression to calculate the transistor dimension.

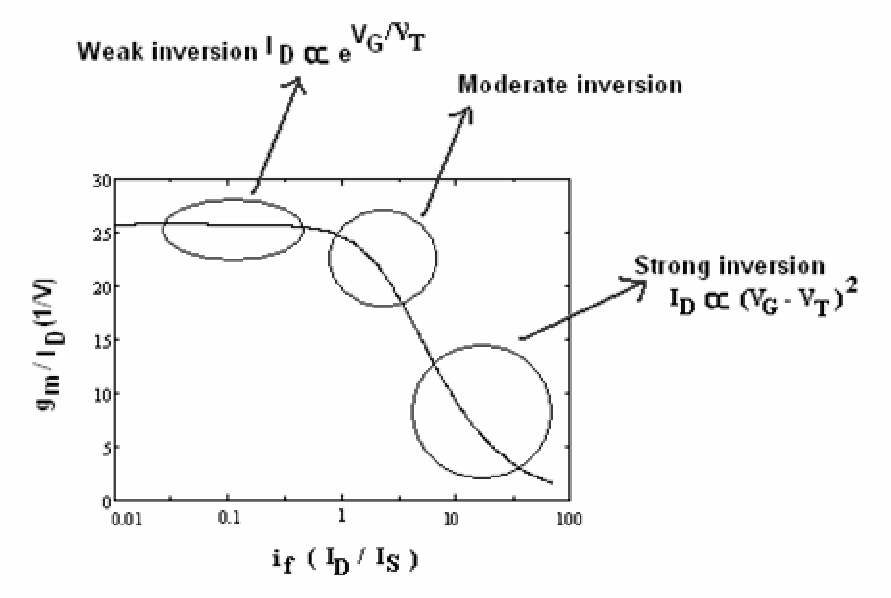

Figure 3.4 Relationship between the inversion factor i_f and the (g_m/I_D) ratio.

3.1.3 Non Quasi-Static Boundary

At this point, one may reasonable think how can highly simplified models be of any use at RF. There are several factors to take into account:

The model presented will become inaccurate at higher frequency when:

1) Extrinsic parasites such as overlap capacitances and gate resistance will appear in the device behaviour because these parasites create poles.
2) If all voltage terminals are varying very slowly, the inversion layer charge has time to follow the input with practically no delay. However, if the variation of voltage is fast, the "inertia" of the inversion layer becomes non negligible. The inversion layer charge does not have enough time to respond fully. These effects are broadly categorized as non-quasi static (NQS) behaviour[1][5]

The most notable difference between the QS and NQS models appears to be the specific dependence of g_m with the frequency. The frequency limits of validity is provided in the literature as only rough indications of the regions within which a given model will perform satisfactorily in most cases. There is not a unique limit and general agreement for the boundary frequency does not exist.

To summarize, the frequency limits in strong inversion, provided in [1] are the follows:

- Quasi static model without transcapacitances: frequencies below $\frac{\omega_o}{10}$
- Quasi static model with transcapacitances: frequencies below $\frac{\omega_o}{3}$

- First order non quasi static model: frequencies below ω_o

Where:
$$\omega_0 = \frac{\mu(V_{GS} - V_T)}{\alpha L^2} = \frac{4}{3\tau} \tag{3.31}$$

- α : coefficient of first –order term in expansion for $-Q_B^{'}/C_{ox}^{'}$
- L : are the channel length.
- τ : transit time defined as the average time that a carrier takes for travel the length of the channel.

On the other hand, many NQS models have been proposed in the literature, taking into account different effects and with different degrees of approximation. These models need replacing the intrinsic capacitances and transconductances with higher order admittances and transadmittances [2]. As an example we show the analytical expression of some of them in order to get a feeling.
Some of the equations (3.11) to (3.15) become frequency dependents as follow[1]:

$$y_m = \frac{g_m}{1 + j\omega\tau_1 + ...} \tag{3.32}$$

$$-y_{gs} = j\omega C_{gs} \frac{1 + j\omega\tau_2 + ...}{1 + j\omega\tau_1 + ...} \tag{3.33}$$

$$-y_{sd} = \frac{g_{sd}}{1 + j\omega\tau_1 + ...} \tag{3.34}$$

$$-y_{bs} = j\omega C_{bs} \frac{1 + j\omega\tau_2 + ...}{1 + j\omega\tau_1 + ...} \tag{3.35}$$

Where, the first order time constant is [3]:

$$\tau_1 = \frac{L^2}{\mu U_T} \frac{1}{5} \frac{1}{\sqrt{1 + i_f}} \tag{3.36}$$

Assuming $\omega\tau_1 << 1 \Rightarrow \frac{1}{1 + j\omega\tau_1} \approx 1 - j\omega\tau_1$

Thus, we can write:

$$y_m \approx g_m - j\omega\tau_1 g_m \tag{3.37}$$

A comparison with y_m obtained for the complete quasi static model (3.17) shows that the form is the same. An examination of the expressions reveals that: $\tau_1 g_m = C_m$ .Thus, this NQS model could be reduced to the complete quasi static model. The expression is in fact identical, only the form, because the coefficients are different. That is a big problem due to in both models, the value of g_m is dependent of the frequency. Thus, where is the non quasi static limit exactly, called f_{NQS} from herein? It is possible to determine the non quasi static limit when the value g_m stars to drop, due to in both models, g_m is gone down at higher frequency?

In the literature [1][5], the quasi static assumption used for deriving the small signal circuit does not hold anymore when the frequency gets close to the intrinsic cut-off frequency of the device defined as the frequency at which the short circuit current gain of the transistor becomes unit.

Let us considerer a transistor where the bias is assumed such that operation is in saturation region, the cut- off frequency is defined as the transition frequency at which the common-source small signal current gain becomes unity at short- circuit load, thus we have:

$$f_T = \frac{g_m}{C_{gs} + C_{gd} + C_{par}} \tag{3.38}$$

Capacitance *Cpar* includes *overlap* capacitance and interconnect capacitance to the substrate.
In practice, the current gain of a complete transistor becomes unity at some frequency less than the cut-off frequency due to the presence of extrinsic parasitic elements and velocity saturation.
In general is accepted that the onset frequency of NQS effect is found to be comparable to f_T and the QS model can do a good job when the operation frequency is sufficiently below f_T. In this work we use this criterion.

In addition, [3], a typical value f_T can be roughly approximated to:

$$f_T = \frac{\mu U_T}{2\pi L^2} 2\left(\sqrt{1+i_f} - 1\right) \tag{3.39}$$

According with [3], the no quasi static correction is significant only for moderate and strong inversion. In weak inversion the quasi static model presented predicts dynamic operation with satisfactory precision at frequencies up to intrinsic cut-off frequency. In moderate and strong inversion the applicability of the quasi-static model should be restricted to frequency values up to one-third of the intrinsic cut-off frequency.

To summarize, the onset frequency of NQS effect is found to be comparable to f_T and the QS model can do a good job when the operation frequency is sufficiently below f_T. In this work we use equation (3.52) (see next section).

In addition with this, the modelling of extrinsic effects (source, drain, gate, and substrate resistance, overlap and junction capacitances) must be done with accuracy and taken into account
The performance of the device is largely determined by the geometry of the device, resulting from its layout. Let us considerer a device of length L and width W and we can see in principle there are three possible layout structures.
The first option is a single structure, which means that the device is drawn or laid out as rectangle with width W and length L. It is shown in the figure 3.5. This structure is usually used in digital circuit but, in contrast in RF applications, this is the worst geometry due to gate resistance. The gate resistance can be approximated by:

$$R_g = \frac{1}{3}\frac{W}{L} R_{sq,poly} \tag{3.40}$$

Where $R_{sq,poly}$ is the sheet resistance of polysilicon.

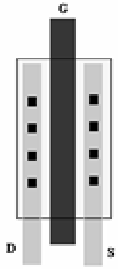

Figure 3.5 Single structure for a MOS transistor

The second option is a parallel structure, where the device is laid out as n devices in parallel structures with each device with a width W/n. If the gate has contacts at both sides, this device has lower gate resistance than the single device because of the reduced width. This structure will reduce the gate resistance but must be used carefully because the drain junction capacitance is increased and it is not optimal due to the parasitic capacitance reduces the cut-off frequency.

The last option can be seen in figure 3.6 and it is a finger structure where the gate is connected from two sides using metal interconnects where a very low total gate resistance could be achieved. To reduce the contribution of the poly resistance to the gate resistance to less than a few ohms, the device must have as many finger as possible. Nevertheless, this layout will increase gate capacitances causing the degradation of f_T .

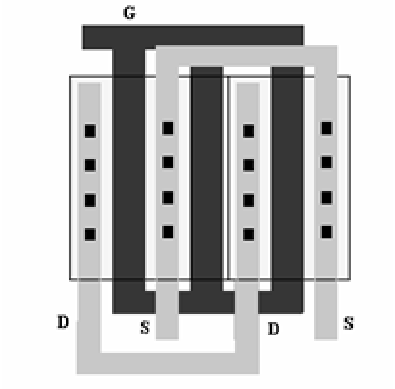

Figure 3.6 Finger structure for a MOS transistor

3.2 TOOL MODELLING APPROACH

The basic amplifier structures considered in figure 2.6 (preamplifiers stages $M_{1,2,3}$ and output power amplifier stage M_p) could be modeled by quadripoles as it is shown in Figure 3.7.

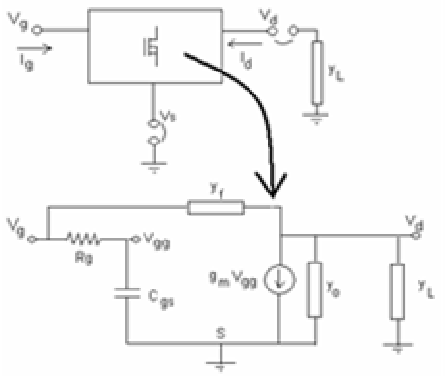

Figure 3.7: MOS Transistor and basic block model

Assuming source voltage as voltage reference and bulk voltage zero, the two port relations of the quadripole in Fig. 3.7 can be written using equation 3.1 and 3.4 as:

$$\begin{aligned} i_d &= y_{dd} v_{ds} + y_{dg} v_{gs} \\ i_g &= y_{gd} v_{ds} + y_{gg} v_{gs} \end{aligned} \tag{3.41}$$

Assuming that MOS transistor operates in saturation and in the quasi-static regimen as it has been discussed, the y- parameters are:

$$y_{dd} = y_O + y_f \tag{3.42}$$

$$y_{dg} = \frac{g_m}{1 + j.2\pi.f.R_g C_{gs}} - y_f \tag{3.43}$$

$$y_{gd} = -y_f \tag{3.44}$$

$$y_{gg} = \frac{j.2\pi.f.C_{gs}}{1 + j.2\pi.f.R_g C_{gs}} + y_f \tag{3.45}$$

Where:

- y_f , y_o :are respectively the feedback and the output admittances, which include parasites capacitances of the MOS transistor and external components, such as a drain - gate feedback resistor when it is added (it is better explained in the next chapter)
- C_{gs} : is the total gate-source capacitance equal to the sum of the gate-source and the gate-substrate capacitances (intrinsic and extrinsic).
- R_g :is the gate resistance and f is the frequency.

The admittances shown in equation (3.42) to (3.45) include five intrinsic capacitances and extrinsic capacitances (gate - source and gate - drain overlap capacitances and drain - substrate and source - substrate junction capacitances). For the intrinsic capacitances, the medium frequency, five capacitor model is deemed enough as it has been discussed. Thus, we can write:

$$y_f = \frac{1}{R_F} + j.2.\pi.f.C_{ov}.W \tag{3.46}$$

Where:

- W : is the transistor width
- C_{ov} : is the gate-drain overlap capacitance by channel width
- R_F : is the drain - gate feedback resistor (some architectures have this in order to get better matching impedance and flatter frequency response at high frequency and must be included in our model.(see figure 3.8 as an example)

The intrinsic load is:

$$y_O = g_d + j.2.\pi.f.C_{db} \tag{3.47}$$

Where:

- g_d is the small signal output conductance of the MOS transistor.
- C_{db} is the extrinsic drain substrate parasitic capacitance given by:

$$C_{db} = X.W\,C_j + (W + 2X).C_{jsw} + W.C_{jswg} \tag{3.48}$$

Where:

- X is the length of the source and drain regions

- C_j is the drain-substrate capacitance per area,
- C_{jsw} is the sidewall parasitic capacitance per unit width
- C_{jswg} is the sidewall parasitic capacitance per unit width in the channel side of the drain area.

The capacitances, C_j , C_{jsw} and C_{jswg} must be corrected in function of the parameters M_{JSW} (sidewall junction grading coefficient) and P_B (junction potential) and the voltage applied to the junction in the following form:

$$C_j(V) = \frac{C_j}{\left(1 + \frac{V}{P_B}\right)^{M_{JSW}}} \tag{3.49}$$

The extrinsic load is:

$$y_L = \frac{1}{Z_{load}} + \left(gd + j.2.\pi.f.C_{db}\right)\Big|_{current\ \ source} \tag{3.50}$$

This expression is composed by the real external load $\frac{1}{Z_{load}}$ and the term $\left(gd + j.2.\pi.f.C_{db}\right)\Big|_{current\_source}$ models the impedance of the bias circuit (which is not shown in Fig.3.7) but we can see an example in the following figure.

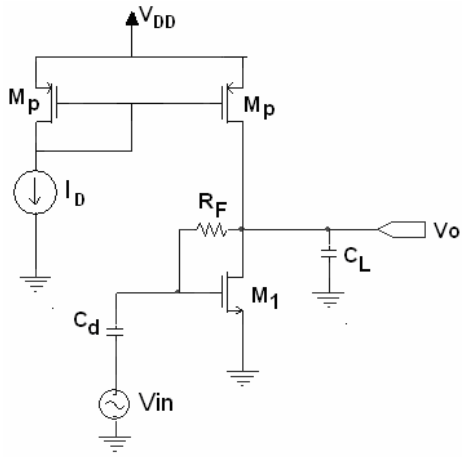

Figure 3.8: Circuit for example

With these expressions, the four admittances can be written as a set of equations suitable to work in MATLAB. Finally, the voltage gain G of the stage is given by:

$$G = \frac{v_{ds}}{v_{gs}} = \frac{-y_{dg}}{y_{dd} + y_L} \tag{3.51-a}$$

And then:

$$A\left(I_D, \frac{g_m}{I_D}\right) = |G| = \frac{|y_{21}|}{|y_{22} + y_L|} \tag{3.51-b}$$

The model that has been presented is a quasi-static model (QS).That is why it is important to have an estimation

of the frequency which limits the zones of QS and NQS operation. This limit has been fixed at $0.1 \cdot f_T$ (where f_T is the unitary gain frequency or also called cut-of frequency) as it is proposed in [1][5] and also we have extensity discussed :

$$f_{QS\max} \approx \frac{f_T}{10} = \frac{0.1\, g_m}{2\pi\left(C_{gs} + C_{gb} + C_{gd}\right)} \tag{3.52}$$

Working below this limit assures also that is not necessary to use the complete model of the six intrinsic capacitances and three transcapacitances of the device.
Another effect that can limit the performance of the transistor MOS at high frequency is the carrier velocity saturation; an effect that is noticeable in very strong inversion. But, as in this work is shown that it is possible and convenient to work in moderate inversion, in the following this effect is not considered. In case of working in very strong inversion (g_m/I_D less than 3…4 1/V) it has to be taken into account that this can modify the showed results.

3.3 TWO PORT NETWORK MODELS

The Z, Y and S parameter are used to characterize a two-port network, but in our circuits we will have a cascade connection of two or more two-port network. Then, we will see that the K matrix (in the literature it is well known as transmission matrix) provide an easily way to study cascade connection due to the transmission matrix of the cascade connection can be easily found multiplying the transmission matrices.
In spite of the fact that we have developed models based on y- parameters, some time we will have to change to K parameter so that study the behaviour of the cascade connection.

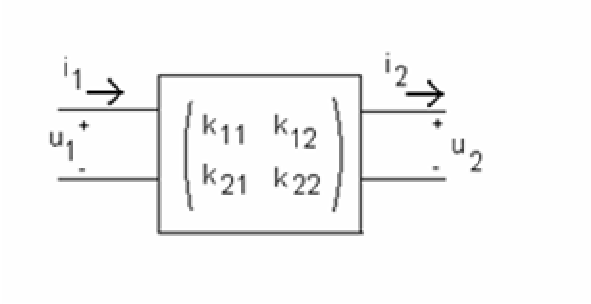

Figure 3.9: Two ports K matrix representation

$$\begin{pmatrix} u_1 \\ i_1 \end{pmatrix} = \begin{pmatrix} k_{11} & k_{12} \\ k_{21} & k_{22} \end{pmatrix} \begin{pmatrix} u_2 \\ i_2 \end{pmatrix} \tag{3.53}$$

The cut-off frequency can be obtained from the K matrix for $u_2 = 0$ as follow:

$$\frac{1}{k_{22}\left(f_T\right)} = 1 \tag{3.54}$$

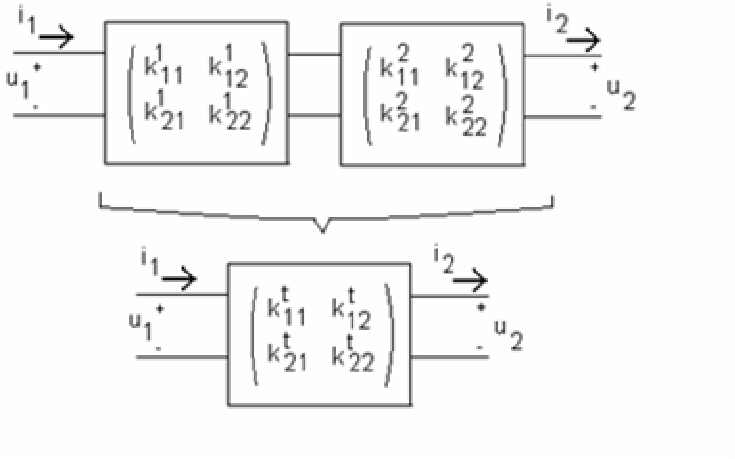

Figure 3.10: Two ports K matrix cascade connection equivalence

Thus, the equations set for transformation is the following:

$$\begin{aligned} k_{11}^{t} &= k_{11}^{1}k_{11}^{2} + k_{12}^{1}k_{21}^{2} \\ k_{12}^{t} &= k_{11}^{1}k_{12}^{2} + k_{12}^{1}k_{22}^{2} \\ k_{21}^{t} &= k_{21}^{1}k_{11}^{2} + k_{22}^{1}k_{21}^{2} \\ k_{22}^{t} &= k_{21}^{1}k_{21}^{2} + k_{22}^{1}k_{22}^{2} \end{aligned} \tag{3.55}$$

If we have a y- parameter representation as:

$$\begin{pmatrix} i_d \\ i_g \end{pmatrix} = \begin{pmatrix} y_{dd} & y_{dg} \\ y_{gd} & y_{gg} \end{pmatrix} \begin{pmatrix} v_{gs} \\ v_{ds} \end{pmatrix} \tag{3.56}$$

The transformation from y-parameters to K- parameters are:

$$k_{11} = -\frac{y_{gg}}{y_{gd}} \tag{3.57}$$

$$k_{12} = -\frac{1}{y_{gd}} \tag{3.58}$$

$$k_{21} = y_{dg} - \frac{y_{dd}\,y_{gg}}{y_{gd}} \tag{3.59}$$

$$k_{22} = -\frac{y_{dd}}{y_{gd}} \tag{3.60}$$

3.3.1- Transformations to study others architectures.

At the moment we have presented a model of MOS transistor for common –source configuration, but it will useful to study others configurations. First we are to going to extend the matrix representation resulting while MOS transistor has source impedance.

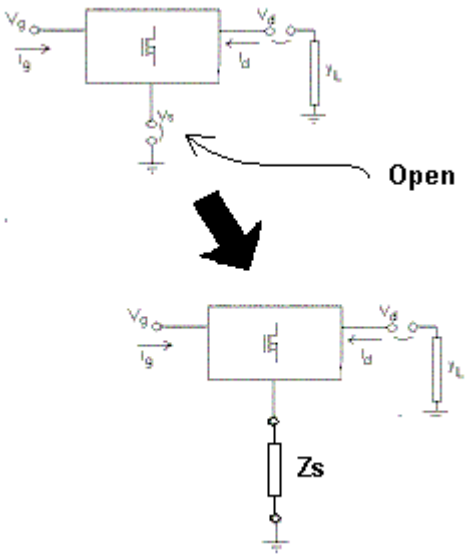

Figure 3.11: MOS transistor and its source impedance

Thus, using y- parameter model, we have:

$$\begin{aligned} v_s &= Z_s\left(i_g + i_d\right) \\ i_g &= y_{dd}\left(v_g - Z_s\left(i_g + i_d\right)\right) + y_{dg}\left(v_d - Z_s\left(i_g + i_d\right)\right) \\ i_d &= y_{gd}\left(v_g - Z_s\left(i_g + i_d\right)\right) + y_{gg}\left(v_d - Z_s\left(i_g + i_d\right)\right) \end{aligned} \tag{3.61}$$

Logically, therefore:

$$\begin{aligned} i_g\left(1 + y_{dd}Z_s + y_{dg}Z_s\right) + i_d\left(y_{dd}Z_s + y_{dg}Z_s\right) &= y_{dd}v_g + y_{dg}v_d \\ i_d\left(1 + y_{gd}Z_s + y_{gg}Z_s\right) + i_g\left(y_{gd}Z_s + y_{gg}Z_s\right) &= y_{gd}v_g + y_{gg}v_d \end{aligned} \tag{3.62}$$

And:

$$\begin{pmatrix} 1 + y_{dd}Z_s + y_{dg}Z_s & y_{dd}Z_s + y_{dg}Z_s \\ y_{gd}Z_s + y_{gg}Z_s & 1 + y_{gd}Z_s + y_{gg}Z_s \end{pmatrix}\begin{pmatrix} i_g \\ i_d \end{pmatrix} = \begin{pmatrix} y_{dd} & y_{dg} \\ y_{gd} & y_{gg} \end{pmatrix}\begin{pmatrix} v_g \\ v_d \end{pmatrix} \tag{3.63}$$

In summary, it is reduced to:

$$\begin{pmatrix} i_g \\ i_d \end{pmatrix} = T^{-1}\begin{pmatrix} y_{dd} & y_{dg} \\ y_{gd} & y_{gg} \end{pmatrix}\begin{pmatrix} v_g \\ v_d \end{pmatrix} \tag{3.64}$$

Where:

$$T = \begin{pmatrix} 1 + y_{dd}Z_s + y_{dg}Z_s & y_{dd}Z_s + y_{dg}Z_s \\ y_{gd}Z_s + y_{gg}Z_s & 1 + y_{gd}Z_s + y_{gg}Z_s \end{pmatrix} \tag{3.65}$$

Of course, if Z_s =0, thus: $T = \begin{pmatrix} 1 & 0 \\ 0 & 1 \end{pmatrix}$ and we have again (3.56) corresponding to common-source configuration.
In conclusion, for software tool we have to calculate the matrix T so that study the effects of source impedance makes on our circuits architecture. Another example shall be useful to study is the common-gate, usually used as cascode configuration. Accordingly with our model, this realization is shown schematically in the following equations:

$$\begin{aligned} i_g &= y_{dd}(v_g - v_s) + y_{dg}(v_d - v_s) \\ i_d &= y_{gd}(v_g - v_s) + y_{gg}(v_d - v_s) \end{aligned} \tag{3.66}$$

In addition, it is sufficiently clear that in common gate configuration:

$$\begin{aligned} v_g &= 0 \\ i_g + i_d &= i_s \end{aligned} \tag{3.67}$$

Thus:

$$\begin{aligned} i_s - i_d &= -(y_{dd} + y_{dg})v_s + y_{dg}v_d \\ i_d &= -(y_{gd} + y_{gg})v_s + y_{gg}v_d \end{aligned} \tag{3.68}$$

$$\begin{aligned} i_s &= -(y_{dd} + y_{dg} + y_{gg} + y_{dg})v_s + (y_{dg} + y_{gg})v_d \\ i_d &= -(y_{gd} + y_{gg})v_s + y_{gg}v_d \end{aligned} \tag{3.69}$$

$$\begin{pmatrix} i_s \\ i_d \end{pmatrix} = \begin{pmatrix} -(y_{dd} + y_{gd} + y_{gg} + y_{dg}) & (y_{dg} + y_{gg}) \\ -(y_{gd} + y_{gg}) & y_{gg} \end{pmatrix} \begin{pmatrix} v_s \\ v_d \end{pmatrix} \tag{3.70}$$

Finally, the y-matrix cascode can be expressed as follow:

$$Y\,cascode = \begin{pmatrix} -(y_{dd} + y_{gd} + y_{gg} + y_{dg}) & (y_{dg} + y_{gg}) \\ -(y_{gd} + y_{gg}) & y_{gg} \end{pmatrix} \tag{3.71}$$

Using y-parameters from (3.42) to (3.45), we have calculated y-matrices for modelling different architectures.

The y-matrix representation as well as K-matrix representation are suitable for making a exploration tool which can be used to study trade-offs and performances of several circuits configurations while a designer explore different circuits behaviour while designing. This issue is the main topic of the next chapter.

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Chapter 4

Tool for CMOS RF Design

Chapter Overview – *This chapter begins with an overview of the tool developed as main goal of this work, which can be used to design amplifiers obtaining an optimum from current consumption point of view and showing the trade off between amplifier's gain and power consumption as well as to evaluate the performance of a particular technology at a desired frequency.*
At the end, two different circuits are presented as design examples implemented in order to validate the results of against simulations and measurements.

4.1- DESIGN EXPLORATION PROCESS

One application example considered in this work is the process of designing a power amplifiers which can be capable to boost up power from VCO (voltage controlled oscillator), as part of a circuit used to implement a wireless sensor network node.

In this way, as designers, we have asked ourselves a variety of "What if…" type questions. For instance, "What if my PA is used instead of ……?", "What happens if I change my level of inversion without touching the size of the transistor ?, "What can I do if multipath fading is considerably more severe than anticipated and for this reason the power amplifier must deliver more power, according with that, what size of the MOS should I draw ?"…….

At the first stage, we have not tried to answer questions definitively and more often we have tried to determine what questions are worth asking. For example, reducing power consumption is one clear objective, but less obvious are the methods and tradeoffs that enable it.
We understood that a good tool for design of analog CMOS RF circuits must involve the study of trade-offs of several performance parameters such as linearity, power gain, voltage gain and power consumption.
In this way, the most important issue in the context of this thesis is the importance of incorporating an easy view of the trade off and constraints into the design process, particularly related to current consumption.

On the other hand, from our point of view, accuracy is not the most important consideration; "first-order" results are sufficient for us. More important, is the ability to modify the system description quickly and easily in order to investigate a wide range of system configurations.
Consequently, we remark the most important features in "exploration stage tools" are simplicity and flexibility.

Without these kinds of tools, we might have been forced to use heuristics, past experience and intuition to guide the design process, and the design "targeted" may have achieved after excessive time and effort.

In principle, this tool seems difficult to create because of circuits descriptions are rarely amenable to be written under closed-form analytic equations, particularly when operation in all regions of inversion of the MOS transistor is considered.

For this reason, we use a y- matrix representation of the MOS transistor because as we have discussed previously in the chapter 3, we mention again that this model has enormous flexibility to explore different architectures and it is relatively easy to implement in MATLAB, which was the tool selected for algorithm implementation.

We choose MATLAB because it is a very powerful environment that allows us a good understanding of the exploration process.

4.2- MATLAB EXPLORATION TOOL

4.2.1- Formalism

The proposed algorithm for designing RF amplifier blocks considers the design space defined by the DC bias current I_D and the g_m/I_D ratio of the transistor, parameters that define the transistor size assuming L_{min} in order to have the best possible frequency response. The use of g_m/I_D ratio as key variable for analog design has been applied for several years for low frequency [1].

The algorithm is summarized as follows: the design space is covered by a grid of couples (I_D, g_m/I_D), for each of these couples the gain A =A(I_D, g_m/I_D), width W =W (I_D, g_m/I_D) and quasi-static boundary B = B(I_D, g_m/I_D) are obtained. As we remember of the chapter 3, we have:

$$A\left(I_D, \frac{g_m}{I_D}\right) = \frac{\left|y_{dg}\right|}{\left|y_{dd} + y_L\right|} \tag{4.1}$$

The graph of the gain A, is the two dimensional surface which is shown geometrically in the Fig: 4.1

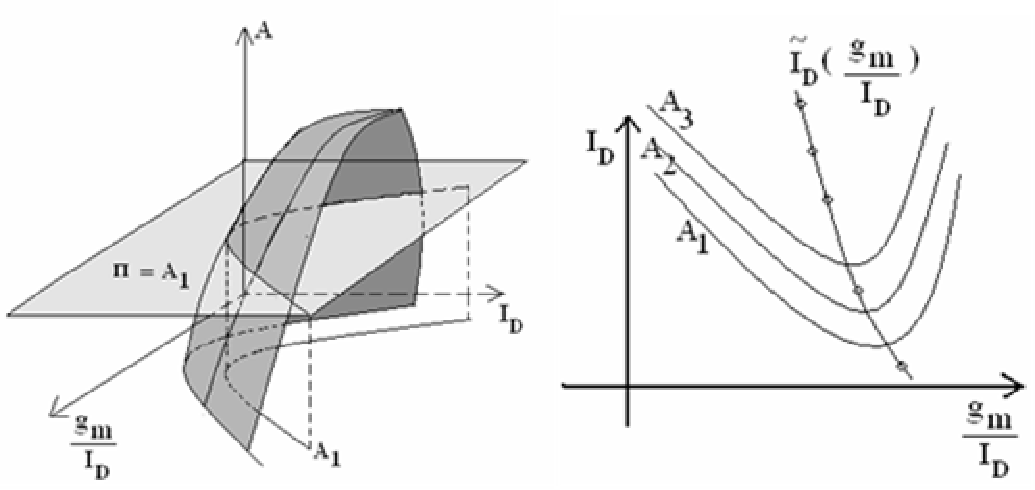

Figure 4.1: The gain A is represented as two dimensional surface and maps of gain are generated as contour maps.

A contour map of the surface $A\left(I_D, \frac{g_m}{I_D}\right)$ is the set of curves obtained by taking horizontal cross-section of the surface. Each of these curves is a family of points $\left(I_D, \frac{g_m}{I_D}\right)$ on the surface at the same height. Thus, the equation of the contour is given by: $I_D = I_D\left(A, \frac{g_m}{I_D}\right)$ in the plane $\left(\frac{g_m}{I_D}, I_D\right)$, also called design space.

For a given gain, there is a g_m/I_D value that results in an optimum of consumption. This optimum lies in moderate inversion for usual gain values at 910MHz in a 0.35µm technology. The locus of the optima represents the set of points where this value is achieved and could be determined analytically in a special case. (See Appendix C)

In the following examples, several circuits are considered and maps of gain generated by the algorithm are shown and explained. We work at 910MHz in a 0.35µm MOS 3.3V technology with the following parameters:

For NMOS transistor:

PARAMETER	VALUE
Gate oxide thickness -tox	7.6 nm
Slope factor – n	1.2
Threshold voltage- VTon	0.5 V
Area junction capacitance- Cjn	0.94e-15 F/µm^2
Sidewall juction capacitance - Cjsn	0.25e-15 F/µm^2
Gate NDIFF/PDIFF overlap - Covn	0.120e-15 F/µm
Effective movility - µn	370 cm^2/Vs
Gain factor - Kn=µnCox	1.68e-4 A/V^2

Table 4.1: NMOS transistor parameters used in the algorithm for the following examples

For PMOS transistor:

PARAMETER	VALUE
Gate oxide thickness -tox	7.6 nm
Slope factor – n	1.4
Threshold voltage- VTop	0.65 V
Area junction capacitance- Cjp	1.36e-15 F/µm^2
Sidewall juction capacitance - Cjsp	0.32e-15 F/µm^2
Gate NDIFF/PDIFF overlap - Covp	0.086e-15 F/µm
Effective movility - µp	126 cm^2/Vs
Gain factor - Kp=µpCox	5.72e-5 A/V^2

Table 4.2: PMOS transistor parameters used in the algorithm for the following examples

4.2.2- Example 1

In the next figure (figure 4.2) a one-stage amplifier with load capacitance C_L and a feedback resistance R_F is presented. The a priori design values are: C_L=0.5pF, R_F =5kΩ, W_{MP} =20µm, f_0 = 910MHz, $L_{MP,M1}$=0.35µm. In the first part of the example the gate resistance R_g is neglected. Later, it is studied the degradation of the previous

results if the R_g corresponding to a non-interdigitized layout is considered.

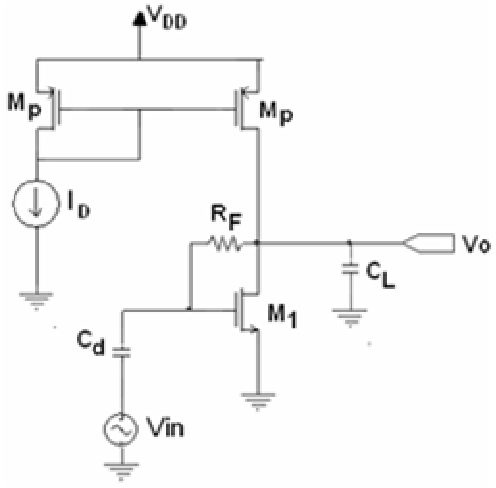

Figure 4.2: Circuit of the example 1

Considering that the desired gain is 2V/V, the algorithm generates the gain curve of Fig.4.3 (circle markers), where we can see that an optimum exists in MI which is marked with an arrow. This optimum has been also shown in analog circuits working at low frequency [3], but as far we know it is the first time that it is shown explicitly for 910MHz and it is a contribution of this work.
It is also shown the curve of optima (points of minimum consumption for a given gain, square markers); thus if it is desired to work optimally for a chosen gain, the current I_D and the g_m/I_D ratio (and therefore the transistor width) are fixed. The last curve of this figure shows the quasi static boundary limit B for this technology (rhomboid markers), where, given a working frequency f_0, the maximum g_m/I_D is fixed independent of I_D. In the optimal point, for this example, the width of M_1 is 223um, I_D is 0.75mA, and g_m/I_D is almost 14. The algorithm results have been contrasted with simulation results using BSIM3v3, and, as it is shown in Fig.4.4, a good correlation has been found.

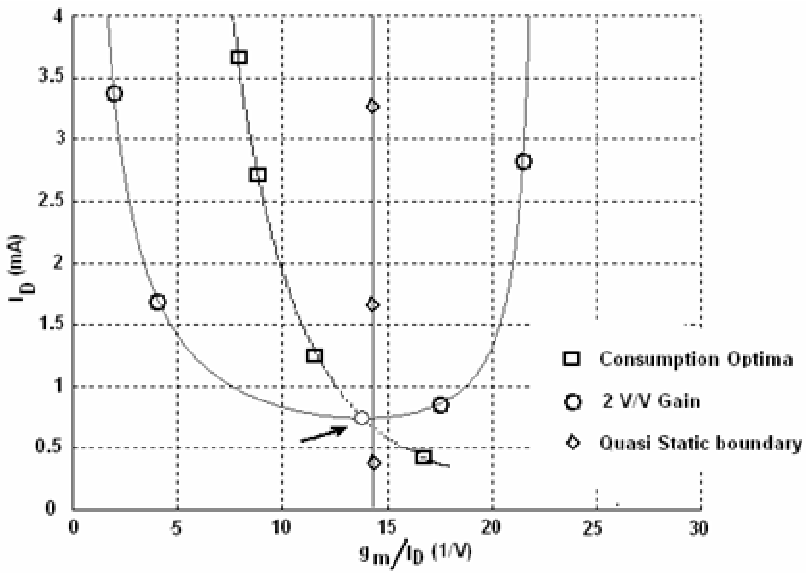

Figure 4.3: Results of example 1. Marked with ○ is the 2V/V gain curve, with □ is the optima of consumption and with ◊ (B curve) is the quasi-static boundary at 910MHz.

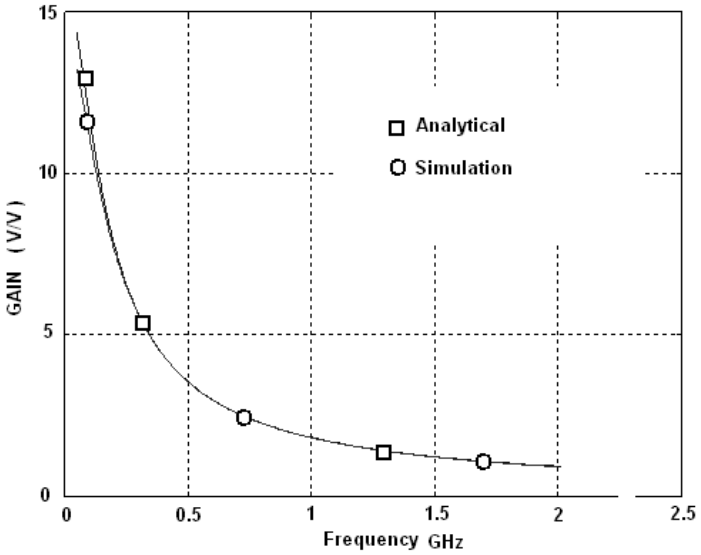

Figure 4.4: Frequency response calculated and simulated, neglecting Rg.

To show the potential of the proposed tool is terms of evaluating design trade-offs, it is studied how the gate resistance degrades the performance of the amplifier designed previously, if proper care is not taken at the layout. The algorithm adds $R_{geff}=R_g/3$, considering a non interdigitized layout for the transistor M_1, with a resistance per square of the gate material of 8.6k Ω/sq. From Fig.4.5 it is clear than the new optimum occurs at a higher current consumption that the previous one (marked by an arrow in the figure). Despite the gate resistance effect is extensively known, it is interesting to see the effect on the consumption at a given gain.

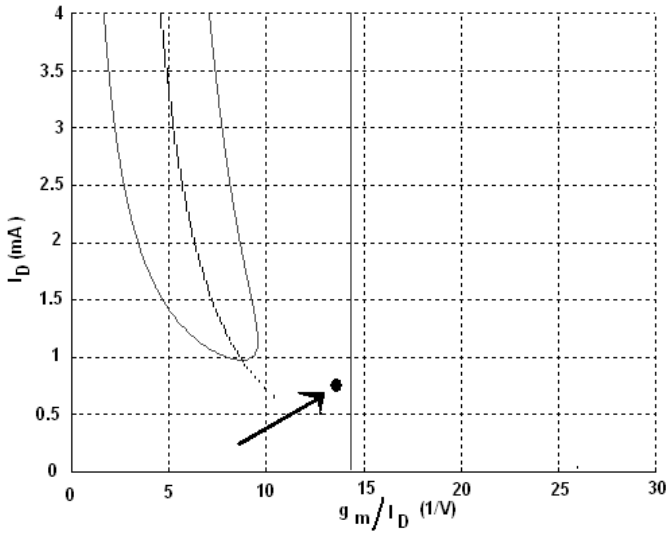

Figure 4.5: Gain curve of 2V/V of example 1 when the effect of R_g of a non interdigitized layout is considered. The point marked by the arrow shows the location of the minimum consumption point determined in Fig. 4.3

4.2.3- Example Nº 2

Using the architecture of Fig.4.2 without R_F and assuming an ideal current source instead of M_1, we have the situation of the figure 4.6. It was used to generate in the figure 4.7, the 2V/V gain curves at 910 MHz for 0.35μm and 0.8μm technologies , with C_L=0.1pF.

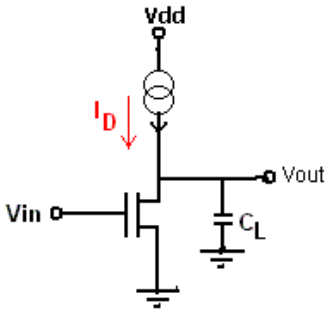

Figure 4.6: Basic amplifier

Introducing the characteristics of each technology into the program, the curves of Fig. 4.7 are obtained. It is clear the possibility of working in moderate inversion with 0.35µm technology, because the optimum is reached in this region, while in 0.8µm it is only possible to work in strong inversion. What is more, the optimum for 0.35µm is reached with a current value 67% smaller than the one for 0.8µm. These advantages for a smaller feature size technology are known but our tool allows to quantify them and determines where the actual limit for a given technology is. The quasi-static boundary limits for both technologies, working at 910MHz, are plotted (curves B_1 for 0.35µm and B_2 for 0.8µm). Also in this case, for the 0.8µm technology, the curve moves to the strong inversion region. Furthermore, it moves beyond the technology optimum, meaning that the minimum required current is probably higher than the one estimated

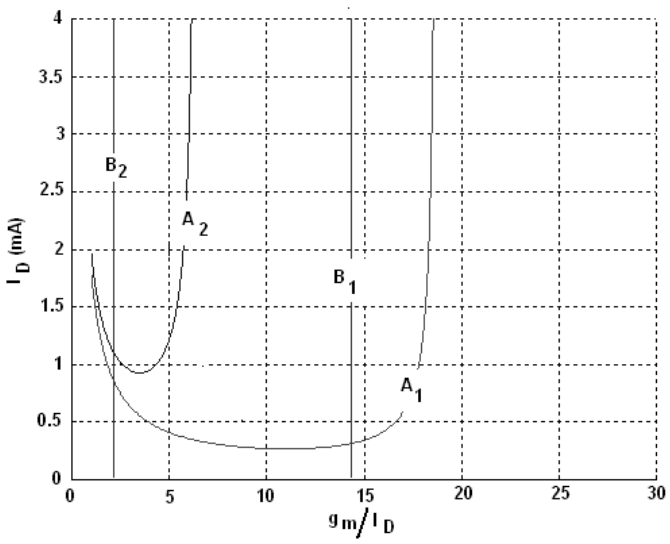

Figure 4.7: Comparison between 0.35µm (A_1) and 0.8µm (A_2) CMOS technologies for a 2V/V gain at 910MHz.

4.2.4- Example Nº 3

More complex architectures could be studied using this tool. For example, in the next figure 4.8 a two-stage amplifier with load capacitance C_L and R_L is presented.. The a priori design values are: C_L=0.1pF, R_L =1kΩ, $W_{MPo,\ MP1}$=20µm, W_{MP2}=60µm, f_0 = 910MHz, $L_{MP,M1,\ M2}$=0.35µm, C_D =1uF and R_1=R_2=50KΩ which provide a DC path that biases the transistors and a capacitance C_2=100pF that opens the feedback in signal.

The size of the transistor M_2 is W_{M2}=200μm and it was designed previously to provide a gain of 4V/V taking into account all possible constraint related to the output power and output voltage swing.
We are looking for an amplifier capable to provide 10 V/V of total amount of voltage gain, thus, considering that the desired gain for the first stage is 2.5V/V, the algorithm generates the gain curve of Fig.4.9, where the optimum is marked with an arrow.

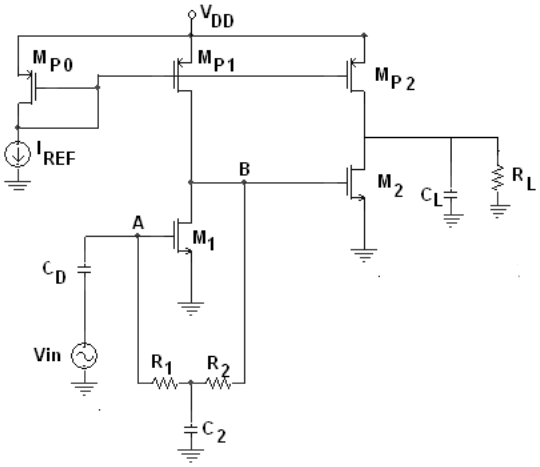

Figure 4.8: Circuit of the example 3

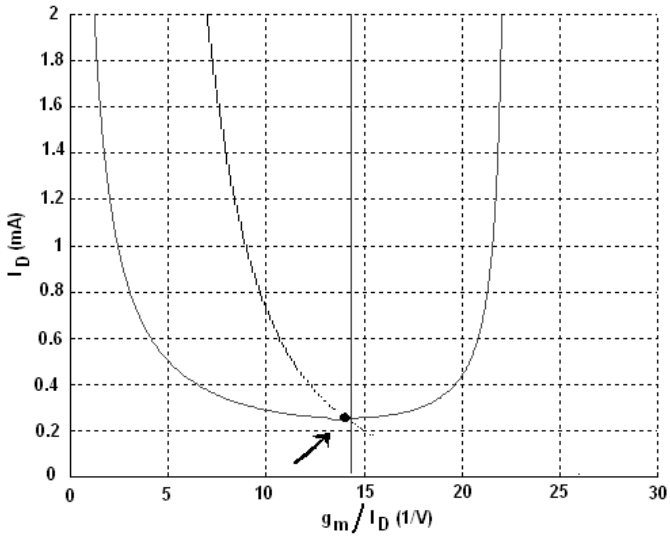

Figure 4.9:Results of the example 3. Marked with arrow we show the 2.5V/V gain desired at minimum current consumption

The algorithm results have been contrasted with simulation results using BSIM3v3, and, as it is shown in Fig.4.10, good correlation has been found.
More specifically we present a comparison of the gain calculated and simulated as well as the gm/Id ratio at 910MHz in the next table 4.3:

Optimum : W=101.41 μm I_D=0. 36mA	Calculated	Simulation
Gain @ 910MHz (V_B/V_A)	2.42 V/V	2.12 V/V
gm/Id (M_1) (1/V)	13.48	13.30

Table 4.3: Gain and g_m/I_D ratio compared between simulation and calculation by the tool at 910MHz

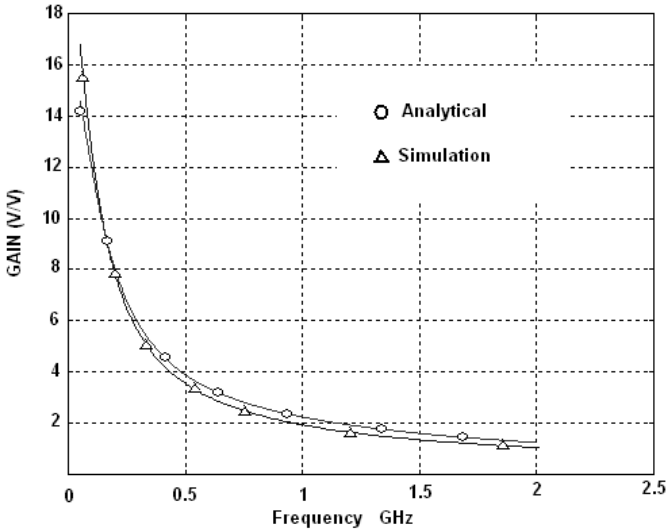

Figure 4.10: V_B / V_A frequency response calculated and simulated in the first stage of the circuit used as example 3

4.3- TOOL USER INTERFACE

Figure 4.12 shows the tool user interface which is a fully interactive plot. The designer can move a cursor on the I_D-g_m/I_D plane and each time the designer selects a point, several characteristics such as bias point, level of inversion, voltage gain, power gain, HD_2, IM_3 and other circuit parameters are automatically computed as a function of the selected I_D-g_m/I_D couple and are shown in the left part of the screen.

The values we see in figure 4.12 will be explained in the tables 4.4, 4.5 and 4.6 and these values are for the point selected by the arrow in the figure 4.13. To generate this result, the tool uses a generic architecture shown in the figure 4.11, where we have:

Zin: input impedance

Po: output power delivered to the load impedance

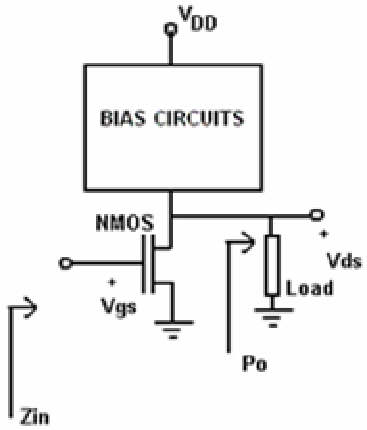

Figure 4.11: Generic architecture to explain the information given by our tool interface

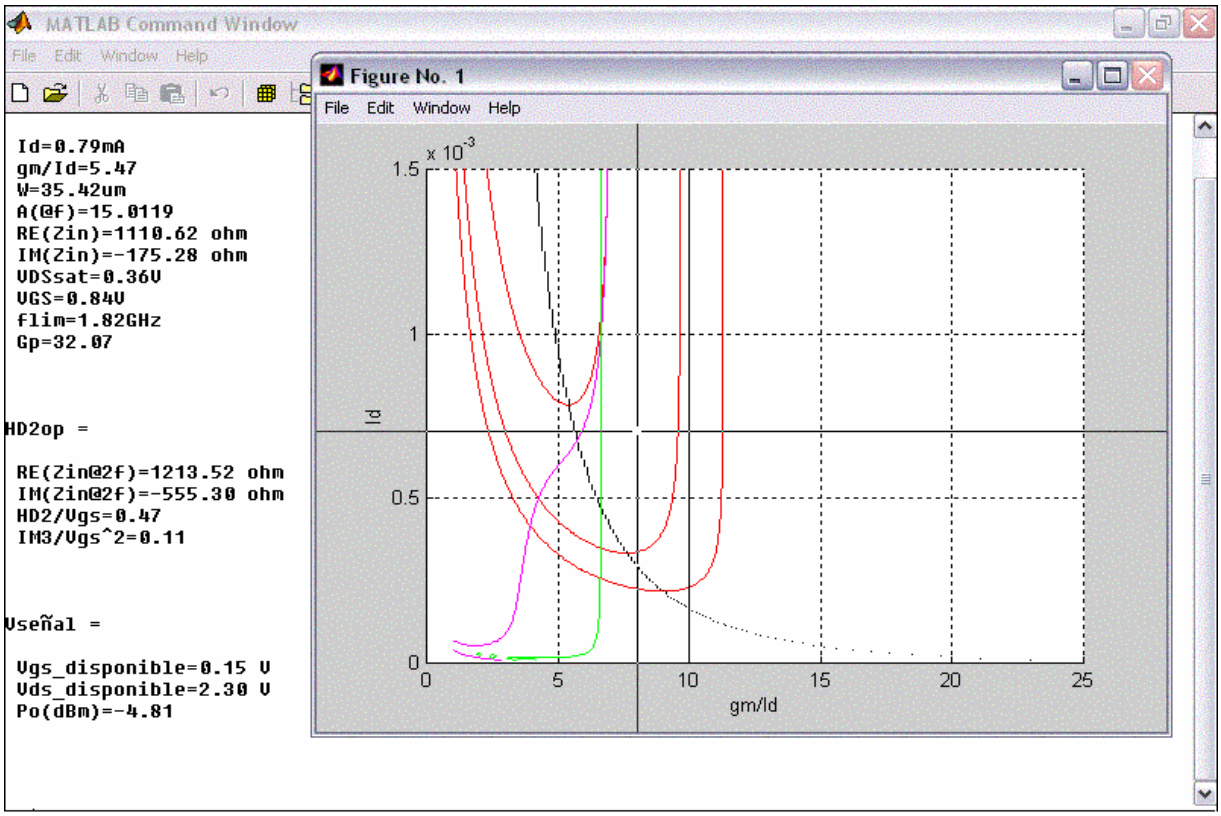

Figure 4.12: Tool user interface

In the next figure 4.13, we present a detailed graph that the tool gives us (the same of figure 4.12)

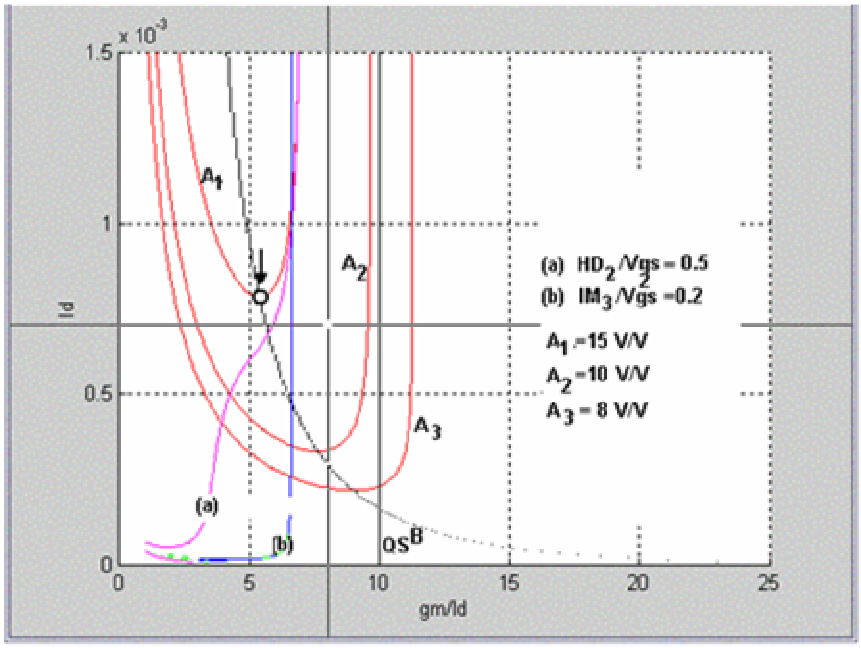

Figure 4.13: Gain map with indications and markers

DCop =	That shows the following information is related to BIAS operation point
Id=0.79mA	Current drain that biases the MOS transistor (the DC current consumption)
gm/Id= 5.47	Transconductance to current ratio (in 1/V) that defines the inversion level
W= 35.42um	Width of the MOS transistor
A(@f)= 15.0119	Voltage Gain at this $\left(I_D, \frac{g_m}{I_D} \right)$ point at a given frequency
RE(Zin)= 1110.62 ohm	Real part of the input impedance Zin at this operation point
IM(Zin)= -175.28 ohm	Imaginary part of the input impedance Zin at this operation point
VDSsat= 0.36V	Saturation Voltage of the MOS transistor
VGS= 0.84V	Gate-source DC voltage at this operation point
flim= 1.82GHz	Non quasi static frequency limit at this operation point
Gp= 32.07	Power gain (mW/mW) at this operation point

Table 4.4: Tool's parameters-Table 1

HD2op =	That shows the following information is related to distortion
RE(Zin@2f)=1213.52 ohm	Real part of the input impedance Zin at this operation point and twice frequency operation
IM(Zin@2f)=-555.30 ohm	Imaginary part of the input impedance Zin at this operation point and twice frequency operation
HD2/Vgs=0.47	Harmonic distortion normalized with Vgs **(1)**
IM3/Vgs^2=0.11	Intermodulation distortion normalized with Vgs^2 **(2)**

Table 4.5: Tool's parameters -Table 2

Vseñal =	That shows the following information is related to input output characteristics
Vgs_disponible=0.15 V	Source gate Voltage amplitude available **(3)**
Vds_disponible=2.30 V	Source drain Voltage (output voltage) amplitude available **(4)**
Po(dBm)=-4.81	Output Power delivered to a given load (in this example it is 8KΩ)

Table 4.6: Tool's parameters -Table 3

(1) (2) The harmonic distortion HD_2 could be written as a function of the operation point and the load impedance, multiplied by the input voltage. In the same way, intermodulation distortion IM_3 could be written as a function of the operation point and the load impedance multiplied by the square of the input voltage (see appendix A, equation A.19, A.21 and A.23, where each Volterra's kernel is a function of the load and the design space)

That is:

$$HD_2 = f_1\left(I_D, \frac{g_m}{I_D}, load \right) V_{gs} \tag{4.2}$$

$$IM_3 = f_2\left(I_D, \frac{g_m}{I_D}, load \right) V_{gs}^2 \tag{4.3}$$

(3)(4) These terms are better explained below:

1) Source gate Voltage available

This is the gate source voltage that make the distortion (harmonic distortion (HD_2) and the intermodulation distortion (IM_3)) keep below a targeted value of distortion. For further information about the harmonic distortion evaluation and the formals method to calculate it, we refer the readers to appendix A.

2) Source drain Voltage available

It is the maximum allowed output swing. It is determined from the most restricting of the two conditions:

a) V_{ds} =A.V_{gs} if V_{gs} is limited by the distortion requirement
b) Otherwise, the output swing limit that was set previously

For instance:
In this example, we have V_{gs}=0.15 V of gate source voltage amplitude, this voltage leads to HD_2 =0.47x 0.15=0.07, less than the maximum value that has been established as maximum in this example, which was 0.5.
In addition with this V_{gs} value, the intermodulation value is IM_3 =0.11x0.15^2 =0.0025, again less than the value 0.2 which has been set in our tool as intermodulation constraint. Thus, the output voltage is given by the second condition and it is V_{ds}=0.15x A =2.3V (the gain is A=15 V/V, see table 4.4)

If V_{gs} may have taken the value 0.3 V, the distortion will be HD_2 =0.47x 0.3=0.141, again less than the value 0.5, but the output voltage will be V_{ds}=0.13xA =4.5V , more than the value 2.3V allowed, thus, the tool must chosen the maximum output swing that was set and shows the value of the maximum drain source voltage available V_{ds} =2.3 V as well as the corresponding gate source voltage available V_{gs} =0.153 V.
For this reason and for the point selected, it is not possible that we use V_{gs}=0.3 V as input voltage due to the constraints that were set in the tool, allowing no more than V_{gs}=0.15V.

When a drain source voltage is found, the tool displays the output power value Po that is delivered to a load whose value was set previously in the kernel of the tool (section of parameter configuration).

The tool incorporates an option to read the input impedance at the frequency we are working and the hypothetical impedance we will see if we changed the work frequency multiplying by a factor of two.
It is necessary because if you connect this block as load of another block, you need to provide this special impedance because of the tool needs it to calculate the amount of harmonic distortion HD_2 and the intermodulation IM_3.

From the figure 4.15, we briefly summarize the procedure that the tool involves to operate correctly:

(1) Information such as frequency, value of load impedance and architecture is written in the tool as lines of code. The constraint related to distortion and maximum output voltage allowed as well as technology parameter could be written as a code form in a special section of the tool.

(2) The tool calculates the parameters, such as intrinsic and extrinsic capacitances that the ACM model needs to calculate the y –parameters for each couple $\left(\frac{g_m}{I_D}, I_D\right)$ in a grid previously generated.

(3) For each of these couples, as soon as the parameter of the ACM model have been estimated , the tool calculates the gain voltage, gain power , distortion and the overall parameters we have explained.
The tool internally works with a matrix representation of each parameter, having the gain voltage matrix, the power gain matrix, the intermodulation matrix, etc.

(4) The procedure of the step (3) takes some minutes; we see a box like this while we are waiting for results.

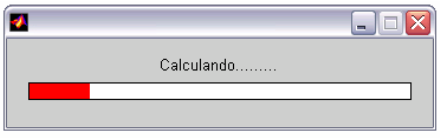

Figure 4.14 Waiting Box

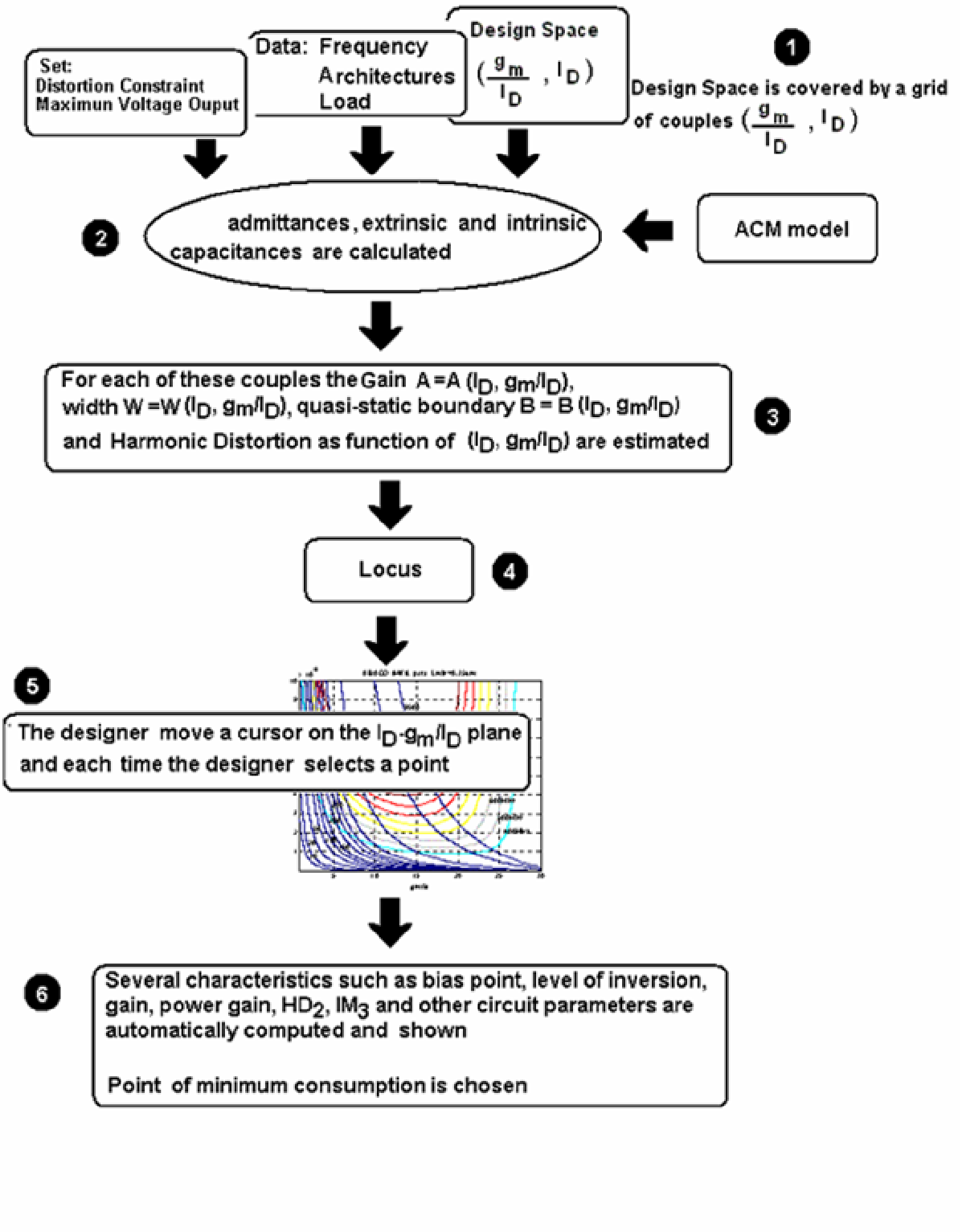

Figure 4.15: Summary of the algorithm implemented.

(5) The contours map appears in the screen , as we showed in figure 4.12

(6) The designer move a cursor on the $\left(\frac{g_m}{I_D}, I_D\right)$ plane and at the same time the selects points are shown. The designer can get information of some interesting point of operation moving the cursor.

4.4- DESIGN EXAMPLES

In this section, we present two circuits implemented.

4.4.1- Optimum Amplifier Stage

In order to achieve high gain levels in an amplifier, gain stages are often cascaded which provides an overall gain of the product of the gain of each of the individual stages. (see figure 2.6**:** a four stage power amplifier). In the next figure (figure 4.16) a one-stage amplifier with resistive load R_L and a feedback resistance R_F is presented.
The a priori design values are: R_L=6847Ω (it is explained below), R_F =20kΩ, f_0 = 910MHz, $L_{MP,M1}$=0.35μm and the PMOS transistor size of the current mirror is W_e =10μm and L_e=0.35μm. This value of W_e was chosen taking into account past designed circuits. From the RF point of view, it should be less than 20 μm in order to neglect the effect of the parasitic capacitances of the PMOS transistor of the current mirror. It has been observed in simulation that higher width of this transistor causes the signal to couple to the transistor gate disturbing the current mirror operation.
For the feedback resistance, the value R_F =20kΩ is used as reasonable value because it make a good compromise between gain and layout area. Usually this resistance is used to have a good matching impedance performance, but in this work we do not study this function. Finally, the load R_L=6847Ω is the result of increasing the 50Ω load resistor to a higher resistance through simple L-C matching network with standard values. It will be better explained in the section *4.4.2*, where the matching process is detailed.

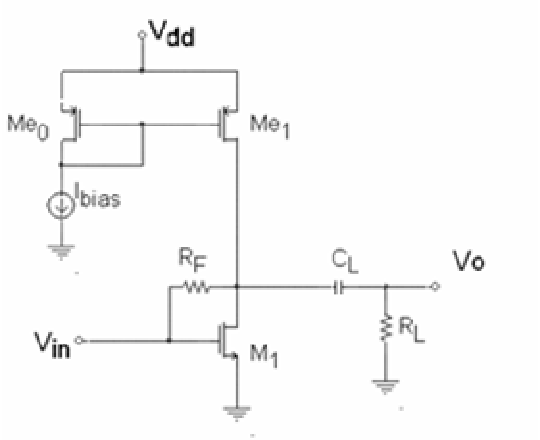

Figure 4.16: Schematic of the Optimum Amplifier Stage

Using the described methodology, the amplifier shown in Fig.4.16 has been designed using the gain map shown in the figure 4.17.The final design parameters are summarized in table 4.7:

	Me_0 (PMOS)	Me_1(PMOS)	M_1
W (um)	10	10	40
I_D (mA)	0.24	0.24	0.24

Table 4.7: Final design parameters

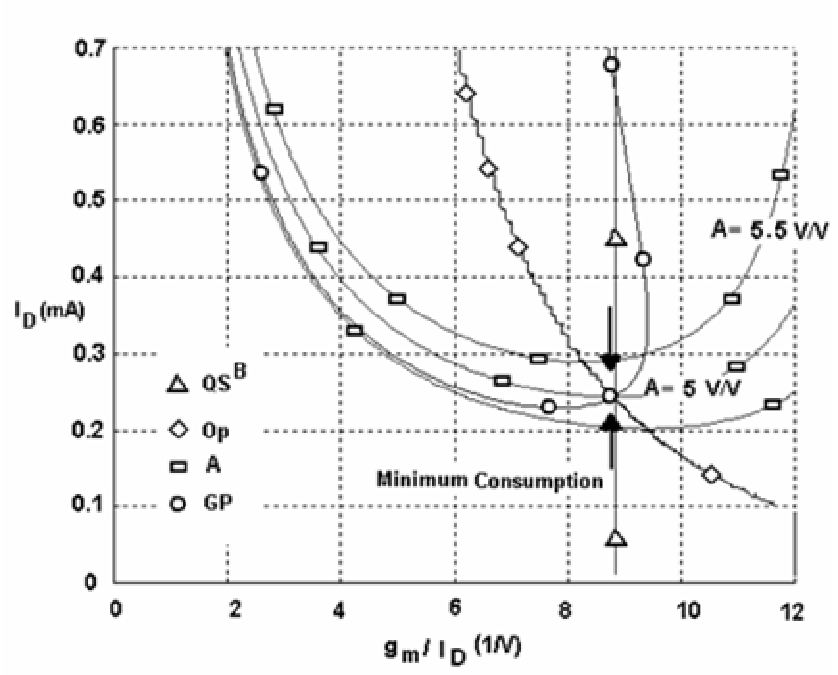

Figure 4.17: Power and Amplitude Gain map for the circuit of the figure 4.16
Where: **Op:** Locus of the optima
QS^B: Quasi static boundary
A: Voltage gain contour map
G_P: Power gain contour map

Numerical results calculated by the tool in the optimum point, which is marked with arrows are presented in the next table:

DCop	HD2op =	Vsenal =
Id=0.24mA gm/Id=8.82 W=36.51um (1) A(@f)=5.0005 RE(Zin)=2976.49 ohm IM(Zin)=-1149.86 ohm VDSsat=0.23V VGS=0.68V flim=0.91GHz Gp=12.49 (4)	RE(Zin@2f)=1127.39 ohm IM(Zin@2f)=-1892.52 ohm HD2/Vgs=0.77 IM3/Vgs^2=0.60 (2)	Vgs_disponible=0.12 V Vds_disponible=0.58 V Po(dBm)=-16.10 (3)

Table 4.8: Numerical results calculated

(1) The MOS transistor laid out has W=40μm
(2) The maximum value for HD_2 was set HD_2 =0.1, (HD_2=0.77. 0.12 =0.092), as well as IM_3=0.1 (IM_3=0.60. 0.12^2 =0.0086)
(3) Over a 50Ω load resistance

(4) Gp: Power gain (mW/mW)

4.4.2- Power Amplifier of a low power short range transmitter

The design of a power amplifier to deliver 0dBm from an integrated VCO to the antenna at 910MHz is presented in the following section. The antenna represents for the power amplifier a load resistance R_L=50 Ω that must be matched as we explain below.
The input voltage provided by the VCO is Vin=0.45V, and the DC voltage V_{DD} =3V.
For this application we use a one stage class B power amplifier with differential output and where an output cascode was added .That configuration is presented in the following figure 4.18 and it is a basic structure discussed in section 2.2.

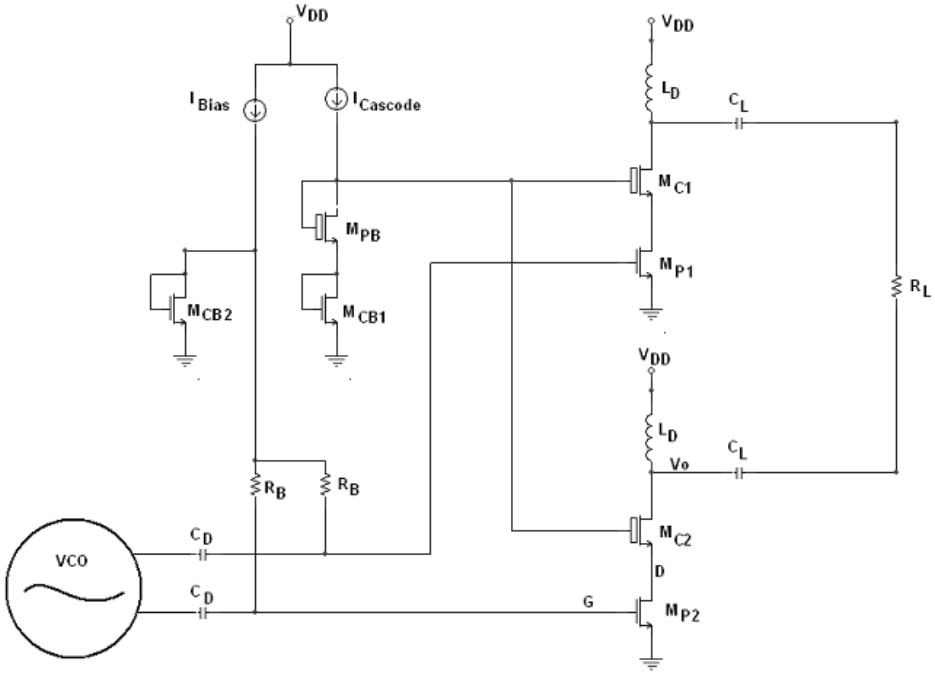

Figure 4.18: Power Amplifier of a low power short range transmitter (see components' value and transistor size in page 62)

The cascode transistor is added for isolation purposes due to the MOS transistor $M_{P1,2}$ are 3.3V transistor and the output swing Vo is higher than 3.3V in order to provide 0dBm output power.
The $M_{C1,2}$ are 0.6μm MOSM 5.5V transistors with the following parameters.

For NMOSM transistor:

PARAMETER	VALUE
Minimum Channel Length (L)	0.6 μm
Gate oxide thickness -tox	15 nm
Slope factor – n	1.3
Threshold voltage- VTon	0.7 V
Area junction capacitance- Cjn	0.94e-15 F/μm^2
Sidewall juction capacitance - Cjsn	0.25e-15 F/μm^2
Gate NDIFF/PDIFF overlap - Covn	0.120e-15 F/μm
Effective movility - μn	435 cm^2/Vs
Gain factor - Kn=μnCox	1e-4 A/V^2

Table 4.9: NMOSM transistor parameters used in the algorithm

The design procedure is the following: the output power over R_L is set Po =0dBm (1mW) , thus , using equation (2.23) $Po = \frac{V_0^2}{2R_{optima}}$ we can calculate R_{optima} , however , we first have to estimate the output voltage swing (Vo) of half amplifier.
This value is determined in the following way: as Vo (DC) =3V and the maximum drain voltage allowed to protect the NMOSM is 5.5V, thus we have 5.5V -3V=2.5 V as possible output voltage swing. For security we take 2.3V as output voltage swing. After that, it is possible to calculate R_{optima} for half amplifier.

Then, for half amplifier: $R_{optima} = \frac{V_0^2}{2(Po/2)} = \frac{(2.3V)^2}{2\,x\,0.5\,mW} = 5290\,\Omega$ (4.4)

We conclude that it is necessary to increase the 50Ω load resistance to a higher resistance through simple L-C matching network with standard values.
Using the software SMITH V1.91 [2] to adapt the load resistance for half amplifier, the matching network L-C is obtained in the next figure:

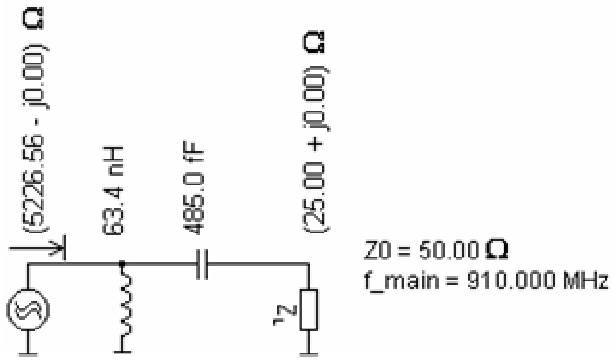

Figure 4.19: Ideal Matching Network

It is important to remark two things:

First: Component's value dispersion:

We have adapted with ideal components and there are not standard components which values are the same we used to create the network. Thus, we need to adapt with standard components that make we have another network, actually very close to our ideal network but it may be capable to generate variations in the output power. An account of having standard components we have to make the following network with the standard values: an inductor of 64.2nH(series of 56nH and 8.2nH) and a capacitance of 0.5pF. Then, we have:

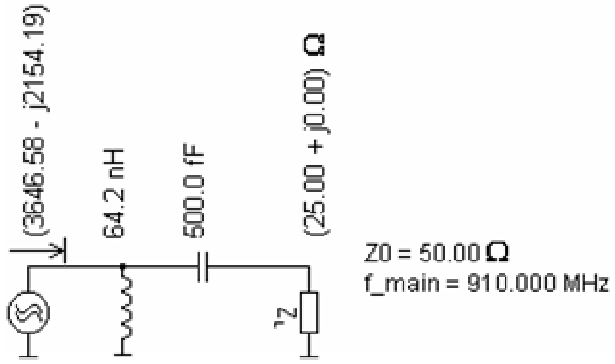

Figure 4.20: Standard matching network

And the new output power for each half amplifier is:

$$P_0 = \frac{1}{2}V_0^2 \,\mathrm{Re}\left(\frac{1}{Zin^*}\right) = \frac{1}{2}(2.3\ V)^2 . \mathrm{Re}\left(\frac{1}{(3646.58 - j2154.19)\Omega}\right) = 0.54mW \qquad (4.5)$$

The first conclusion is the standard network does not represent a problem from the output power point of view. However, the standard components have dispersion. For example, we use two inductors to create the value 64.2nH. These inductances are L_1=56nH and L_2=8.2nH and each inductance has a dispersion of 5 % due to factory process. Consequently, we have to study the dependency with the dispersion:

The generic impedance adaptation using a network L-C is shown in figure 4.21 and produces:

$$y_{in} = \frac{1}{Z_{in}} = \frac{\omega^2 C^2 R_L}{R_L^2\omega^2 C^2 + 1} - j\frac{(\omega^2 LC - 1)}{R_L^2\omega^2 C^2 + 1} \qquad (4.6)$$

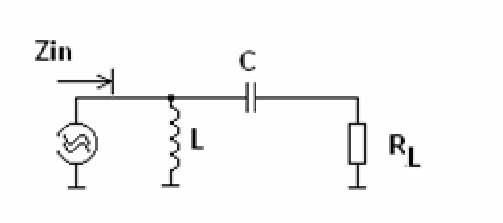

Figure 4.21: Generic L-C impedance transformation network (or matching network)

If we assume that Vo is fixed, the output power is given by:

$$P_o = \frac{1}{2}V_0^2 \,\mathrm{Re}(y_{in}) = \frac{1}{2}V_0^2 \frac{\omega^2 C^2 R_L}{R_L^2\omega^2 C^2 + 1} \qquad (4.7)$$

It is interesting that it only depends on the dispersion of the capacitance C.
If the dispersion for the capacitance C is 50%, (specifically, we use a commercial capacitance whose value is 0.5pF ± 0.25pF) then C=0.5pF varies from 0.25pF to 0.75pF and this make the output power for half amplifier varies from 0.13mW to 1.2mW. Besides this, the total power delivered to the antenna varies from -5.8dBm to 3.8 dBm.

Second: Qualify factor of the standard components.

The standard components have quality factor. In other words, thinking in the case of the inductor, it is not a pure inductor due to it has resistance that produce inductor loss. The inductor loss is then represented by a parallel resistance Rp as is shown in figure 4.22 and it is usually to specify the inductor Q factor at the frequency of interest in order to quantify inductor loss.

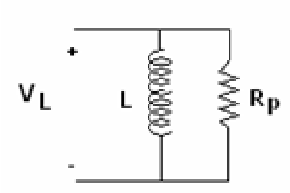

Figure 4.22: Inductor equivalent circuits

The inductor loss is calculated as:

$$P_{loss} = \frac{1}{2}\frac{V_L^2}{R_P} = \frac{1}{2}V_L^2\frac{1}{\omega LQ} = \frac{1}{2}\frac{\omega L I_L^2}{Q} \tag{4.8}$$

(It is assumed that $\omega L << R_p$)

To put things into perspective, we analyze the network showed in figure 4.20. The inductor is formed with the series L_1=56nH and L_2=8.2nH.
If we assume Vo=2.3V as we have done until this moment, is easy to see that the current peak in the inductor is:

$$I_L = \frac{2.3V}{\omega(L_1 + L_2)} = \frac{2.3V}{2\pi\ 910MHz\ 64.2nH} = 6.27mA \tag{4.9}$$

Then, if we use commercial inductor that specify a quality factor of Q=68 for inductor L_1 =56 nH and Q=56 for L_2=8.2nH at 900MHz (it is not exactly 910MHz , but we use this value so that has a estimation)

After that, using equation (4.8) and for L_1, the inductor loss is:

$$P_{loss\ L_1} = \frac{1}{2}\frac{2\pi 910\,MHz.56nH.(6.27mA)^2}{68} = 0.093\,mW \tag{4.10}$$

And for L_2 :

$$P_{loss\ L_2} = \frac{1}{2}\frac{2\pi 910\,MHz.8.2nH.(6.27mA)^2}{56} = 0.017\,mW \tag{4.11}$$

The total amount of inductor loss is 0.11mW, and it represents 22 % of the output power that we intend to deliver to the load resistance. (Remember equation (4.5)). Thus, the real power delivered by half amplifier will be 0.43 mW and the total amount of power delivered will be 0.86mW (-0.66dBm) It is only taken into account the inductor loss.
On the other hand, the value of R_P for a quality factor of Q=68 for the inductor L_1 =56 nH is:

$$R_p = \omega LQ = 2\pi 910MHz.56nH.68 = 21773\Omega \tag{4.12}$$

To sum up, using the equation 4.6, the effect on the impedance transformation network would be written as follow:

$$y_{in} = \frac{1}{Z_{in}} = \frac{1}{R_p} + \frac{\omega^2 C^2 R_L}{R_L^2\omega^2 C^2 + 1} - j\frac{(\omega^2 LC - 1)}{R_L^2\omega^2 C^2 + 1} \tag{4.13}$$

We can see that, in general the value of R_P is not large enough to affect the load impedance but must be considered as inductor loss.

Another problem that we will focus in the appendix D, it related to the bond pads and bonding inductances and capacitances. Due to the presence of these parasites capacitances and inductances, we need to change the matching network in order to find the resonant network at the frequency of interest. For further information about the matching resonance because of bonding and pads, we refer the readers to appendix D

4.4.2.1- Calculus

The gain desired for the amplifier $G_T = V_o/V_{in}$= 2.3V/0.45V =5.1. After this estimation, the power and amplitude gain map are generated and it is shown in the next figure 4.23.

Numerical results calculated by the tool in the optimum point, which is marked with arrows in figure 4.23 are presented in the next table 4.10:

DCop	HD2op =	Vsenal =
Id=1.32mA gm/Id=8.80 W=196.23um (1) A(@f)=5.1153 RE(Zin)=140.29 ohm IM(Zin)=-490.54 ohm VDSsat=0.23V VGS=0.68V flim=0.92GHz GP(dB)=9.86	HD2=0.39 IM3=0.12 (2)	Vgs_disponible=0.45 V (3)

Table 4.10: Numerical results calculated

(1) The MOS transistor has been laid out with W=200µm
(2)The value of HD_2 was not limited in this case due to higher harmonics are filtered in the final output resonant network and for IM_3, it was set IM_3=0.1.For this design the optimum is achieved at the right of the IM_3 (see figure 4.23) and this indicates the value IM_3=0.1 is not possible at the minimum current consumption. Thus we have IM_3=0.12.
(3) This voltage is fixed by the VCO

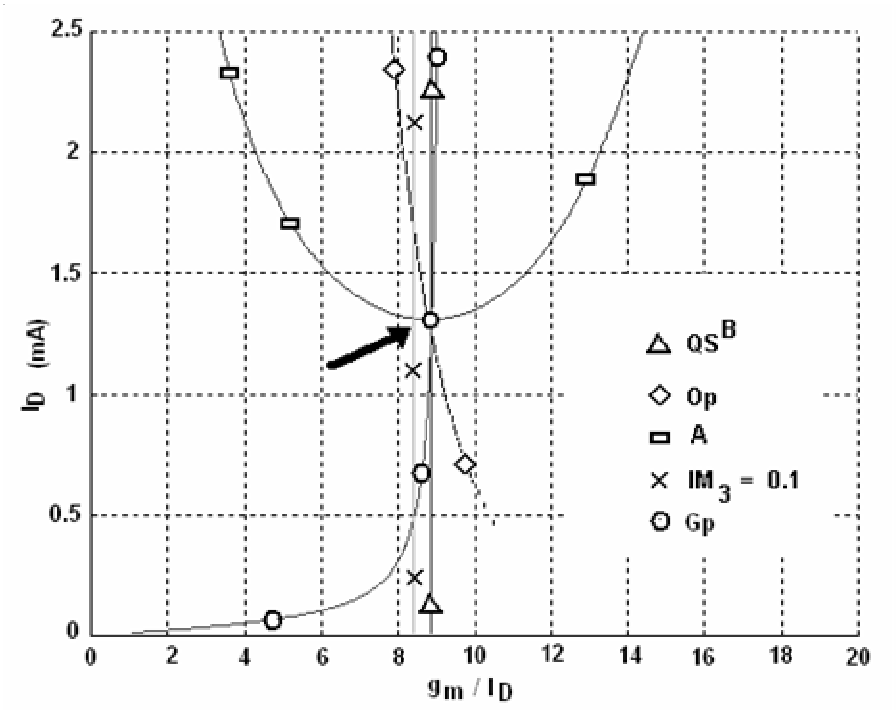

Figure 4.23: Power and Amplitude Gain map of the amplifier detailed in figure 4.18:

Where:
Op: Locus of the optima
QS^B: Quasi static boundary
A: Voltage gain contour map (A=5.11 V/V)
G_P: Power gain contour map (Gp=9.8dB)

Finally, from the figure 4.18, the final design is:

Currents consumption : Ibias = 30μA
Icascode = 200μA

Transistor sizes :

$M_{P1,2}$	L=0.35 μm W=200 μm
M_{CB2}	L=0.35 μm W=5 μm (Ibias / W_{CB2} =I_D/$W_{P1,2}$)
$M_{C1,2}$	MOSM 5.5V technology L=0.6 μm W=10 μm
M_{PB}	MOSM 5.5V technology L=0.6 μm W=5 μm
M_{CB1}	L=0.35 μm W=5 μm

Table 4.11: Final design

Other components values are:
-R_B= 20KΩ
-C_D=10pF

The value of R_B is not critical in this design, the higher value, the better in order to prevent signal coupling at the drain of M_{CB2} .We have selected 20KΩ due to layout area considerations.

It is interesting to note the following problem:
As we are not sure about the exact value of the inductances and capacitances parasites because of the package, we have added in the tool a extra impedance load of Ce=0.23pF to take into account dispersion in the matching network being sure in a worst case the desired output power is delivered to the load independently of some soft dispersion in our matching network.

If the Ce is modified from 0.23pF to 0.3pF, the tool generates another map we show in the next figure 4.24 and the tool predicts that at the same current consumption the voltage gain is 4 V/V , the gain power is dropped from 9.8dB to 8dB and the output power is then 0.33mW for each half amplifier. The total amount of power delivered in this situation is 0.66mW (-1.8dBm). The voltage gain is a function very sensible with variations in the load impedance (see appendix C, equation (C.40))

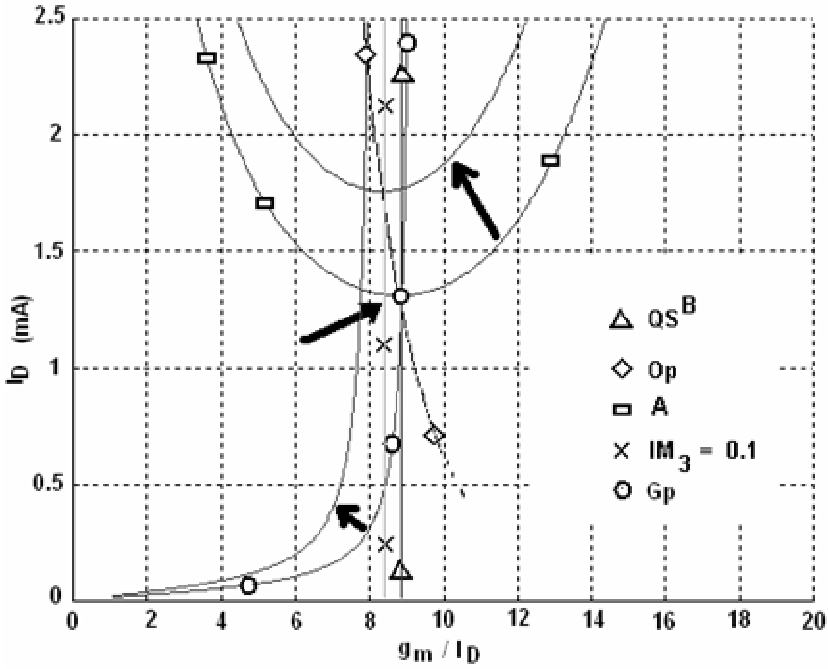

Figure 4.24: Variations in the power and amplitude gain map, contrasted with the previous calculus

4.5- REFERENCES

[1] F.Silveira, D. Flandre, P.G.A. Jespers, "A gm/ID Based Methodology for the Design of CMOS Analog Circuits and its Application to the Synthesis of a Silicon-on-Insulator Micropower OTA", *IEEE Journal of Solid State Circuits*, Vol. 31, No. 9, Sept. 1996, pp. 1314 – 1319

[2] SMITH V1.91 Demo version freely distributed from The University of Applied Sciences Berne -Berne Institute of Engineering and Architecture F. Dellsperger Professor Morgartenstrasse 2c CH-3014 Bern Switzerland Fax. ++41 31 33 30 625 e-mail fritz.dellsperger@hta-be.bfh.ch.

[3] F.Silveira, D. Flandre, P.G.A. Jespers, "A gm/ID Based Methodology for the Design of CMOS Analog Circuits and its Application to the Synthesis of a Silicon-on-Insulator Micropower OTA", *IEEE Journal of Solid State Circuits*, Vol. 31, No. 9, Sept. 1996, pp. 1314 – 1319

Chapter 5

Layout and Experimental Results

Chapter Overview- *This chapter describes the layout of the circuits and presents the results obtained from measuring prototypes. Performance of each power amplifiers is characterized as well as simulations of the synthesized circuits are presented.*

5.1- LAYOUT

We made an experimental prototype that was fabricated in 0.35um CMOS process from AMS, and the die was encapsulated in JLCC68 package. The general picture is shown in the figure 5.1 and 5.2. The CAD environment applied was CADENCE (layout editor VIRTUOSO and simulator tool SPECTRE).In this chip we included three amplifiers:

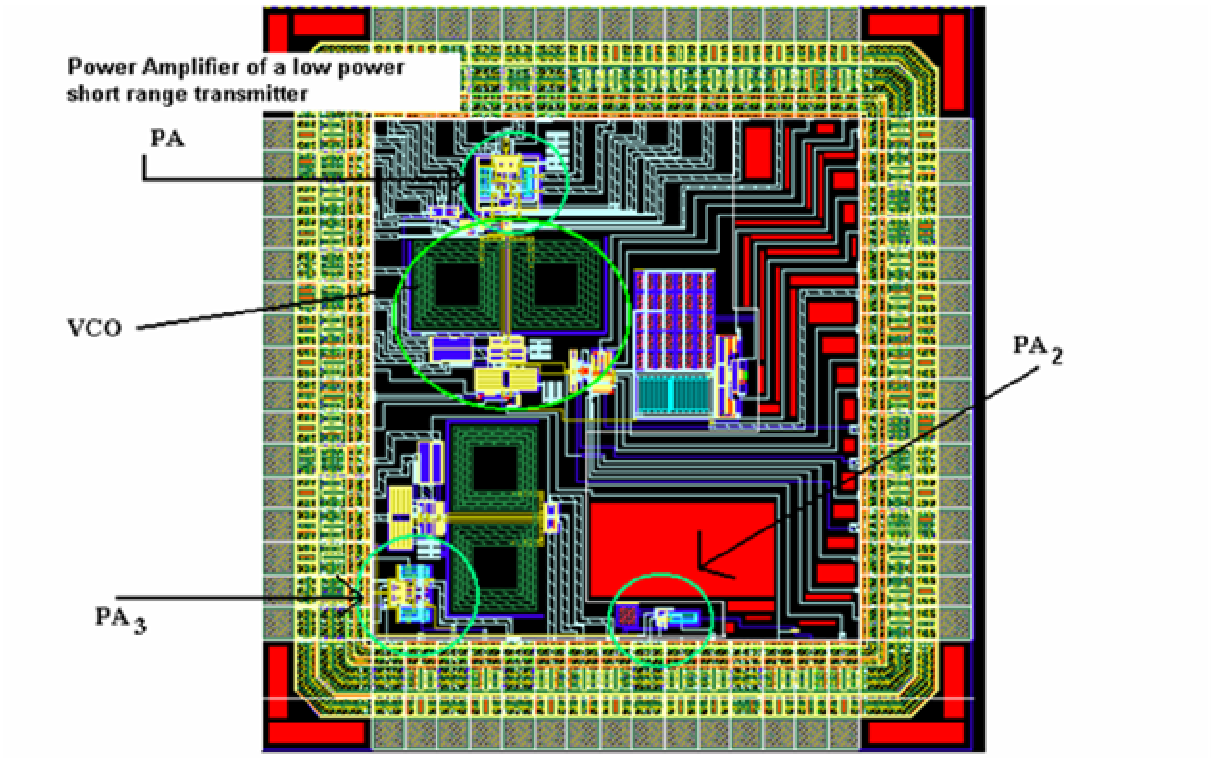

Figure 5.1: An overview of the prototype and building blocks

In the figure 5.1, we have marked specifically the followings blocks:
PA : Power Amplifier of a low power short range transmitter. It is the power amplifier that is driven by a VCO
PA $_2$: It is the optimum amplifier stage
PA $_3$: It is a copy of the PA for testing, it was drawn alone in order to test and to compare measurements obtained from PA

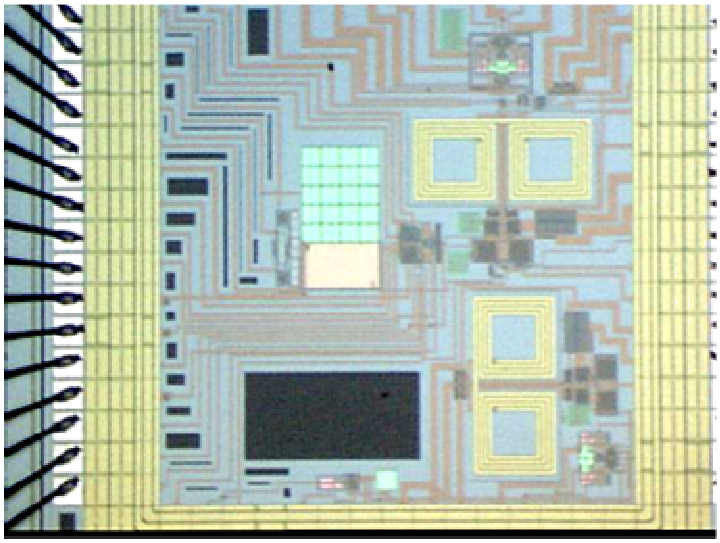

Figure 5.2: Picture of die

In the next section, we show the layout of each block together with its schematic.

It was also important to underline that adequate layout techniques were employed to obtain a good performance in the RF device and particular care was taken with the followings issues:

- To reduce the contribution of the poly resistance to the gate resistance to less than a few ohms, the MOS transistors have been built with as many fingers as possible.

- All PAs were surrounded by ground and V_{DD} connection, that is a double guard ring so that reduce the coupling to other signals and protect output MOS transistor which were designed to directly attack an unprotected output pad. (See Appendix D)

- The inductance and capacitance of the wire bond at the output were taken into account in simulations and they were absorbed as part of the matching network as we discuss in the section 5.3

- The current density and its maximum allowed for each metal layer was studied, specifically in the case of the output MOS transistor due to the high peak current consumption (around 10mA)

- The power amplifier employed as output of the VCO has been laid out as much symmetrical as possible so as not to have different parasitic effects for each half amplifier and in order to get good differential output with reduced second order harmonics.

5.2 TEST SETUP

The fabricated amplifiers were characterized by mounting them on a printed circuit board suitable for RF applications.The chip was soldered directly on the board to decrease the parasitic effects and to get an efficient impedance transformation, surface mounted components were used. The test setup includes the following

equipments:
For RF measurements:

- HP 8546 A (9kHz - 6.5 GHz Spectrum Analyzer and EMI Receiver)
- Gigatronics 6061 A (RF Signal Generator 10KHz - 1050MHz).

To analyze DC characteristics, biasing and consumption measurement:

- HP4155 (Semiconductor Parameter Analyzer).

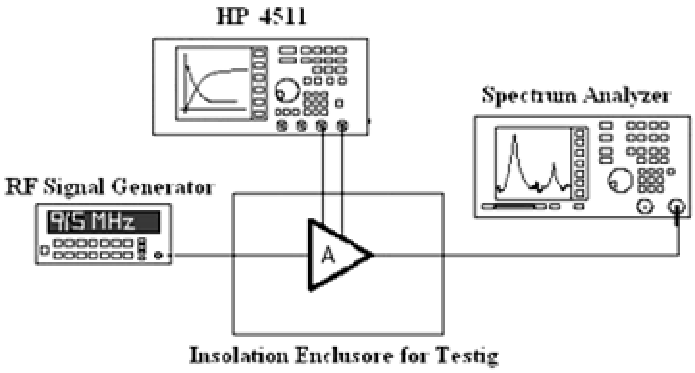

Figure 5.3: Schematic of the test setup to evaluate the prototypes. The ground connections of the test equipments are not shown

5.3 OPTIMUM AMPLIFIER STAGE

In order to achieve high gain levels in an amplifier, gain stages are often cascaded providing an overall gain of the product of the gain of each of the individual stages (see figure 2.6**:** a four stage power amplifier).
First of all we study the optimum amplifier stage that was designed in the Chapter 4, which can be considered as a stage of the cascade and whose architecture is presented in figure 5.4 and layout in figure 5.5:

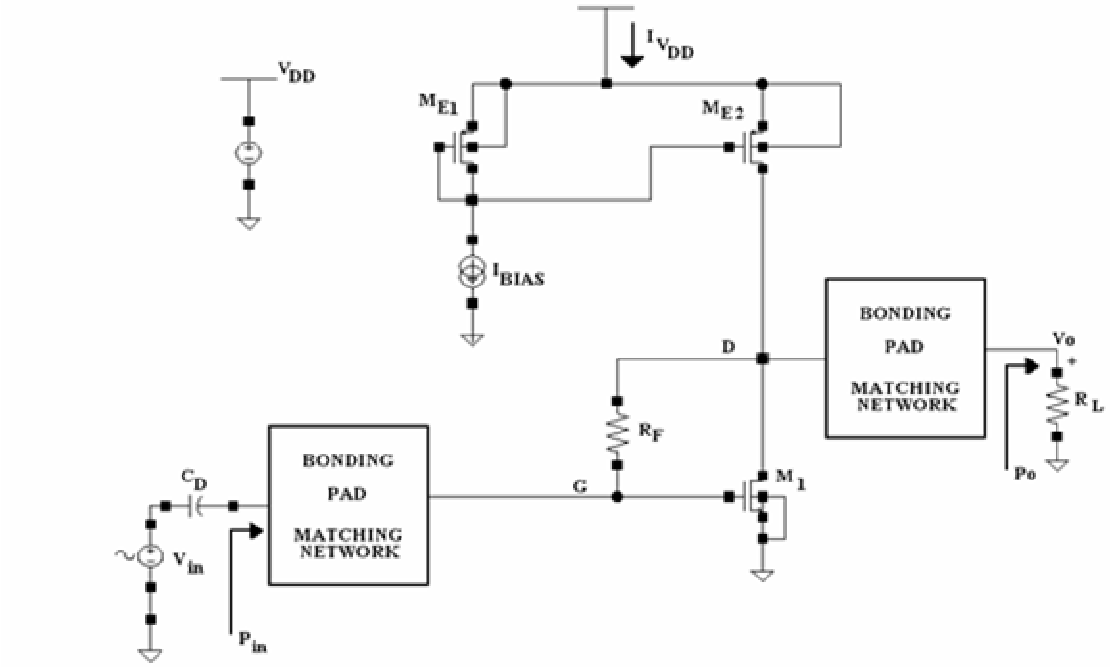

Figure 5.4: Optimum Amplifier Stage PA_2. Schematic

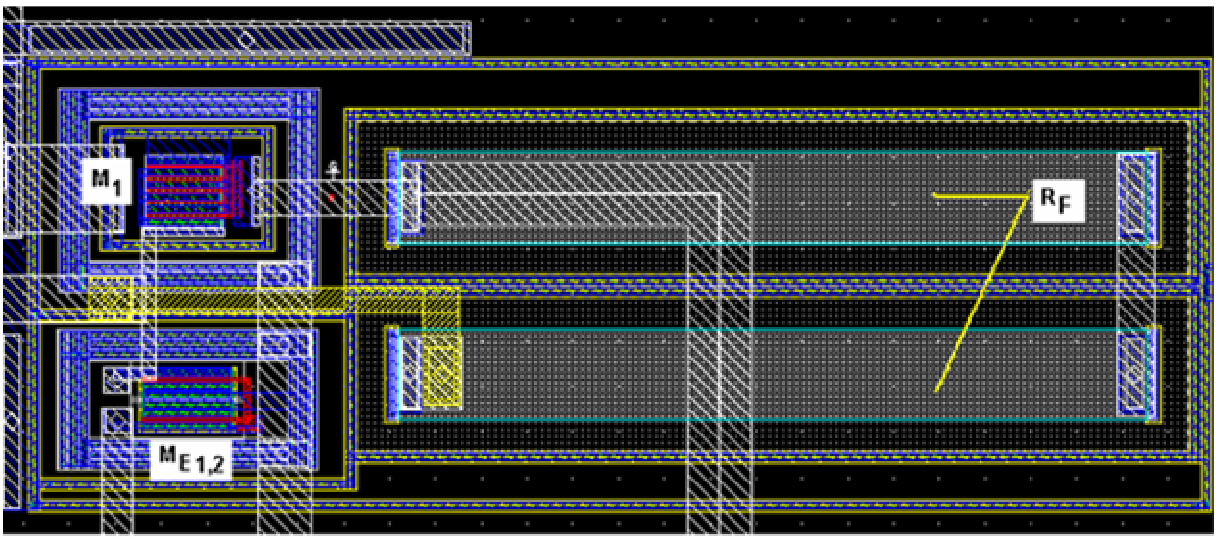

Figure 5.5: Optimum Power Amplifier PA_2 .Layout overview

The purpose of the network impedance transformation is to transform the load impedance to the value needed by the amplifier, as we have discussed in chapter 4. This network impedance transformation was built using the Tool SMITH V1.91 [1]. The network is presented in the figure 5.6, where we have the ideal network (A) and its implementation with standard components (B)

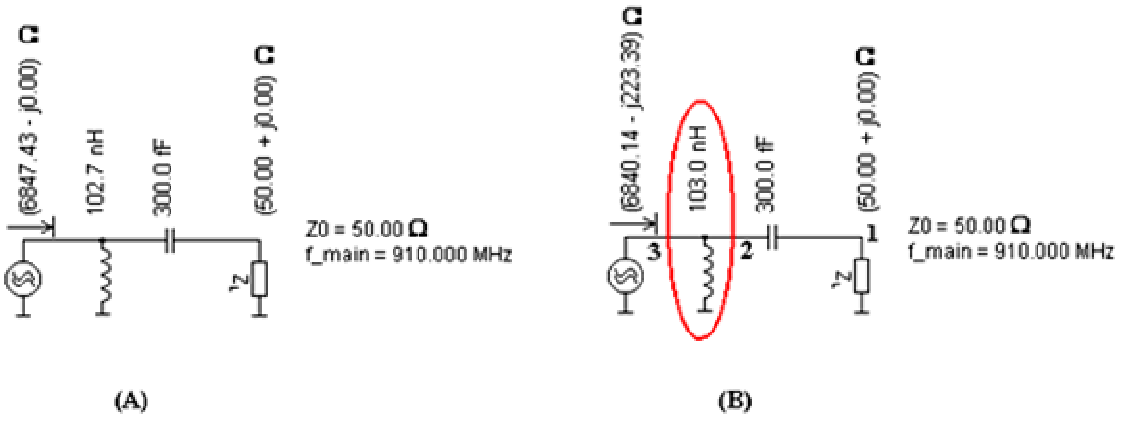

Figure 5.6: Network impedance transformation for PA_2: (A) ideal network - (B) implementation with standard components

Ideally, we would have to use the network presented in figure 5.6 (B) as load impedance of the power amplifier as follow:

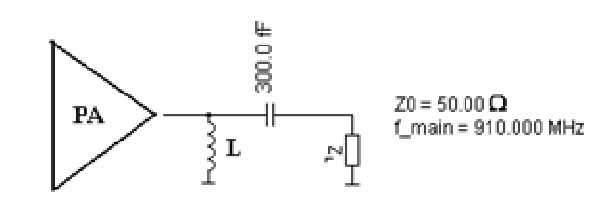

Figure 5.7: Impedance Transformation Network (where L=103nH)

From figure 5.8, it is important to remark that the only use of the impedance transformation network is not enough due to the package and pads will influence the behavior of the circuit, so, it is important a good simulation with those parasitics as well. In this way, more realistic situation is presented in figure 5.8, where L_b is the bonding inductance and C_b package parasitic capacitor.
According with this idea, figure 5.8, explains that it is necessary to add an inductor Lr in order to form a resonant tank with the package and pad parasitic capacitances. This assures that the power amplifier does not see the parasitic effects. No power gain degradation is caused by these parasitic elements because the output amplifier only "see" the effects of the impedance transformation network, which purpose is only to transform the antenna impedance in the impedance wanted at the output of the amplifier.
With the process and package specifications, we run simulations with L_b=5.6nH, and C_b=0.5pF and by trial and error, that was performed through simulation and we selected the best inductance Lr which provides the resonant behavior wanted.

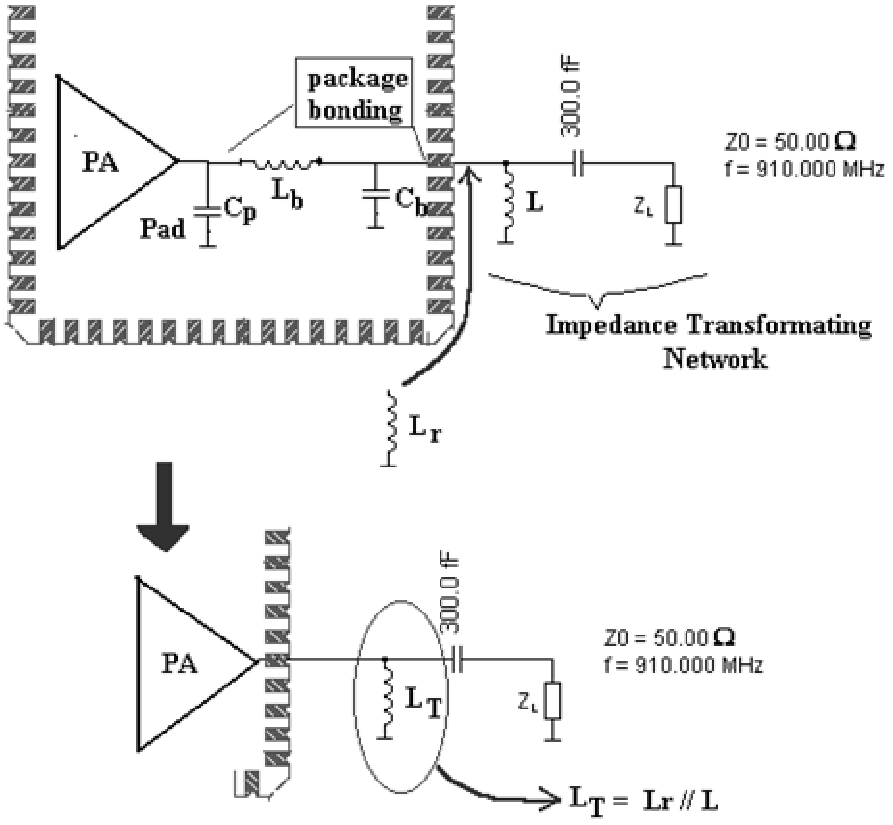

Figure 5.8: Modifications in the external network which provides behaviour independent of the parasitic effect of the package and pad at a given frequency

Then, the total inductor value L_T is achieved, resulting in our case L_T=14.7nH (that is made with series of standard inductor L=10nH and 4.7nH)

5.3.1-Measurement and Simulation Conditions

Measurement Setup Conditions: I_{BIAS} =0.25mA (see figure 5.4)
V_{DD} =3V

Power Source: Input Power =-19dBm

A PSS analysis with SpectreRF was performed in order to estimate the reflection coefficient Γ at the input of the amplifier, which results Γ =0.9785.Thus, the input power to the amplifier is:

$$Pin_A = \left(1-\Gamma^2\right)P_{in} = -32.71dBm \ \ (0.54\mu W) \tag{5.1}$$

The next picture shows the result that was taken from the Spectrum Analyzer. Clearly, the output power is lower than the value desired, and no resonant peak is observed.

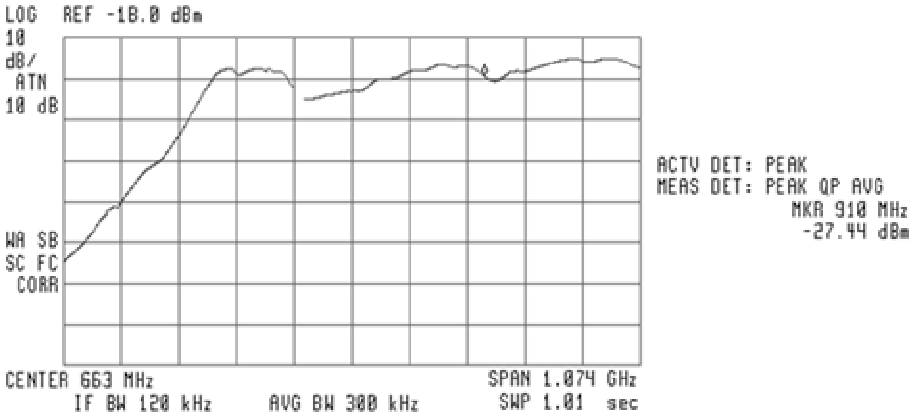

Figure 5.9: First measurement failed at 910.9MHz.

After that, by trial and error, the output network was better adjusted and L_T was changed from 14.7nH to 8.2nH. The result is shown in the figure 5.10 and 5.11 where good agreement with the simulation results has been found thus confirming the correct power gain of the amplifier.

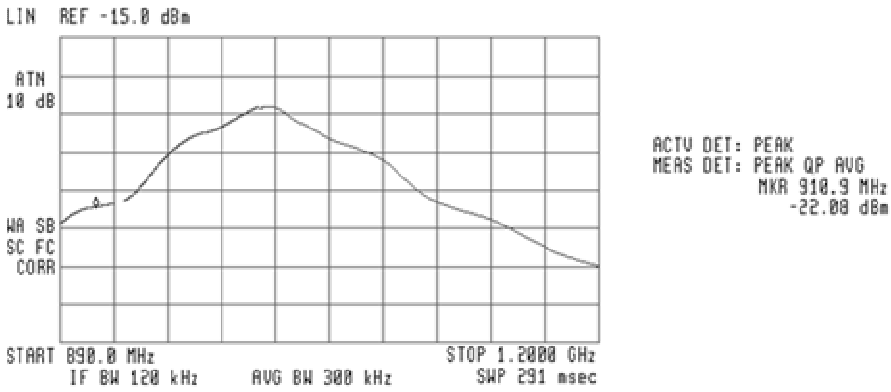

Figure 5.10: Output power at 910.9MHz.

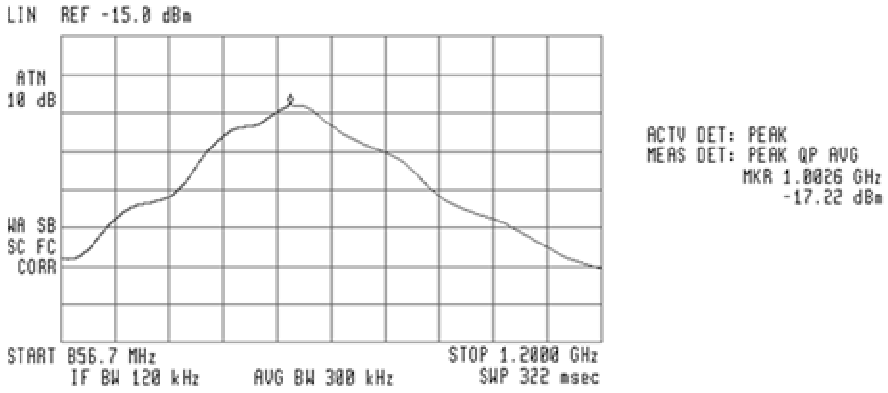

Figure 5.11: Output power at 1GHz

We present two tables. In table 5.1 we compare the DC values and in table 5.2 the AC values.

	G (DC)	D (DC)	$I_D(V_{DD})$
Simulated	0.75 V	0.75 V	0.53 mA
Measured	0.68 V	0.68 V	0.54 mA
Estimated	0.68 V	0.68 V	0.50 mA

Table 5.1: Simulated, measured as well as estimated DC characteristics of the PA_2

	Pout	Gp (Power Gain)	G (Peak input voltage)	D (Peak output voltage)	A (Amplitud-Gain)
Simulated	-21.78dBm	10.93 dB	0.092 V	0.36 V	11.85 dB
Measured	-22.08dBm	10.6 dB	(2)	(2)	(2)
Estimated	-16.10dBm (1)	11 dB	0.1 V	0.6V	14 dB

Table 5.2: Power and voltage gain and AC characteristics of the PA_2 at 910MHz

(1) It is achieved in the hypothetical situation without wire bond inductances and package capacitances as it was applied in table 4.8.In order to get an accurate simulation, the package model and wire bonding were included in the simulation. The values for the specific package used are given by the manufacturer and it explains the difference with the estimated value. The wire bond and package capacitances change the output power but do not change the power gain when the impedance transformation network is properly adjusted.

(2) Voltage measurement is not available from the Spectrum Analyzer and EMI Receiver:

According to figure 5.11, it could be seen that the maximum power peak is moved toward 1GHz. The fact that the maximum output power was moved to around 1GHz does not imply that the impedance transformation is inefficient, because we have to take into account that the input impedance of the amplifier depends on the frequency and consequently the factor Γ too.

This hypothesis is easily verifiable by simulation, where by analysis with SpectreRF, we can see that the parameter Γ decrease at higher frequency. More specifically, at 1GHz Γ=0.9615 and the new power balance is:

$$Pin_A = \left(1-\Gamma^2\right)P_{in\,SRC} = -30.22dBm \;\; (0.95\mu W) \tag{5.2}$$

Thus, assuming power gain 11 dB (Table 5.2) that is not all correct because this values was taken at 910MHz, we have output power Pout=-19.22dBm.This has a good agreement with the simulation at first approximation. Finally, coming back to the output transformation network and in order to test others inductor values, we present in figure 5.12 the results whit L_T=12.5nH. This shows, and opens further discussion, about how much care must be taken during the design of the input and output matching networks.

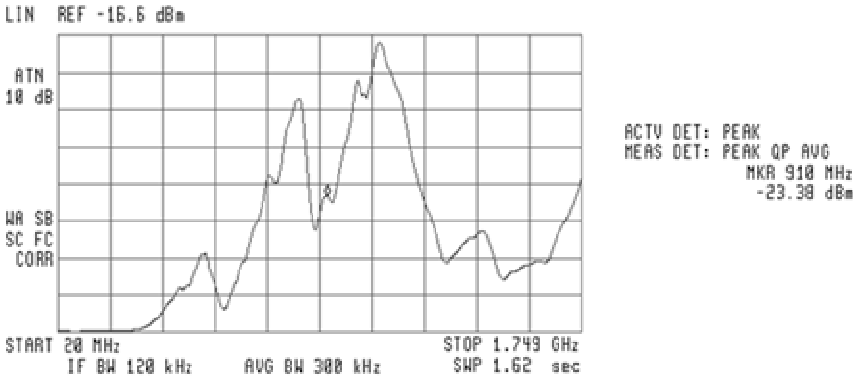

Figure 5.12: Variations in the power gain changing the inductance of the output network from 8.2nH to 12.5nH.

5.4 POWER AMPLIFIER OF A LOW POWER SHORT RANGE TRANSMITTER

The power amplifier of a low power short range transmitter was designed in the Chapter 4 and its architecture is presented in figure 5.13 and layout in figure 5.14.

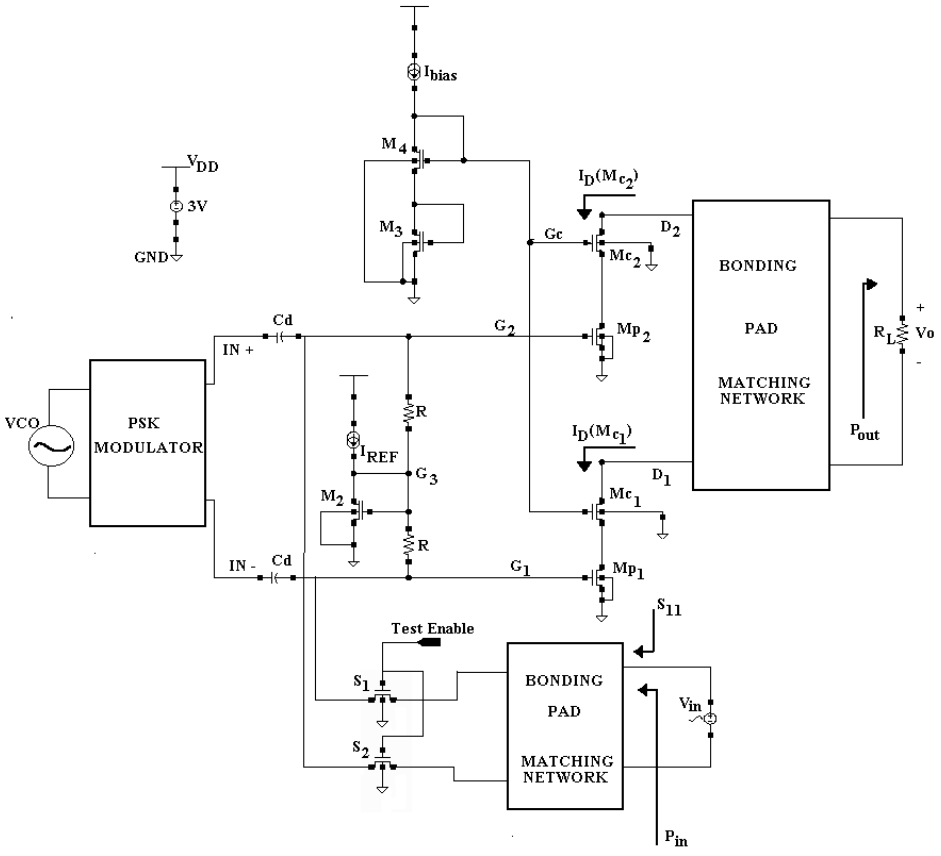

Figure 5.13: Power amplifier of a low power short range. Schematic

From figure 5.13, having the original design from chapter 4, we added switches S_1 and S_2 designed in order to provide an independent input for testing.

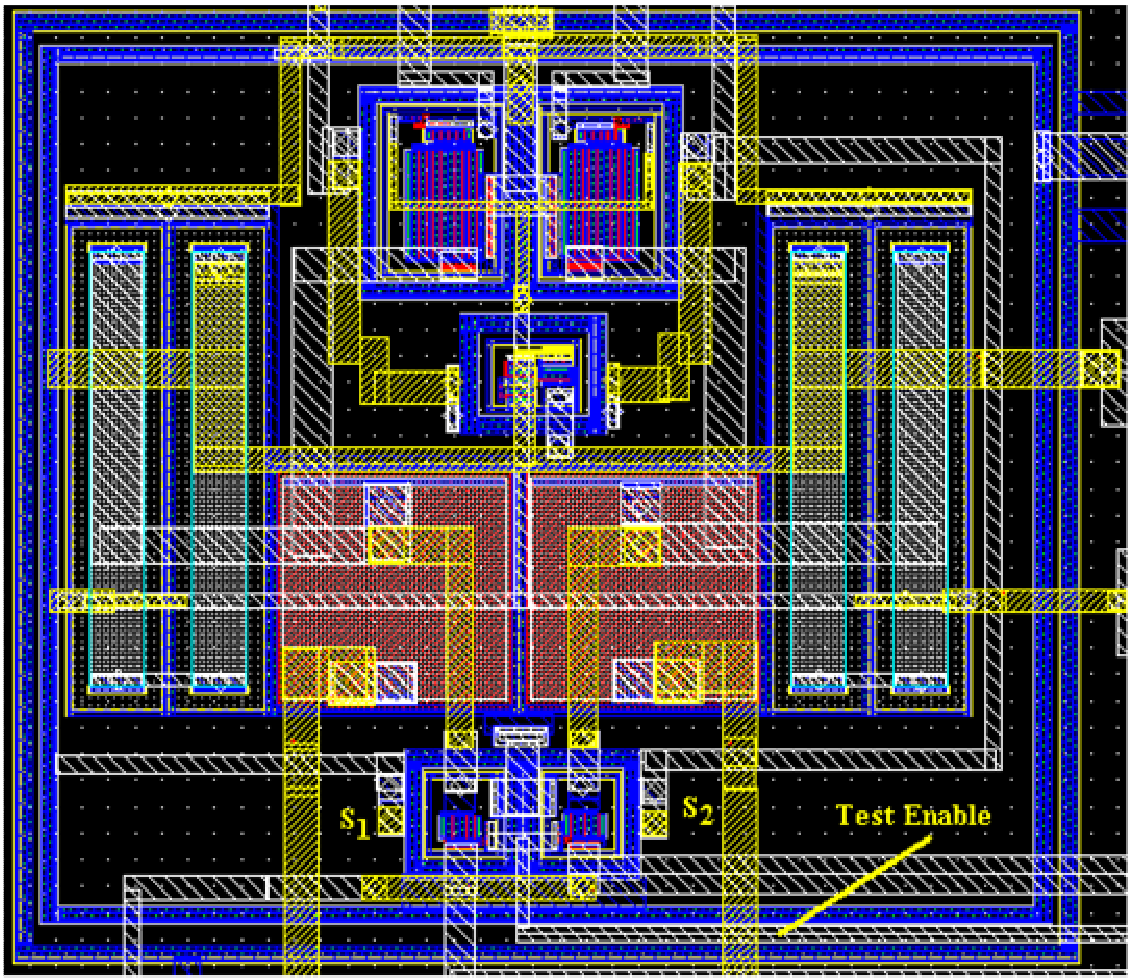

Figure 5.14: Power amplifier of a low power short range. Layout overview

In the next figure 5.15 we present a picture of the die:

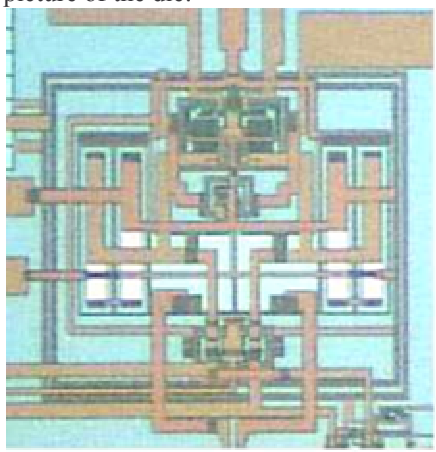

Figure 5.15: Picture of die

In the next figure 5.16, a detailed output MOS transistors (Mp_1 and Mp_2) with cascode (Mc_1 and Mc_2) as well as a part of the circuit for biasing are presented.

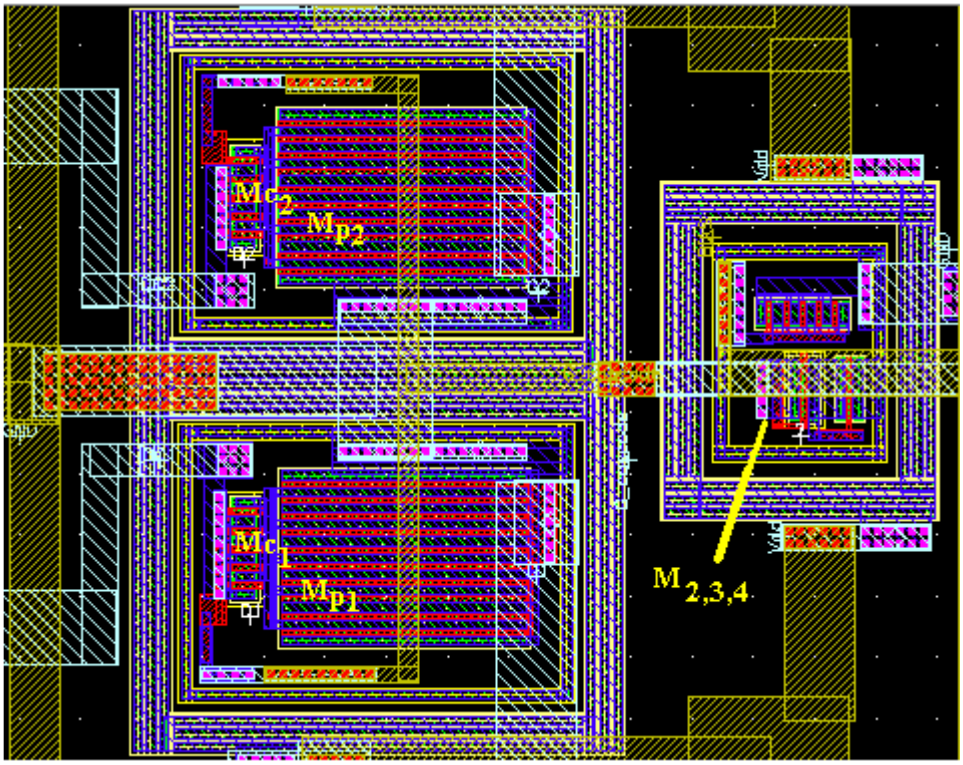

Figure 5.16: Detail of the output MOS transistors with the cascode and bias. Layout overview

5.4.1-Measurement and Simulation Conditions

Measurement Setup Conditions: I_{REF} =35 µA (see figure 5.13)
I_{Bias} =0.2mA (see figure 5.13)
V_{DD} =3V

Power Source: Input Power =2.75dBm (1.88mW)

We present two tables. In table 5.3 we compare the DC values and in table 5.4 the power gain values.

	$G_2=G_1=G_3$ (DC)	D_1 =D2 (DC)	Gc (DC)	$I_D(Mc_1) = I_D(Mc_2)$ (BIAS)
Simulated	0.76 V	3 V	2.68 V	1.45 mA
Measured	0.62 V	3 V	2.82 V	1.22 mA
Estimated	0.68 V	3 V	(1)	1.32 mA

Table 5.3: Simulated, measured as well as estimated DC characteristics of the power amplifier of a low power short range

(1) This value is not predicted by the tool.

A PSS analysis with SpectreRF was performed in order to estimate the reflection coefficient Γ at the input of the amplifier, which results Γ=0.9505. Thus, the input power to the amplifier is:

$$Pin_A = \left(1-\Gamma^2\right)P_{in} = -7.4dBm \ \ (0.18mW) \tag{5.3}$$

	Pout	Gp (Power Gain)
Simulated	-0.51dBm	6.9 dB
Measured	(1)	(1)
Estimated	0 dBm	9.86 dB

Table 5.4: Power and voltage gain and AC characteristics of the power amplifier of a low power short range

(1) Preliminary results indicate that measurements of the power amplifier of a low power short range transmitter need to be repeated more carefully.
Besides the circuit's biasing characteristics have been measured and correct functionality has been found, the power amplifier seems to amplify power but serious power gain degradation was observed when operated.

In the figure 5.17 we can see the output power gain that shows the degradation of the output power.

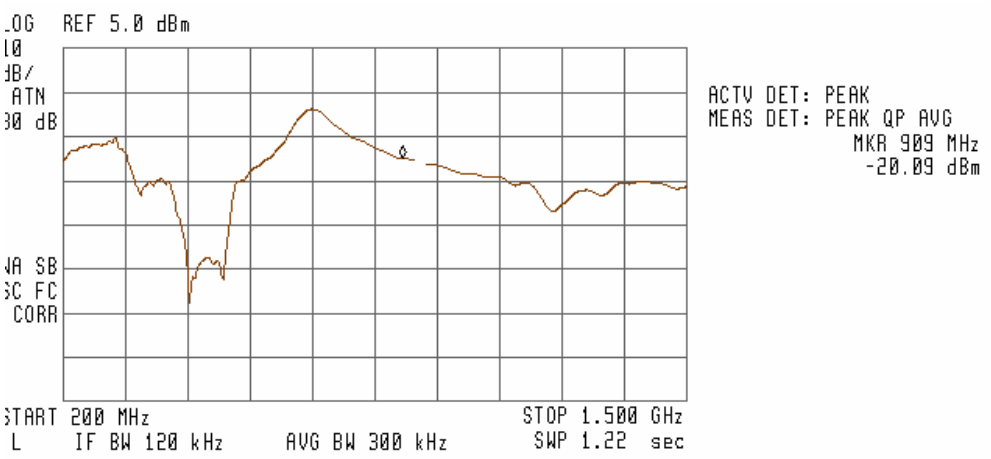

Figure 5.17: Output power at 909 MHz

The problems presented by this power amplifier were mostly due to problems with the selected impedance transformation network, which in our opinion is the main cause of low performance. It was not expected because complete analysis in simulation study was performed without important variations.

On the other hand, we can calculate the simulated efficiency as follow:

$$\eta = \frac{P_{out}}{P_{DC}} = \frac{0.89mW}{V_{DD}.2\left(i_{D,peak}/\pi\right)} \tag{5.4}$$

Where the current $i_{D,peak}$ represents the drain current peak of the output transistor $Mp_{1,2}$, and whose value is $i_{D,peak}$=2.14 mA

Thus, an estimation of the efficiency is: $\eta = \frac{0.89mW}{V_{DD}.2(2.14\,mA/\pi)} = 0.218 \quad (21.8\%)$ (5.5)

Finally, we test the compression point 1dB as follow:

From Table 4.10 and equation A.15 (see appendix A), we have:

$$\frac{H_3(f_o, f_o, -f_o)}{H_1(f_o)} = 0.12.\frac{4}{3V_{gs}^2} = 0.12.\frac{4}{3}\frac{1}{(0.45V)^2} = 0.79 \quad (5.6)$$

(With f_o=910MHz)

Using equation A.28 (see appendix A):

$$A_{1dB} \approx \sqrt{0.145.\frac{|H_1(f_o)|}{|H_3(f_o, f_o, -f_o)|}} = 0.423V \quad (5.7)$$

Finally, the compression point 1dB is : $P_{1dB} = \frac{A_{1dB}^2}{2.\,50\Omega} = 1.8mW$ (5.8)

A PSS analysis with SpectreRF was performed in order to estimate the compression point 1dB, whose value results $P_{1dB} \approx 1.518dBm$ or 1.42 mW

A good correlation has been found between compression point 1dB estimated by the tool and calculated by simulation.

5.5 REFERENCES

[1] SMITH V1.91 Demo version freely distributed from The University of Applied Sciences Berne Berne Institute of Engineering and Architecture F. Dellsperger Professor Morgartenstrasse 2c CH-3014 Bern Switzerland Fax. ++41 31 33 30 625 e-mail fritz.dellsperger@hta-be.bfh.ch.

Chapter 6

Conclusions

Chapter Overview - *Conclusions and ideas for future research are presented.*

6.1 CONCLUSIONS

In this work it has been presented a flexible tool to help in the design of low power RF blocks by identifying limiting constraints between current consumption and voltage and power gain. This constitutes the primary focus of this research.
The tool presented in Chapter 4 has been used to introduce the application of the g_m/I_D methodology and the idea of design space exploration toward high frequency operation (910MHz).

Several amplifier topologies were analyzed and simulated whit the foundry provided BSIM3v3 model and good agreement with the tool estimations has been found. It has also been shown the existence of an optimum inversion level which gives the minimum power consumption for a given gain, or equivalently, the maximum gain for a given consumption. This optimum inversion level appears in different types of amplifiers and in varied technologies and finally it has been shown the viability of working, with 0.35µm technologies, in moderate inversion, at 910MHz which gives a better compromise between speed and consumption.

The tool was partially verified with experimental prototypes. A 910 MHz power amplifier for low power short range transmitter capable to deliver 0dBm to an antenna has been designed and implemented in standard 0.35µm AMS process in order to enable a wireless sensor network operation as well as an optimum amplifier stage has been designed to check the operation at the predicted optimum inversion level.

6.1.1 Performance

The implementations of these architectures (an optimum amplifier stage and a power amplifier of a low power short range transmitter) were investigated in the chapter 4. After a complete analysis, each block was simulated for performance estimation and good agreement between simulation and tool estimation has been found. For this amplifier it is pending an adjustment of the matching networks yet.

The fabricated optimum amplifier stage has been measured and characterized and seems to match the simulation and measurement results with tool estimations as we have discussed in the chapter 5.

On the other hand, preliminary results indicate that measurements of the power amplifier of a low power short range transmitter need to be repeated more carefully.
Besides the circuit's biasing characteristics have been measured and correct functionality has been found, the power amplifier seems to amplify power but serious power gain degradation was observed when operated.
The problems presented by this power amplifier were mostly due to problems with the selected impedance transformation network, which in our opinion is the main cause of low performance. It was not expected because complete analysis in simulation study was performed without problem.

Moreover, more careful study of issues such as the spread of standard components as well as inductor loss and non considered parasitic capacitances or signal coupling from place to place at higher frequencies need implementing .

6.2 FUTURE WORK

Additional work is needed to extend the results of this research and there are also still much to do. In this way, this work also identifies at least four major directions

A first priority is:

● As we have mentioned previously, the problems presented by the power amplifier of a low power short range transmitter prototype were not expected because analysis and simulation study was performed without problem.
In this way, new simulation studies have to include no ideal effects in the impedance transformation network such as dispersion in the components' values and the quality factor Q of inductors and capacitances.
The loss of power gain caused by this problem must not have been negligible as we suppose in the first stage of this work.
A new board is being mounted with different impedance transformation networks to test the performance of this power amplifier.

●The complete effect that the power amplifier has on the VCO should be studied. At the moment no successful measurement was possible. We have observed variations in the oscillation frequency of the VCO due to the connexion with the amplifier.

●The future research efforts should focus on the following effects and how it could be implemented in the tool:

a) The variability of the non quasi-static frequency boundary caused by the spread of slope factor (n) of the technology as it is shown in appendix E.
b) The effects of the size of the MOS cascode as well as the current mirror that biases the power amplifier. Until this moment, these sizes (width W) are not considered a variable in our tool. By exploring the variations in the power and voltage map due to variations in the biasing circuits we may find other optimum points.
c) The dispersion in the power and voltage gain map caused by spread and losses in the load impedance and impedance transformation network.

Finally:

●The tool presented here should be extended to other architectures, to explore major advantages and disadvantages in power consumption optimization. It would be helpful to improve the user interface to explore more complicated architectures and its constraints and tradeoffs.

Appendix A

Introduction to Volterra Series & Effects of Nonlinearity

A.1 Volterra Series Representation

In the next section a brief introduction to the concept of Volterra Series and how it is used in calculating distortion terms in transistors, amplifiers and other systems is shown. We utilize the notation of the bibliography [A.1][A.2] [A.3]

A linear and causal system with memory can be described by the convolution representation as:

$$y(t) = \int_{-\infty}^{\infty} h(u)x(t-u)du \tag{A.1}$$

Where:
$x(t)$: is the input
$y(t)$: is the output
$h(t)$: is the impulse response of the system

A nonlinear system without memory can be described with a Taylor series representation as follows:

$$y(t) = \sum_{n=1}^{\infty} a_n [x(t)]^n \tag{A.2}$$

Where, again:
$x(t)$: is the input
$y(t)$: is the output
a_n: are the coefficients of behavior

Without memory imply that the output is not a function of $x(t-\tau)$ where τ is some delay.
The Volterra series is a series that combines the above two representations to describe weakly nonlinear systems with memory as follows:

$$y(t) = \sum_{n=1}^{\infty} \int_{-\infty}^{\infty} du_1 ..... \int_{-\infty}^{\infty} du_n h_n(u_1, ...u_n) \prod_{r=1}^{n} x(t-u_r) \tag{A.3}$$

$$y(t) = \int_{-\infty}^{\infty} du_1 h_1(u_1)x(t-u_1) + \int_{-\infty}^{\infty} du_1 \int_{-\infty}^{\infty} du_2 h_2(u_1,u_2)x(t-u_1)x(t-u_2)$$
$$+ \int_{-\infty}^{\infty} du_1 \int_{-\infty}^{\infty} du_2 \int_{-\infty}^{\infty} du_3 h_3(u_1,u_2,u_3)x(t-u_1)x(t-u_2)x(t-u_3) \quad \text{(A.4)}$$
$$+ .....$$

Where, again:

$x(t)$: is the input

$y(t)$: is the output

$h_n(u_1,u_2.....u_n)$: are called the Volterra kernels or higher order impulse response of the systems [A.2]

u_i : are time variables instead of t_i to distinguish them from t.

More succinctly, we can find in the literature [A.2] the following notation:

$$y(t) = H_1(x(t)) + H_2(x(t)) + H_3(x(t)) + ... \quad \text{(A.5)}$$

Where H_n represent the n-th operator with kernel h_n.

The first three terms in (A.3) have been explicitly written out in (A.4) .The first term is the familiar convolution integral, where $h_1(u_1)$ will be recognized as the familiar impulse response. The representation of the nonlinearity as a summation of operators operating on a signal allows us to determine the contribution of nonlinearity individually and the dominant contribution would be identified and analyzed.

Just as (A.3) is analogous to n-convolution, there are n-Laplace and n-Fourier transform and they are defined by:

$$H_n(s_1,.....s_n) = \int_{-\infty}^{\infty} du_1 ..... \int_{-\infty}^{\infty} du_n h_n(u_1,.....u_n) e^{-s_1 u_1} .....e^{-s_n u_n} \quad \text{(A.6)}$$

and

$$H_n(f_1,.....f_n) = \int_{-\infty}^{\infty} du_1 ..... \int_{-\infty}^{\infty} du_n h_n(u_1,.....u_n) e^{-jw_1 u_1} .....e^{-jw_n u_n} \quad \text{(A.7)}$$

Where: $s_i = jw_i$

$w_i = 2\pi f_i$

These frequency domain representations are useful because they are much simpler to calculate than the time domain representations, for this reason, obtaining the Volterra series coefficients is the key to calculate the harmonic distortion, intermodulation, gain compression and cross modulation Finally, the traditional frequency domain input-output representation becomes:

$$Y(f) = H_1(f)X(f) + \int_{-\infty}^{\infty} df_1 H_2(f_1, f-f_1)X(f_1)X(f-f_1)$$
$$+ \int_{-\infty}^{\infty} df_1 \int_{-\infty}^{\infty} df_2 H_3(f_1,f_2,f-f_1-f_2)X(f_1)X(f_2)X(f-f_1-f_2) \quad \text{(A.8)}$$
$$+ .....$$

A.2 Output from Volterra Kernels

The spectrum of an output signal can be expressed in terms of the n-th transfer function. If the input signal is a single sinusoid $x(t) = A\cos(w_o\, t)$ the spectrum of the output is given by [A.4]:

$$y(t) = \sum_{n=1}^{\infty}\left(\frac{A}{2}\right)^n \sum_{k=0}^{n} n!\frac{\exp\left(j(2k-n)w_o t\right)}{k!(n-k)!}H_{k,n-k}(f_o) \tag{A.9}$$

Expanding this expression for a few different values:

$$\begin{aligned} y(t) = &\left[\frac{A^2}{2}H_2(f_o,-f_o)+.....\right] \\ &+e^{jw_o t}\left[\frac{A}{2}H_1(f_o)+\frac{3A^3}{8}H_3(f_o,f_o,-f_o)+.....\right] \\ &+e^{j2w_o t}\left[\frac{A^2}{4}H_2(f_o,f_o)+.....\right] \\ &+e^{j3w_o t}\left[\frac{A^3}{8}H_3(f_o,f_o,f_o)+.....\right] \\ &+e^{-jw_o t}\left[\frac{A}{2}H_1(-f_o)+\frac{3A^3}{8}H_3(-f_o,-f_o,f_o)+.....\right] \\ &+e^{-j2w_o t}\left[\frac{A^2}{4}H_2(-f_o,-f_o)+.....\right] \\ &+e^{-j3w_o t}\left[\frac{A^3}{8}H_3(-f_o,-f_o,-f_o)+.....\right] \end{aligned} \tag{A.10}$$

For example, consider again the first harmonic of the expansion of $y(t)$ in (A.9), the three first terms are shown:

$$e^{jw_o t}\left(\frac{A}{2}H_1(f_o)+\frac{3A^3}{8}H_3(f_o,f_o,-f_o)+\frac{5A^5}{48}H_5(f_o,f_o,f_o,-f_o,f_o)+.....\right) \tag{A.11}$$

The first term dominates for small input, this term is the linear transfer function, and it corresponds to the linear gain. As the input gets larger, the second term starts to contribute and it represents the gain compression.
Thus, Volterra series give us a simple method of calculating distortion parameters, for example, the 1-dB compression point of a system as we will show promptly. Following the definition for harmonic distortion, that is related to Volterra kernels in the following way [4]:

$$HD_2 = \frac{A}{2}\frac{H_2(f_o, f_o)}{H_1(f_o)} \tag{A.12}$$

$$HD_3 = \frac{A^2}{4}\frac{H_3(f_o, f_o, f_o)}{H_1(f_o)} \tag{A.13}$$

Similarity, intermodulation could be expressed as:

$$IM_2 = A\frac{H_2(f_o, -f_o)}{H_1(f_o)} \tag{A.14}$$

$$IM_3 = \frac{3}{4}A^2\frac{H_3(f_o, f_o, -f_o)}{H_1(f_o)} \tag{A.15}$$

Where A represents the amplitude of the input voltage.

A.3 Applicability of Volterra Series

Volterra series give a method of calculating small distortion terms in weakly nonlinear systems. The idea of what exactly mean *"weakly nonlinear systems"* is the following: a weak nonlinear system implies that the infinite sums will converge and converge rapidly; otherwise, the time to compute the sum increases exponentially.
If the nonlinearity is *"too strong"*, the sums will converge or not. It depends on the kind of nonlinearity, but if converges require a long time for computing. Despite the fact that the sum converges, it is important to remark that Volterra series are impractical in strongly nonlinear problems due to the large computing time[A4].

A.4 The Harmonic Input Method

Considering the following circuit that represents the model for the MOS transistor in figure A.1, the kernels H_n in the frequency domain are going to be determined by using the Harmonic Input Method.

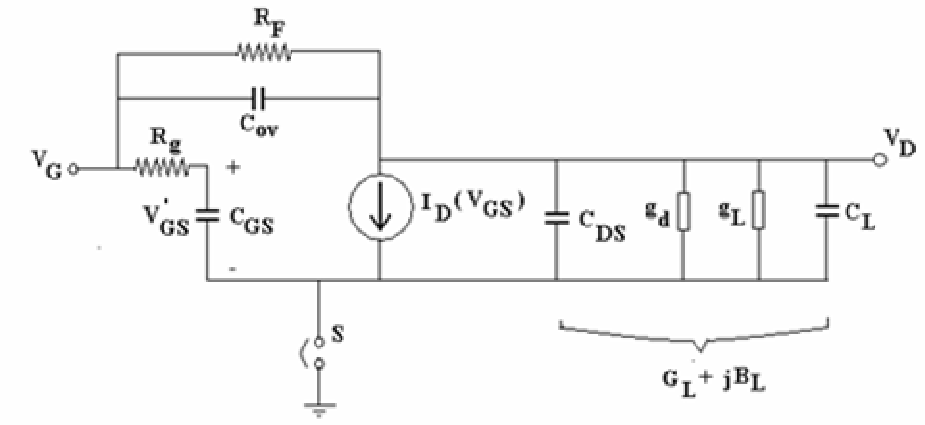

Figure A.1: Representation of the MOS transistor to calculate the kernels H_n.

The nonlinearities considered is due to the transconductance g_m .This nonlinearities are associated with de I-V characteristics of the drain current: $I_D = I_D(V_{GS})$. Where we the total drain current is the DC current and signal current: $I_D = I_{bias} + i_d$, and $V_{GS} = v_{GS} + v_{gs}$, where v_{GS} is DC voltage and v_{gs} is signal voltage.

This current drain signal characteristic would be approximated using the first three term of a power series expansion (see appendix B) in the following way:

$$i_d \approx g_m v_{gs} + g_m k_2 v_{gs}^2 + g_m K_3 v_{gs}^3 \tag{A.16}$$

Then, from figure A.1 we define the total load admittance: $y_L = g_l + j\omega C_L$

And: $B_l = \omega C_T = \omega(C_{DS} + C_L)$

$G_L = g_d + g_L$

(C_L and g_L are representing the load admittance)

Assuming Rg=0, it is possible to write the equation (A.17)

$$g_m v_{gs} + g_m K_2 v_{gs}^2 + g_m K_3 v_{gs}^3 = y_F(v_{gs} - v_{ds}) + C_{OV}\frac{d(v_{gs} - v_{ds})}{dt} - G_L v_{ds} - C_T \frac{d v_{ds}}{dt} \tag{A.17}$$

To apply the harmonic input method, we assume that $v_{gs} = e^{jw_1 t}$, and putting it into equation (A.17) we have to separate terms that have the exponential form $e^{jw_1 t}$ because we are looking for outputs that could be written as $v_{ds} = ae^{j\omega_1 t}$

Thus we have:

$$g_m = y_F - y_F v_{ds} + C_{OV} j\omega_1 (1 - v_{ds}) - G_L v_{ds} - C_T j\omega_1 v_{ds} \tag{A.18}$$

After some manipulation, it is possible to write H_1 as follow:

$$v_{ds} = H_1(j\omega_1) = -\frac{g_m - y_F - C_{OV} j\omega_1}{y_F + j\omega_1 C_{OV} + G_L + j\omega_1 C_T} = -\frac{y_{dg}}{y_{dd} + y_L} \tag{A.19}$$

Where y_{dg}, y_{dd} have been explained in the chapter 3.

To calculate H_2 we assume that $v_{gs} = e^{j\omega_1 t} + e^{j\omega_2 t}$, and putting it into equation (A.17) we have to separate terms that have the exponential form $e^{j(\omega_1+\omega_2)t}$ because we are looking for outputs that could be written as $v_{ds} = ae^{j(\omega_1+\omega_2)t}$. Thus we have:

$$2g_m K_2 = -y_F v_{ds} - C_{OV} j(\omega_1 + \omega_2)(v_{ds}) - G_L v_{ds} - C_T j(\omega_1 + \omega_2) v_{ds} \tag{A.20}$$

After some manipulation, it is possible to write H_2 as follow:

$$v_{ds} = H_2(\omega_1, \omega_2) = -\frac{2g_m K_2}{y_F + G_L + j(\omega_1 + \omega_2)(C_{OV} + C_T)} = -\frac{2g_m K_2}{(y_{dd} + y_L)|_{\omega 1+\omega 2}} \quad \text{(A.21)}$$

To calculate H_3 we assume that $v_{gs} = e^{j\omega_1 t} + e^{j\omega_2 t} + e^{j\omega_3 t}$, and putting it into equation (A.17) we have to separate terms that have the exponential form $e^{j(\omega_1+\omega_2+\omega_3)t}$ because we are looking for outputs that could be written as $v_{ds} = ae^{j(\omega_1+\omega_2+\omega_3)t}$. Thus we have:

$$6g_m K_3 = -y_F v_{ds} - C_{OV} j(\omega_1 + \omega_2 + \omega_3)(v_{ds}) - G_L v_{ds} - C_T j(\omega_1 + \omega_2 + \omega_3) v_{ds} \quad \text{(A.22)}$$

After some manipulation, it is possible to write H_3 as follow:

$$v_{ds} = H_3(\omega_1, \omega_2, \omega_3) = -\frac{6g_m K_3}{y_F + G_L + j(\omega_1 + \omega_2 + \omega_3)(C_{OV} + C_T)} = -\frac{6g_m K_3}{(y_{dd} + y_L)|_{\omega 1+\omega 2+\omega 3}} \quad \text{(A.23)}$$

A.4 Gain Compression

As it is widely shown in the literature, in most circuits of interest, the output would be a compressive or saturating function of the input. This effect is quantified by the *1dB compression point*, defined as the input signal that causes the small signal gain drop by 1dB.
In the following figure A.2, the input power at which the linear gain of the amplifier has compressed by 1 dB is the 1-dB compression point (in dB)

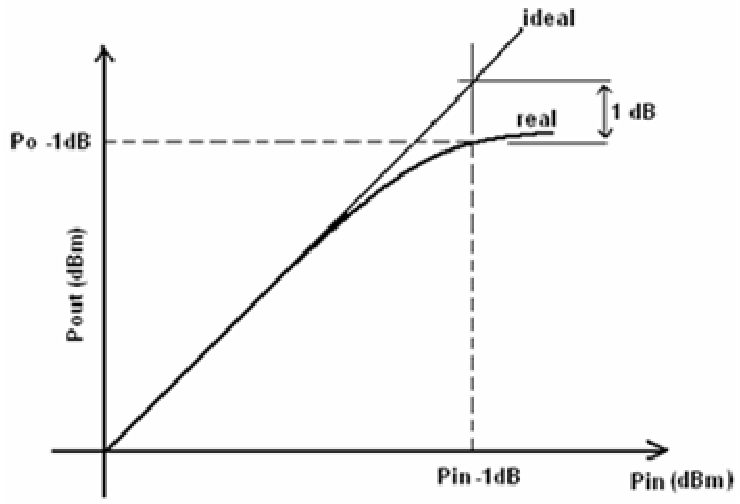

Figure A.2: Representation of the point 1dB compression.

To understand the compressive or saturating effect, from equation (A.10), we take only the dominant contributions at frequency f_o (fundamental frequency) in the output amplitude that could be written as:

$$\left[\frac{A}{2}H_1(f_o)+\frac{3A^3}{8}H_3(f_o,f_o,-f_o)+.....\right] \quad (A.24)$$

Thus, to calculate the 1-dB compression point, we have to find the value A_{1dB} that satisfy the following equation:

$$20\log\left|\frac{A_{1dB}}{2}H_1(f_o)+\frac{3A_{1dB}^3}{8}H_3(f_o,f_o,-f_o)\right| = 20\log\left|\frac{A_{1dB}}{2}H_1(f_o)\right|-1dB \quad (A.25)$$

Or, more easily to understand:

$$20\log\left|\frac{\frac{A_{1dB}}{2}H_1(f_o)+\frac{3A_{1dB}^3}{8}H_3(f_o,f_o,-f_o)}{\frac{A_{1dB}}{2}H_1(f_o)}\right| = -1dB \quad (A.26)$$

Where we expand:

$$\left|1+\frac{3}{4}\frac{A_{1dB}^2H_3(f_o,f_o,-f_o)}{H_1(f_o)}\right| = 0.8913 \quad (A.27)$$

And we have:

$$A_{1dB} \approx \sqrt{0.145.\frac{|H_1(f_o)|}{|H_3(f_o,f_o,-f_o)|}} \quad (A.28)$$

A.5 References

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[A.2] M.Schetzen *"The Volterra and Wiener Theories of Nonlinear Systems "* . New York :Wiley 1980

[A.3] Wei Yu et. *Al " Distortion Analysis of MOS Track-and-Hold Sampling Mixers Using Time-Varying Volterra Series "* IEEE Transactions on Circuits and Systems: Analog and Digital Signal Processing ,VOL 46 No2 February 1999 1057-7130/99$10.00

[A.4] Cherry J.A. 1994, Distortion Analysis of Weakly Nonlinear Filters Using Volterra Series: Chap. 3 http://lanoswww.epfl.ch/studinfo/courses/cours_nonlinear_de/material.htm

Appendix B

Power Series Expansion of The Drain Current

The current drain can be approximated using the first three terms of a power series as follow:

$$i_d \approx g_m v_{gs} + g_m k_2 v_{gs}^2 + g_m K_3 v_{gs}^3 \tag{B.1}$$

We are going to use the ACM model to calculate K_2 and K_3. As we have shown previously in the chapter 3, the I-V characteristic of the MOS transistor is:

$$Vp - Vs = U_T\left(\sqrt{1+i_f} - 2 + Ln\left(\sqrt{1+i_f} - 1\right)\right) \tag{B.2}$$

Where the pinch of voltage is:

$$Vp = \frac{V_{GB} - V_{To}}{n} \tag{B.3}$$

The gate bulk voltage is the bias voltage with signal gate bulk voltage $\left(V_{GB} = V_{GB\ BIAS} + v_{gb}\right)$

The transconductance could be written as:

$$g_m = \frac{2I_S}{nU_T}\left(\sqrt{1+i_f} - 1\right) \tag{B.4}$$

Where the forward normalized current is:

$$i_f = \frac{I_D}{I_S} \tag{B.5}$$

It is remarkable that the current is referred to the total amount o drain current, it is bias current in addition with the signal current $\left(I_D = I_{bias} + i_d\right)$

We define a new variable:

$$x = \frac{V_P - V_S}{U_T} \tag{B.6}$$

Thus, equation (B.2) becomes:

$$x = \sqrt{1+i_f} - 2 + Ln\left(\sqrt{1+i_f} - 1\right) \tag{B.7}$$

It is easy to see that:

$$\frac{\partial i_f}{\partial x} = 2\left(\sqrt{1+i_f} - 1\right) \tag{B.8}$$

Or, using equation (B.4), the previous equation becomes:

$$\frac{\partial i_f}{\partial x} = \frac{nU_T}{I_S} g_m \tag{B.9}$$

In this way, it is clear that:

$$\frac{\partial\, i_d}{\partial v_g} = I_S \frac{\partial i_f}{\partial x}\frac{\partial x}{\partial v_g} = \frac{2I_S}{nU_T}\left(\sqrt{1+if} - 1\right) = g_m \tag{B.10}$$

Then,

$$\Rightarrow \frac{\partial i_d}{\partial v_g} = g_m \tag{B.11}$$

At the moment, we have refreshed mathematical relationships and equations (B.10) and (B.11) actually are not news. Having this procedure in mind, we continue until we get the expression (B.1)

From the last equality of (B.10) we obtain:

$$\sqrt{1+i_f} = \frac{2}{nU_T\, g_m / I_D} - 1 \tag{B.12}$$

The higher derivates are:

$$\frac{\partial^2 i_f}{\partial x^2} = \frac{\partial}{\partial x}\left(2\left(\sqrt{1+i_f} - 1\right)\right) = \frac{\partial}{\partial i_f}\left(2\left(\sqrt{1+i_f} - 1\right)\right)\frac{\partial i_f}{\partial x} = \frac{1}{\sqrt{1+i_f}}\frac{\partial i_f}{\partial x} \tag{B.13}$$

And:

(B.14)

$$\frac{\partial^3 i_f}{\partial x^3} = \frac{\partial}{\partial x}\left[2\left(\sqrt{1+i_f} - 1\right)\frac{1}{\sqrt{1+i_f}}\right] = \frac{\partial}{\partial x}\left[2 - \frac{2}{\sqrt{1+i_f}}\right] = -2\frac{\partial}{\partial i_f}\left[\frac{1}{\sqrt{1+i_f}}\right]\frac{\partial i_f}{\partial x} = \frac{1}{\left(1+i_f\right)^{\frac{3}{2}}}\frac{\partial i_f}{\partial x}$$

The first three terms of a power series are:

$$i_f = i_{f0} + \frac{\partial i_f}{\partial x}\left(x - x_o\right) + \frac{1}{2}\frac{\partial^2 i_f}{\partial x^2}\left(x - x_o\right)^2 + \frac{1}{6}\frac{\partial^3 i_f}{\partial x^3}\left(x - x_o\right)^3 \tag{B.15}$$

Using (B.12), equation (B.14) is transformed to appear: (B.16)

$$i_d = I_S\left(\frac{nU_T}{I_S}g_m\right)\frac{v_g}{nU_T} + \frac{1}{2}I_S\left(\frac{nU_T g_m}{I_S}\frac{1}{\frac{2}{nU_T\, g_m/I_D}-1}\right)\frac{v_g^2}{(nU_T)^2} + \frac{I_S}{6}\left[\frac{g_m n^{U_T/I_S}}{\left(\frac{2}{nU_T\, g_m/I_D}-1\right)^3}\right]\frac{v_g^3}{(nU_T)^3}$$

It could be summarized as:

$$i_D = g_m v_g + g_m K_2 v_g^2 + g_m K_3 v_g^3 \tag{B.17}$$

Where, we finally have:

$$\begin{aligned} K_2 &= \frac{1}{2}\frac{1}{2\, g_m/I_D - nU_T} \\ K_3 &= \frac{8}{6}nU_T K_2^3 \end{aligned} \tag{B.18}$$

Appendix C

Analytic Solution of the Optima

C.1 Formalism

The purpose of the appendix is to provide a solution of the problem of finding the minimum current consumption that defines a given gain. As we remember of the chapter 3, we have:

$$A\left(I_D, \frac{g_m}{I_D}\right) = \frac{|y_{dg}|}{|y_{dd} + y_L|} \tag{C.1}$$

The graph of the gain A, is the two dimensional surface which is shown geometrically in the Fig: C.1

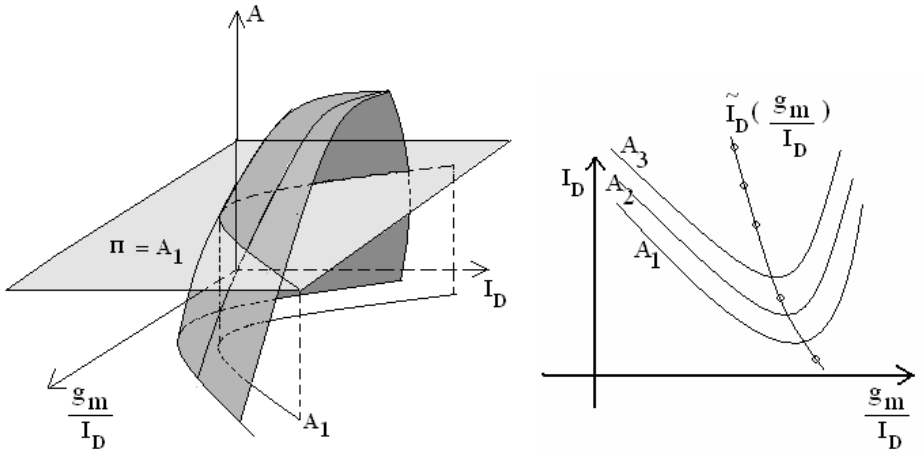

Figure C.1: The gain A is represented as two dimensional surface and maps of gain generated as contour map

A contour map of the surface $A\left(I_D, \frac{g_m}{I_D}\right)$ is the set of curves obtained by taking horizontal cross-section of the surface. Each of these curves is a family of points $\left(I_D, \frac{g_m}{I_D}\right)$ on the surface at the same height. Thus, the equation of the contour is given by: $I_D = I_D\left(A, \frac{g_m}{I_D}\right)$ in the plane $\left(\frac{g_m}{I_D}, I_D\right)$, also called design space.

For a given gain, there is a g_m/I_D value that results in an optimum of consumption. This optimum lies in moderate inversion for usual gain values. The locus of the optima represents the set of points where this value is achieved and could be determined analytically in a special case. The problem is written compactly as follow:

$\Rightarrow$ the exact problem is to find a function of the optima $\widetilde{I}_D = \widetilde{I}_D\left(\frac{g_m}{I_D}\right)$ that make $\left.\frac{\partial A}{\partial\, g_m/I_D}\right|_{\widetilde{I}_D,} = 0$

C.2 Algorithm

As we remember of the chapter 3, we have:

$$A = \frac{\left|y_{dg}\right|}{\left|y_{dd} + y_L\right|} \tag{C.2}$$

Let us take a break for a moment and we consider the problem of differentiation of a complex number $Z(x)$ which has real part $a(x)$ and imaginary part $b(x)$, i.e. $Z(x) = a(x) + j\,b(x)$
An obvious method is:

$$\frac{\partial\left|Z(x)\right|}{\partial x} = \frac{\partial\left(\sqrt{a^2 + b^2}\right)}{\partial x} = \frac{1}{2}\frac{1}{\sqrt{a^2 + b^2}}\left(2a.\frac{\partial a}{\partial x} + 2b\frac{\partial b}{\partial x}\right) = \frac{1}{\left|Z(x)\right|}\left(a\frac{\partial a}{\partial x} + b\frac{\partial b}{\partial x}\right) \tag{C.3}$$

From which we have:

$$\frac{\partial\left|Z(x)\right|}{\partial x} = \frac{1}{\left|Z(x)\right|}\left(a\frac{\partial a}{\partial x} + b\frac{\partial b}{\partial x}\right) \tag{C.4}$$

Again, returning to the original problem:

$$\frac{\partial}{\partial g_m / I_D}\left(\frac{\left|y_{dg}\right|}{\left|y_{dd} + y_L\right|}\right) = 0 \quad \Rightarrow \quad \frac{\partial\left|y_{dg}\right|}{\partial g_m / I_D}\left|y_{dd} + y_L\right| = \left|y_{dg}\right|\frac{\partial\left|y_{dd} + y_L\right|}{\partial g_m / I_D} \tag{C.5}$$

Using (C.4), in summary we have:

$$\frac{\left|y_{dg}\right|^2}{\left|y_{dd} + y_L\right|^2} = \frac{\dfrac{\partial\left|y_{dg}\right|}{\partial g_m / I_D}}{\dfrac{\partial\left|y_{dd} + y_L\right|}{\partial g_m / I_D}} \tag{C.6}$$

In many problems of practical interest we can neglect the gate resistance and we assume that our MOS is driving a load which is independent of the bias point. In others words:

- $y_L = G_L + jB_L$ is independent of bias current
- $R_g = 0$

Under these hypotheses, from (C.6) we expand two terms:
First:

$$\frac{\left|y_{dg}\right|^2}{\left|y_{dd} + y_L\right|^2} = \frac{\left(g_m - \dfrac{1}{R_F}\right)^2 + \omega_o^2 W^2 C_{ov}^2}{\left(g_d + G_L + \dfrac{1}{R_F}\right)^2 + \left(\omega WC + 2x\,\omega_o C_{jsw} + B_L\right)^2} \tag{C.7}$$

And second, by differentiating:

$$\frac{\partial |y_{dg}|}{\partial g_m / I_D} = \frac{1}{|y_{dg}|}\left(\left(g_m - \frac{1}{R_F}\right) I_D + \omega_o^2 W C_{ov}^2 . \overset{*}{W}\right) \tag{C.8}$$

$$\frac{\partial |y_{dd} + y_L|}{\partial g_m / I_D} = \frac{1}{|y_{dd} + y_L|}\left(\omega_o C_{ds} + \omega_o W C_{ov} + B_L\right)\omega_o \left[\overset{*}{C}_{ds} + \overset{*}{W} C_{ov}\right] \tag{C.9}$$

Where, for analytic simplicity we define: $\overset{*}{W} = \frac{\partial W}{\partial g_m / I_D}$ and $\overset{*}{C}_{ds} = \frac{\partial C_{ds}}{\partial g_m / I_D}$

Equation (eqC.6) can be written either as follow:

(C.10)

$$\left(\frac{g_m}{I_D} I_D^2 - \frac{I_D}{R_F} + \omega_o^2 C_{ov}^2 I_D^2 . \alpha\right)\left(G^2 + \omega_0^2 W^2 C^2 + 2\omega W . C\left(2.x\omega_o C_{jsw} + B_L\right) + \left(2.x\omega_o C_{jsw} + B_L\right)^2\right) =$$
$$\left(\left(\frac{g_m}{I_D} I_D - \frac{1}{R_F}\right)^2 + \omega_0^2 W^2 C_{ov}^2\right)\left(\omega_0^2 C^2 . W . \overset{*}{W} + \left(2.x\omega_o C_{jsw} + B_L\right)\omega_o C \overset{*}{W}\right)$$

We continue this process substituting the transistor width *W* and its derivates form which are calculated using ACM model. Some simple algebraic manipulation shows that:

$$W = I_D \frac{L}{I_{SQ}} \frac{h^2}{1-2h} \tag{C.11}$$

$$W^2 = I_D^2 \left(\frac{L}{I_{SQ}} \frac{h^2}{1-2h}\right)^2 \tag{C.12}$$

$$W \overset{*}{W} = I_D^2 \eta U_T \frac{L^2}{I_{SQ}^2} \frac{h^3(1-h)}{(1-2h)^3} \tag{C.13}$$

$$\overset{*}{W} = I_D \frac{L}{I_{SQ}} \eta U_T \frac{h(1-h)}{(1-2h)^2} \tag{C.14}$$

Where $h = \eta \frac{U_T}{2} \frac{g_m}{I_D}$ (C.15)

Again, in order to avoid complexity, one time more we rename the variables:

$$\eta U_T \frac{L^2}{I_{SQ}^2} \frac{h^3(1-h)}{(1-2h)^3} = \alpha \tag{C.16}$$

$$\frac{L}{I_{SQ}} \frac{h^2}{1-2h} = \delta \tag{C.17}$$

$$\left(\frac{L}{I_{SQ}} \frac{h^2}{1-2h} \right)^2 = \delta^2 = \beta \tag{C.18}$$

$$\frac{L}{I_{SQ}} \eta U_T \frac{h(1-h)}{(1-2h)^2} = \Delta \tag{C.19}$$

Thus, in terms of the new variables, we obtain the following new reformulation:

$$W = I_D.\delta \tag{C.20}$$

$$W^2 = I_D^2.\beta \tag{C.21}$$

$$\overset{*}{W} = I_D.\Delta \tag{C.22}$$

$$W \overset{*}{W} = I_D^2.\alpha \tag{C.23}$$

After that, precisely from (C.10) and after some algebraic manipulations we have a polynomial expression of I_D:

$$a I_D^3 + b I_D^2 + c I_D + d = 0 \tag{C.24}$$

Where its coefficients take the following expressions:

$$a = \frac{g_m}{I_D} \omega_o^2 C^2.\beta - \left(\frac{g_m}{I_D} \right)^2 \omega_o^2 C^2.\alpha \tag{C.25}$$

(C.26)

$$b = 2\frac{g_m}{I_D} \omega_o C.\delta.K - \frac{\omega_o^2 C^2 \beta}{R_F} + 2\omega_o^3 C_{ov}^2.\alpha.C.K.\delta - \left(\frac{g_m}{I_D} \right)^2 K.\omega_o.C.\Delta + 2\frac{g_m}{I_D} \frac{\omega_o^2 C^2.\alpha}{R_F} - \omega_o^3 C_{ov}^2.K.C.\beta.\Delta$$

$$c = \frac{g_m}{I_D}.\gamma - 2\omega_o \frac{C.K.\delta}{R_F} + \omega_o^2 C_{ov}^2.\alpha.\gamma - \frac{\omega_o^2 C^2.\alpha}{R_F^2} + 2\frac{g_m}{I_D} \frac{1}{R_E} K\omega_o.C.\Delta \tag{C.27}$$

$$d = -\frac{\gamma}{R_F} - \frac{K\omega_o.C.\Delta}{R_F} \tag{C.28}$$

The solution is then the root of a polynomial expression that could be evaluated through the Cardana's solution:

C.3 Cardana's Solution

$$\widetilde{I}_D\left(\frac{g_m}{I_D}\right)=\sqrt[3]{-q+\sqrt{q^2+p^3}}+\sqrt[3]{-q-\sqrt{q^2+p^3}}-\frac{b}{3a} \tag{C.29}$$

Where:

$$2q=\frac{2b^3}{27a^3}-\frac{bc}{3a^2}+\frac{d}{a} \tag{C.30}$$

And

$$3p=\frac{3ac-b^2}{3a^2} \tag{C.31}$$

In spite of the fact that an analytic expression for the optima has been found as a real root of a third order polynomial, this result makes it abundantly clear that the optima function is a very complicated function of g_m/I_D There is an analytic expression because of the hypothesis assumed make that our polynomial function of I_D would be a third order polynomial and there are a rational solution of its roots, but for canonical higher order polynomials does not exist analytic solution and it requires numerical computation.

C.4 Variations due to the load impedance

In the next section we study the dependency with the load impedance y_L and its variations:
Again, the gain is:

$$A\left(I_D,\frac{g_m}{I_D}\right)=\frac{\left|y_{dg}\right|}{\left|y_{dd}+y_L\right|} \tag{C.33}$$

Where the load impedance is: $y_L=g_L+jb_L$

Thus:
$$\Delta A=\frac{\partial A}{\partial g_L}\Delta g_L+\frac{\partial A}{\partial b_L}\Delta b_L \tag{C.34}$$

It is :

$$\frac{\partial A}{\partial g_L}=-\frac{\left|y_{dg}\right|}{\left|y_{dd}+y_L\right|^2}\frac{\partial\left|y_{dd}+y_L\right|}{\partial g_L} \tag{C.35}$$

And using equation (C.4), it is easy to see that:

$$\frac{\partial\left|y_{dd}+y_L\right|}{\partial g_L}=\frac{1}{\left|y_{dd}+y_L\right|}\mathrm{Re}\left(y_{dd}+y_L\right). \tag{C.36}$$

In the similar way:

$$\frac{\partial A}{\partial b_L} = -\frac{\left|y_{dg}\right|}{\left|y_{dd} + y_L\right|^2} \frac{\partial \left|y_{dd} + y_L\right|}{\partial b_L} \tag{C.37}$$

Again, using equation (C.4), it is easy to see that:

$$\frac{\partial \left|y_{dd} + y_L\right|}{\partial b_L} = \frac{1}{\left|y_{dd} + y_L\right|} \mathrm{Im}\left(y_{dd} + y_L\right). \tag{C.38}$$

Thus, we have:

$$\Delta A = -\frac{\left|y_{dg}\right|}{\left|y_{dd} + y_L\right|^3} \mathrm{Re}\left(y_{dd} + y_L\right) \Delta g_L - \frac{\left|y_{dg}\right|}{\left|y_{dd} + y_L\right|^3} \mathrm{Im}\left(y_{dd} + y_L\right) \Delta b_L \tag{C.39}$$

Finally:

$$\frac{\Delta A}{A} = -\left(\frac{\mathrm{Re}\left(y_{dd} + y_L\right)}{\left|y_{dd} + y_L\right|^2} \Delta g_L + \frac{\mathrm{Im}\left(y_{dd} + y_L\right)}{\left|y_{dd} + y_L\right|^2} \Delta b_L \right) \tag{C.40}$$

Appendix D

Bond Wires, Bond Pads & Guard Rings

The circuits and their connection with the outside world is a very important issue to take into account. The IO ports in our circuit are connected to bond pads, which in turn are connected to bond wires. This bond wires are the interface from the circuits to the outside world connecting the bond pad with the package pin, which is connected to the PCB.

D.1 Bond Pads

Bond pads and their ESD protection circuits will heavily influence the RF performance. Electrostatic Discharge Structure (ESD) is normally included at the periphery of circuits connected to the input-output pads in order to prevent circuit damage by external electrostatic pulses. This ESD device basically has the same architecture and behavior that a DIODE has, but it must be treated in the context as a capacitor capable to absorb the RF power creating power losses. We can see in the next figure D.1, the schematic of a PAD with its ESD protection.

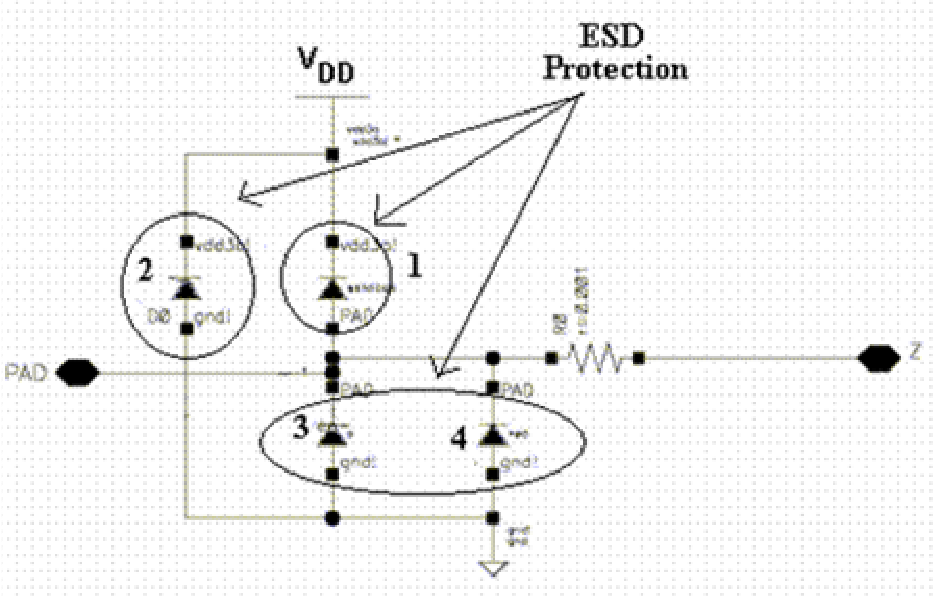

Figure D.1: Schematic overview of a PAD and its ESD protection (DIODES). The port Z represents the connection to the integrated circuit and the PAD is connected to wire bond.

On the other hand, in same cases such as power amplifier class A and B, the output voltage swing in the output MOS transistor must not be limited in order not to degrade the signal and to deliver the totality of the power desired. If we connect a ESD structure in the drain of the output MOS transistor, the diode of the ESD structure will switch on when the voltage raise up and overcomes the value of the DC power source.

Consequently, we will see a signal wave deformed and higher current consumption throughout the diode, which still on, appears making a serious damage in our circuit.

For this reasons a special bond pad was made without ESD protection for our device In the figure D.2, we can see one of the pads without ESD protection that was specifically made for using as output of the power amplifier.

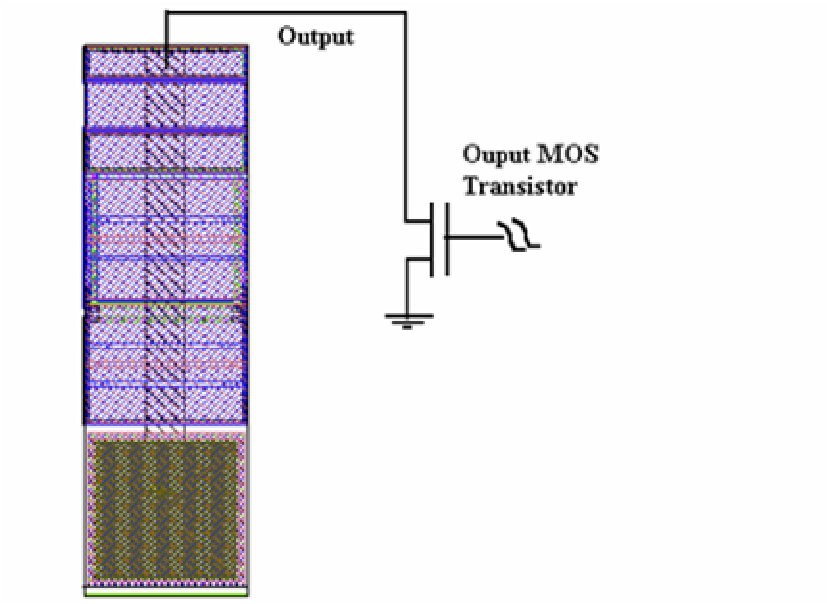

Figure D.2: Layout overview of the PAD without ESD protection.

Although we need to use pads without protection, caused by the problem discussed previously when the output voltage must exceed the voltage V_{DD} connected to the ESD protection, turning on the diode, normally the pads without protection could be avoided if the maximum voltage swing keeps below V_{DD} and if a correct resonance network is used close to the pad. That is the case of the input of our power amplifier.

To demonstrate it, we show in the next figure a schematic that depicts how by using a simple inductance L, connected parallel to the PAD, it would produce a resonance in the circuit.

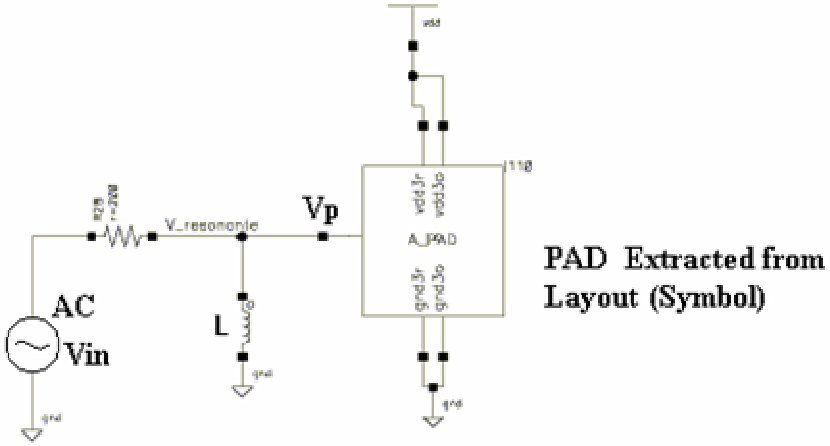

Figure D.3: PAD with resonant inductance

It is clearly visible in the figure D.4 where we have study the AC response that connecting different values on inductances, there is a value of inductance L that does not produce attenuation at our desired frequency of 915MHz.

From this figure, it follows that moving the value of L from the value L_1 to Lr, we will found one of them that the ESD structure would became resonant. This process is depicted in the next figure.

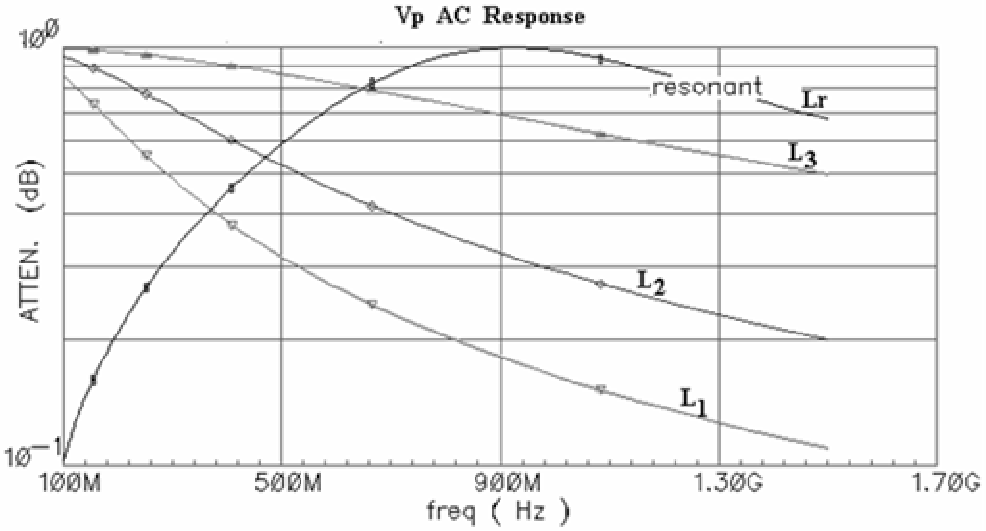

Figure D.4: Lr is the value (Lr=6.37nHy) which could be used to "kill " the attenuation produced by the ESD protection built into the pad , at a proper frequency (in our case 915 MHz). As we do not know exactly the value of pad's capacitance, this value was achieved manually through simulation study.

Because there is not ideal inductor which value is 6.37nH, we must use standard components. If we use a standard inductor value of 6.8nH with dispersion of 5 %, through simulation we can see that in a worst case if the inductor changes from 6.37nH to 7.14nH, the resonance frequency is moved from 914.6 MHz to 861MHz.

The variation of the frequency could be also expressed analytically as follow if the pad's capacitance value is fixed:

$$\Delta f = f_o - f = f_o\left(1 - \sqrt{\frac{L_o}{L}}\right) \tag{D.1}$$

Where:

f_o : is the resonant frequency when L_o is used

f : is the resonant frequency when L is used

In our case: $\Delta f = 914.6MHz.\left(1 - \sqrt{\frac{7.14nH}{6.37nH}}\right) = -53.7MHz$

Through simulation study and estimation calculus, it is possible to conclude that the variation of L respect to the ideal value will be a problem. Also, the pad's capacitance value is a problem due to we know its value only by simulation study, and it is an estimation which actually we are not sure how many dispersion has.
In a L-C resonant network, the variation of the frequency caused by capacitance's value variations could be expressed analytically as follow if the L value is fixed:

$$\Delta f = f_o - f = f_o\left(1 - \sqrt{\frac{C_o}{C}}\right) \tag{D.2}$$

Where:

f_o : is the resonant frequency when C_o is used

f : is the resonant frequency when C is used

If we have estimated a capacitance's value of 4.8pF through simulation study, a hypothetical dispersion of 5% on this value will make that the resonant frequency will move Δf :

$$\Delta f = 914.6MHz.\left(1 - \sqrt{\frac{4.8pF}{4.56pF}}\right) = -23.8MHz \quad \text{(D.3)}$$

D.2 Bond wires

The ideal package should create a transparent link between the printed circuit board and the internal chip. Any deviation from the ideal package causes signal degradation.
For RF applications, the bond wire cannot be treated as a simple wire. The bond wire must be considered as an inductor in series with a resistor and a parasitic capacitor connected to backplane ground, which values are determined by the package used.
Particularly, the capacitance is created between the solder pad and the backplane ground and it is dependent on the dielectric constant, solder PAD area and thickness of the PCB.

We have to make specials matching networks so that absorb the inductance and capacitance of the wire bond at the input-output port as part of the matching impedance network.

D.3 Guard Ring

Guard rings around a circuit provide a low resistance path to AC ground for the noise and help to minimize the amount of noise that usually couples from place to place at higher frequencies
In our circuits, guard rings have been built to provide effective isolation by taking care to ensure that the guard rings are connected to a quiet supply.

Special attention was taken, not only to provide isolation for each block that conform our integrated circuit, but also, because the output MOS transistor was designed to directly attack an unprotected output pad. Thus, protective double guards preventing latchup were added to all transistors. We can see an example in the following figure D.5

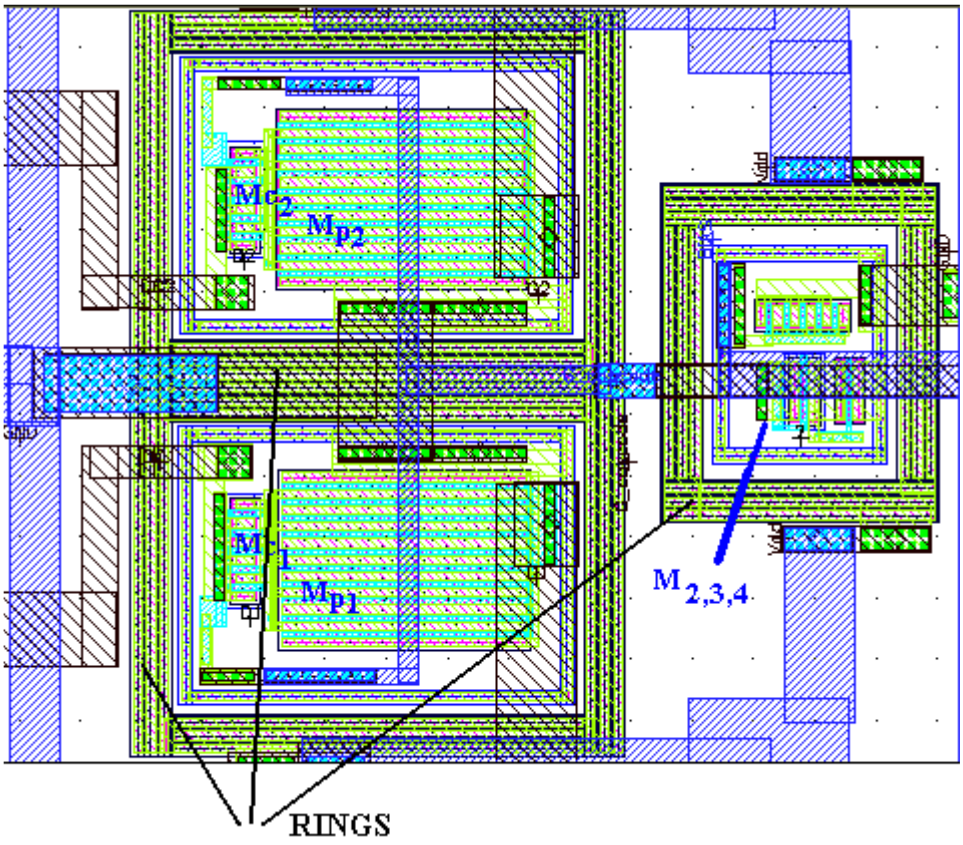

Figure D.5: Examples how the guard ring is implemented in the output MOS transistor of the power amplifier.

Appendix E

Non Quasi-static Frequency Boundary

E.1- Relationships between f_{NQS} and f_T

As we have discussed in the chapter 3, in the literature [1][2], the quasi static assumption used for deriving the small signal circuit does not hold anymore when the frequency gets close to the intrinsic cut-off frequency of the device. The onset frequency of NQS effect is found to be comparable to f_T and the QS model can do a good job when the operation frequency is sufficiently below f_T [2],
Next, we will develop a more exactly onset frequency of NQS effect based on the ACM model.

It is well known that NQS models have been proposed in the literature[1][3], which taking into account different effects requires to replace the parameter g_m with first order transconductance that depends on the frequency as follow :

$$y_m = \frac{g_m}{1 + j\omega\tau_1 + ...} \tag{E.1}$$

It has also been presented in equation (3.32)

Where the time constant τ_1 [3] depends on the forward normalized current as follow:

$$\tau_1 = \frac{L^2}{\mu U_T}\frac{1}{5}\frac{1}{\sqrt{1+i_f}} \tag{E.2}$$

Then, QS model will predict accurate dynamic operation at frequencies up to the f_{NQS} , where it could be assumed as follow:

$$\omega\tau_1 << 1 \quad \Rightarrow 2\pi f_{NQS}\tau_1 = 0.1 << 1 \tag{E.3}$$

More succinctly:

$$f_{NQS} = \frac{1}{20\pi}\frac{1}{\tau_1} \tag{E.4}$$

Using (E.2) into (E.4), we have:

$$f_{NQS} = \frac{1}{20\pi}\frac{1}{\tau_1} = \frac{1}{20\pi}\frac{5\mu U_T}{L^2}\sqrt{1+i_f} = \frac{1}{4\pi}\frac{\mu U_T}{L^2}\sqrt{1+i_f} \tag{E.5}$$

From [3], the cut off frequency can be roughly approximated to:

$$f_T \approx \frac{1}{\pi}\frac{\mu U_T}{L^2}\left(\sqrt{1+i_f}-1\right) \tag{E.6}$$

Coming back to equation (E.5), and using (E.6), it is easy to see that:

$$f_{NQS} = \frac{1}{4\pi}\frac{\mu U_T}{L^2}\left(\sqrt{1+i_f}-1+1\right) \approx \frac{1}{4\pi}\frac{\mu U_T}{L^2}\left(\frac{\pi L^2}{\mu U_T} f_T + 1\right) \tag{E.7}$$

More succinctly:

$$f_{NQS} \approx \frac{1}{4}\left(f_T + \frac{\mu U_T}{\pi L^2}\right) \tag{E.8}$$

It is an approximation less conservative that $f_{NQS} \approx \frac{1}{10} f_T$, which is often used in the literature. While we were developing the tool shown, we did not know (E.8) and this must be improved in our tool in the future.
For instance, if we use the values given in table 4.1 where the effective mobility is μn =370cm^2/Vs and considering L =0.35μm and U_T =26mV, then:

$$\frac{\mu U_T}{\pi L^2} = \frac{370\left(0.01m\right)^2/Vs.0.026V}{\pi 0.35^2\left(1e^{-6}\right)^2 m^2} = 2.5GHz \tag{E.9}$$

E.2 Effect of the slope factor n

In the next section we present an example in order to show the effect of the spread of the slope factor n.
Considering the basic amplifier shows in figure E.1, the tool creates a set of gain map and non quasi static boundary as we can see in the figure E.2, with different values of n ,and where:

-Slope factor n: varies from n =1 to 1.6 with step fixed of 0.05

-Non quasi static boundary is considered as $f_{NQS} \approx \frac{1}{10} f_T$

-The gain map is generated for voltage gain of A=4 V/V

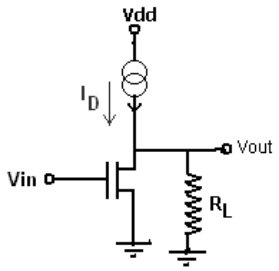

Figure E.1: Basic amplifier: For our example we took V_{dd}=3V and R_L=6500Ω

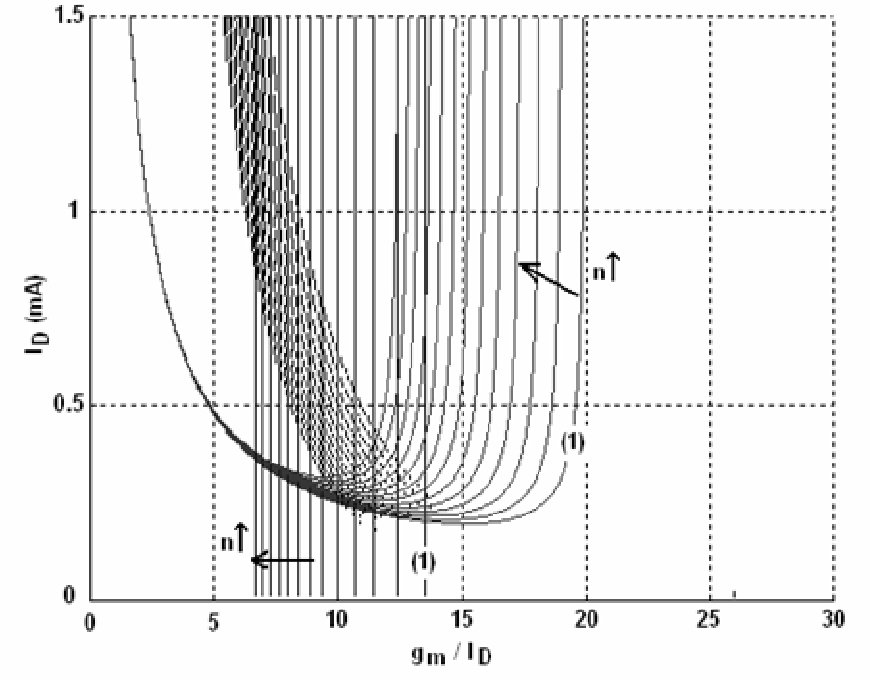

Figure E.2: Effect of the variations of the slope factor n
The mark **(1)** correspond with the lowest value of n

It is interesting to see how the non quasi static boundary is moved to strong inversion.