Biopotential integrated preamplifier

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***Abstract*—This work presents a novel amplifier architecture which is the input stage of an analog front end targeting the acquisition of biological signals with low voltage supply, low noise, and low power consumption. A prototype was designed and fabricated in a 130 nm CMOS technology, and characterized by simulations and preliminary measurements. It presents an input noise of 1.41 μV_{rms}, a current consumption of 30 μA, and operates from a 1.2 V voltage supply. The bandwidth ranges from 20 Hz to 10 kHz, the gain is 40 dB and the NEF is 2.97.**

I. Introduction

In recent decades, the increasing demand for medical equipment capable of health monitoring, diagnosis aid, patient recovery and follow-up, has led to the development of a significant number of portable and implantable medical devices. In particular, technological evolution has allowed the miniaturization of electrocardiogram (ECG), electromyogram (EMG), and electroencephalogram (EEG) recording devices. These devices must have a small size and low power consumption. In this regard, CMOS technology has played a fundamental role in the miniaturization process over time because it has been increasing the functionalities and processing capacity, reducing both size and power consumption. Clear examples of these advances, among others, are the Insertable Cardiac Monitor [1], EEG recording devices that non-invasively record and process neural signals for the most diverse purposes: medical, prosthetics [2], research [3], and even entertainment [4].

The preamplifier is the input stage of the biopotential recording device. It must amplify signals in the range of interest for the application, and filter unwanted signals while maintaining the highest possible signal to noise ratio. Besides, the dc signals caused by the contact potential between the electrodes and the skin must be filtered. In [5], a neural preamplifier featuring low input noise, high Common Mode Rejection Ratio (CMRR), and current-efficiency (low Noise Efficiency Factor, NEF [6]) was presented. The amplifier improves the performance with respect to capacitive feedback neural amplifiers (i.e., [7]) by taking advantage of the high CMRR achievable in a standard DDA (Differential Difference Amplifier) structure without jeopardizing power consumption. In addition, this preamplifier introduced a novel technique for blocking the input dc voltage. However, this architecture was implemented in a 0.5 μm CMOS technology and therefore required a power supply of 3.3 V, and some aspects of the previously mentioned technique were never studied in depth.

The main goal of our work is to design, fabricate, and test a preamplifier for biological signals, based on the architecture proposed in [5] but implemented in a 130 nm CMOS technology. For this, some changes are introduced in the original architecture to lower the supply voltage from 3.3 V to 1.2 V. In addition, a deep analysis of the effect on the gain and high-pass frequency of the technique for blocking the input dc voltage is presented. The targeted preamplifier has the following specifications:

- Voltage supply: $V_{DD} \leq$ 1.2 V
- Gain: G = 40 dB
- High-pass frequency: $f_{high-pass}$ = 20 Hz
- Low-pass frequency: $f_{low-pass}$ = 10 kHz
- Input noise $\leq$ 2.5 μV_{rms}
- Input linear range = 2 mV_{pp} with a THD (Total Harmonic Distorsion) $\leq$ 5%
- CMRR $\geq$ 75 dB

II. Architecture

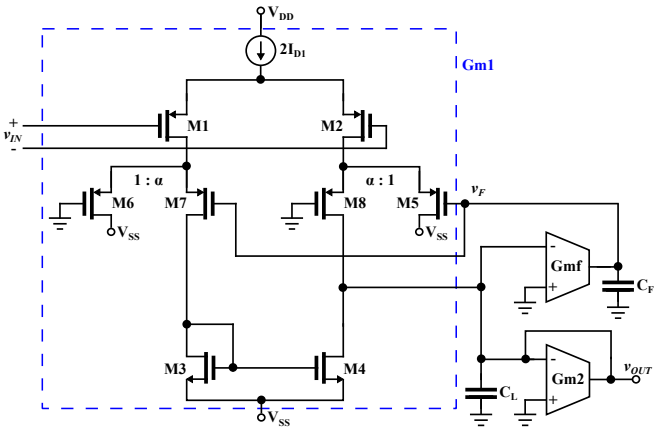

Fig. 1: Preamplifer architecture.

In this work, we propose a variant of the architecture in [5] aiming at decreasing the supply voltage (from 3.3 V to 1.2 V). The main novelty of our proposal consist of to replace the NMOS asymmetric differential pair of [5] for a PMOS one, and place it on the other branch of Gm1 (M6 and M7 in Fig. 1). In this way, it is possible to reduce the supply voltage, because Gm1 has fewer transistors stacked in the output branch. It also offers a symmetric structure, which ensures that the transistors of the asymmetric pairs have the same nominal transconductance.

Gm1 core is formed by M1, M2, M3 and M4 and its transconductance is $Gm1$. The M5-M8 block jointly with Gmf and C_F, implement an output feedback loop that establishes

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the high-pass characteristic and blocks the dc input. Gm2 and Gmf are symmetric OTAs (Operational Transconductance Amplifiers) whose respective transconductances are G_{m2} and G_{mf} (see Fig. 1). The source degeneration using MOS transistors linearisation technique proposed in [8] was used to improve the Gm2 input linear range.

The M5-M8 block, jointly with Gmf and C_F, are dedicated to establish the high-pass characteristic and to block the dc input (we refer to the interested reader to [5] for further details on the functioning of this part of the circuit). In small-signal operation M6-M7 and M5-M8 can be interpreted as asymmetric differential pairs where α defines the degree of asymmetry. $g_{m7} = \alpha g_{m6}$ and $g_{m8} = \alpha g_{m5}$, where g_{m5}, g_{m6}, g_{m7} and g_{m8} are the transconductance of M5, M6, M7 and M8 respectively. The effect of these transistors in the value of G_{m1} can be observed in Eq. 1.

$$G_{m1} = g_{m1}\frac{\alpha}{1+\alpha} \tag{1}$$

where g_{m1} is the transconductance of the input transistors of Gm1 (M1 and M2).

α is a key parameter that rules the trade-off between the capacity of blocking input dc voltage $V_{IN,dc}$, the high-pass frequency $f_{high-pass}$ accuracy, and the gain value G. An in-depth analysis of the influence of α on these characteristics of the preamplifier is presented in the following subsections.

A. Asymmetric differential pair

M7 and M8 are implemented as α transistors identical to M6 and M5 respectively, connected in parallel as shown in Fig. 2. We will refer to the transconductance of the asymmetric differential pair as G_{mADP}.

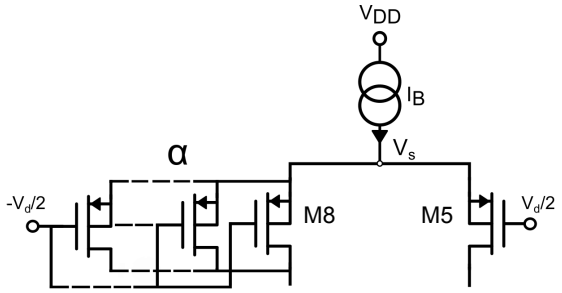

Fig. 2: Asymmetric differential pair.

The output conductance of the asymmetric differential pair (the conductance view from the drain of M8) is given by Eq. 2.

$$G_{out_{ADP}} = g_{DS_8}\frac{1}{1+\alpha} \tag{2}$$

where g_{DS_8} is the small-signal output conductance of M8. Therefore, the output conductance of Gm1 G_{out_1} will be given by Eq. 3.

$$G_{out_1} = g_{DS_5} + g_{DS_8}\frac{1}{1+\alpha} \tag{3}$$

where g_{DS_5} is the small-signal output conductance of M5. The dependence of the output conductance of Gm1 with α is noted.

B. Transfer function

The circuit depicted in Fig. 1 has the transfer function presented in Eq. 4.

$$\frac{V_{out}}{V_{in}}(s) = \frac{\frac{G_{m1}}{C_L}}{s^2 + \frac{G_{out}}{C_L}s + \frac{G_{mADP}G_{mf}}{C_L C_f}} \tag{4}$$

where $G_{out} = G_{out1} + G_{m2}$. The bandpass gain G is given by Eq. 5, the high-pass frequency $f_{high-pass}$ by Eq. 6, and the low-pass frequency $f_{low-pass}$ is given by Eq. 7.

$$G = \frac{G_{m1}}{G_{out}} \tag{5}$$

$$f_{high-pass} = \frac{G_{mADP}G_{mf}}{2\pi G_{out}C_F} \tag{6}$$

$$f_{low-pass} = \frac{G_{out}}{2\pi C_L} \tag{7}$$

where $G_{mADP} = \frac{1}{2}G_{mADP_{85}} + \frac{1}{2}G_{mADP_{67}}$, and $G_{mADP_{85}}$ is the transconductance of the asymmetric differential pair M5-M8, and $G_{mADP_{67}}$ is the transconductance of the asymmetric differential pair M6-M7.

C. Variations in $Gm1$ due to the input dc voltage blocking technique

The results presented in this subsection are numerically calculated using the ACM [9] model with M5, M6, M7, and M8 biased in weak inversion. In this condition, transistors have low V_{DSsat}, which is necessary to meet the requirements of a low voltage supply.

The input dc blocking capacity will be evaluated according to the variation of the DC current ΔI_{DC} that is generated in M1 and M2 by an input dc voltage V_{inDC}.

$$\Delta I_{DC} = \frac{I_1 - I_2}{2I_{D1}} \tag{8}$$

where I_{D1} is the bias current of Gm1. The graphs are normalized with respect to their steady state: $G_0 = G_{@\Delta I_{DC}=0}$, and $f_{high-pass0} = f_{high-pass@\Delta I_{DC}=0}$.

According to Eq. 1 there is a gain attenuation due to the asymmetric differential pairs. Fig. 3 shows how the asymmetric differential pairs modify the gain, as a function of α and ΔI_{DC}.

In the transient of the input dc voltage blocking, the operation point of the asymmetric differential pairs will be changing until $I_{D7} = I_{D8}$. This will result in a variation of the transconductance of the asymmetric differential pairs G_{mADP} (which is a function of α). In addition, Eq. 6 shows that the preamplifier high-pass frequency depends on G_{mADP}. Fig. 4 shows the variation of $f_{high-pass}$ considering different values of α and ΔI_{DC}.

For α = 1, the differential pair M5-M8 (and M6-M7) will be symmetrical, according to Eq. 1 half of the gain will be lost,

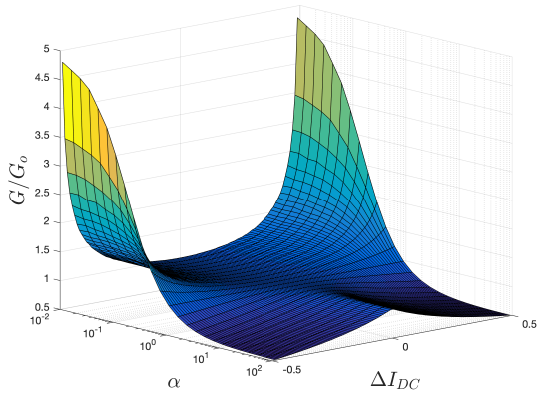

Fig. 3: Variation of gain G as a function of α and ΔI_{DC}

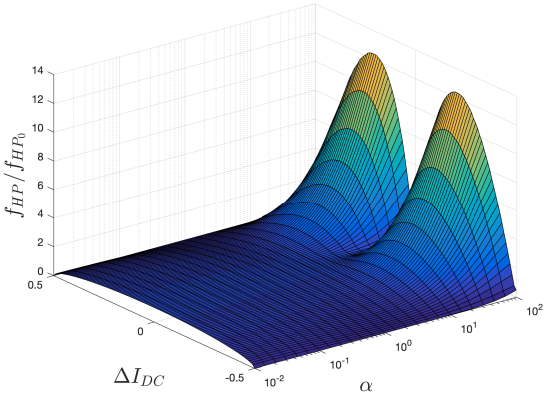

Fig. 4: Variation of $f_{HP} = f_{high-pass}$ as a function of α and ΔI_{DC}

and the circuit will be able to block higher levels of dc input signals (see Fig. 3). On the other hand, if α = 100 or greater is adopted, the loss of gain will be negligible, but the capacity of blocking high levels of dc input signals will be reduced. In addition, large values of α will introduce a significant variation on the high-pass frequency (see Fig. 4).

III. Implementation

According to the discussion made in the previous section, α = 4 is chosen. Gm1 is the main contributor of noise. Therefore, to reduce thermal noise, the input differential pair of Gm1 (M1 and M2) was biased in weak inversion, and the current mirror (M3 and M4) in strong inversion [5]. The effect of Flicker noise was reduced by adjusting the size of M1 and M2 (increasing the width W and the length L while keeping the W/L ratio constant, to keep the same inversion level). Once G_{m1} and G_{mADP} were set, using the specifications presented in Section I, and equations from Section II-B, the preamplifier main parameters were determined (see Table I).

Cascode transistors were added in Gm1, Gm2, and Gmf, to increase their output resistance and improve the overall performance of the circuit.

C_L = 48 pF and C_F = 100 pF were built as poly-poly capacitors. The connection of external capacitors was foreseen to provide the possibility of configuring the preamplifier bandwidth.

TABLE I: Preamplifier main parameters.

Parameter	Value
G_{m1}	270 μS
G_{mADP}	100 μS
G_{m2}	1.8 μS
G_{mf}	300 pS
C_F	100 pF
C_L	48 pF

A preamplifier was implemented in a 130 nm standard CMOS process, Fig. 5 shows the layout of the fabricated chip. The complete preamplifier occupies an area of 0.2 mm^2.

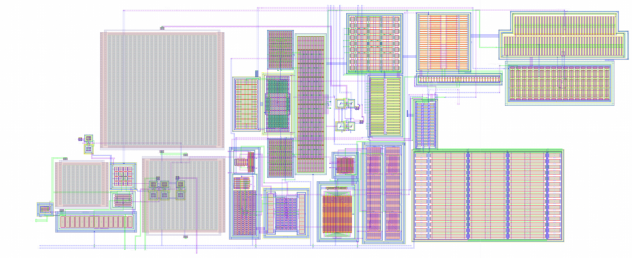

Fig. 5: Preamplifier layout.

IV. Results

Table II presents results of Monte Carlo (MC) post-layout simulations (500 runs) using PSP model. PSRR+ is the positive power supply rejection ratio (V_{DD}) and PSRR- refers to the negative power supply rejection ratio (V_{SS}).

TABLE II: Simulation results.

	Specs	Result	Obs.
Gain (dB)	40	40.2	σ=0.2
$f_{high-pass}$ (Hz)	20	19.5	σ=0.8
$f_{low-pass}$ (kHz)	10	10.0	σ=0.4
Voltage supply (V)	$\leq$1.2	1.2	-
Supply current (μA)	-	29.7	-
Input noise (μV_{rms})	2.5	2.45	σ=0.2
NEF	5	5.1	-
CMRR @ 1 kHz (dB)	$\geq$80	75	worst-value
Gain w/$V_{IN,dc}$ = 50 mV (dB)	-	35.5	-
Gain w/$V_{IN,dc}$ = 100 mV (dB)	-	27.5	-
THD w/V_{in} = 2 mV_{pp}	$\leq$5%	2.3%	-
PSRR+ (dB)	-	79	worst-value
PSRR- (dB)	-	53	worst-value

Preliminary noise laboratory characterization on six samples was performed. The noise power spectral density S_{Vin} was measured using an Agilent 4395A Spectrum Analyzer. Fig. 6 presents the noise results for one sample. Integration under the solid curve yields to an input-referred noise voltage of 1.41 μV_{rms} where the integration bandwidth was [10 Hz-100 kHz].

Table III shows a comparison with the state of the art. Our preamplifier presents one of the lowest noise levels reported up-to-date (over the considered bandwidth) while presenting a very competitive performance in other important features, like CMRR or NEF. On the other hand, the overall preamplifier linearity input range, which is limited by the input differential pair linearity range (M1 and M2), is low but adequate to deal with the targeted input signals (amplitudes of hundreds of micro-volts).

TABLE III: Comparison with prior work.

	[7]	[10]	[11]	[12]	[13]	[14]	[5]	[15]	This Work
Technology (μm)	1.5	0.13	0.065	0.35	0.18	0.5	0.18	0.5	0.13
Gain (dB)	39.5	47.5	52.1	46.0	70	49.2	40.4	47	40
$f_{low-pass}$ (kHz)	7.2	6.9	8.2	10.0	1.0	10.3	5	7.5	10.0
$f_{high-pass}$ (Hz)	25m	167	1.0	200	0.5	0.1	200	1.0	19.5
Supply current (μA)	16.0	1.6	3.3	22.4	2.2	8.5	0.8	16.1	29.7
Input noise (μV_{rms})	2.2	3.8	4.1	2.9	1.2	1.9	4.1	1.8	1.4
Noise integration bandwidth (Hz)	0.5-50k	1-100k	1-8.2k	N/A	0.5-1k	0.03-25k	200-5k	N/A	10-100k
NEF	4.0	2.3	3.2	6.6	2.4	2.1	2.0	3.2	3.0
$CMRR_{measured}$ (dB)	83	83	80	110	110	88	68	100.5	N/A
$CMRR_{worst-case}$ (dB)	42	N/A	46	N/A	N/A	84	N/A	N/A	75
V_{DD} (V)	5.0	1.2	1.0	3.3	1.0	3.3	1.0	3.3	1.2
THD (% @ V_{in})	1% @ 17 mV_{pp}	1% @ 3 mV_{pp}	1% @ 1.4 mV_{pp}	0.1% @ 20 mV_{pp}	N/A	1% @ 2 mV_{pp}	1% @ 0.7 mV_{pp}	N/A	2.3% @ 2 mV_{pp}

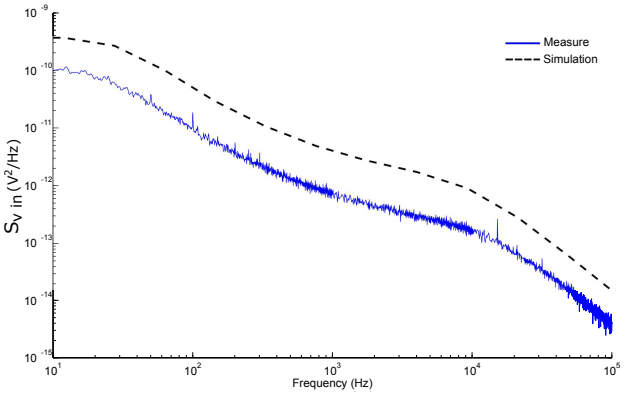

Fig. 6: Input-referred noise power spectral density

V. Conclusions

A low voltage biopotential preamplifier, suitable for use in implantable or wearable devices, was designed and fabricated on a 130 nm CMOS technology.

Results from simulations and preliminary measurements show its remarkable low input-referred noise, low supply voltage (1.2 V), low current consumption, and state-of-the-art NEF (2.97). These results favorably compare with prior work.

Preliminary results show that the input-referred noise ia 1.4 μV_{rms}, the current consumption is 30 μ, the gain is 40 dB, $f_{high-pass}$ = 20 Hz and $f_{low-pass}$ = 10 kHz.

The PSP model was very precise in terms of predicting preamplifier behavior. However, the simulation showed significant differences in the total noise of the system with respect to what was measured.

Future work includes a complete characterizations of the fabricated chips, including the experimental analysis of the variations in $Gm1$ due to the input dc voltage blocking technique, and in-vivo validation of the architecture.

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