Variability-aware Design Method for a Constant Inversion Level Bias Current Generator

G. Antúnez-Calistro, M. Siniscalchi, F. Silveira and C. Rossi-Aicardi

***Abstract*—A model for estimating the dispersion in the output of a MOS-only, constant inversion level, current reference is presented. Based on such model, a design method is introduced that allows to optimize how area is spent in order to minimize dispersion for a given layout complexity. The model was successfully compared to measurements of a current source fabricated on a 130 nm CMOS technology and to simulations of six other designs. The fabricated, ultra low power, current source has an area of 0.032 mm2 and produces 11.4 nA on average while all 8 measured devices were inside +/-2.1 % of the average.**

***Index Terms*—Current References, MOS transistors, mismatch, ACM, temperature effects, constant inversion.**

I. Introduction

Current sources are used in every kind of analog circuit for biasing purposes. Although constant or PTAT current sources are mostly used, some circuits benefit from current references working at a constant inversion level as shown in several recent publications [1]–[8]. A MOS-only simple circuit [9]–[11] generates a constant inversion level current. The constant inversion property implies that the generated bias current varies with temperature, so compensating the mobility related temperature dependency of the biased circuit.

Although insights on the design of these current source circuits have been previously published [11]–[13], the dispersion of the bias current due to mismatch among the involved transistors has received so far little consideration. In fact, the reported dispersion of the bias current reaches $\pm 10\,\%$ [12] and even as much as $\pm 30\,\%$ [10]. Moreover, in the past, the authors have observed both excellent and very poor dispersion among circuits they designed. This is expected to happen since the dispersion of the bias current is sometimes just reported as another item in a full characterization, rather than minimized or at least estimated during the design stage. Also, this parameter is not even reported for other state-of-the-art constant inversion level bias current sources [14], [15].

In order to address this issue, the authors have proposed a dispersion model well suited for these circuits and showed simulation results that validate it [16]. In the present work, we review the aforementioned model and the associated design method while validating them through Monte Carlo and DCmatch simulations.

We also present a constant inversion level current source design example which was fabricated in CMOS 130 nm, and used to validate the model through measurements. The dispersion of the obtained bias current is almost 5 times smaller than those of [10], [12].

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Section II reviews known results about the constant inversion level current generator. Section III introduces a mismatch based variability model for the current while Section IV presents a design method based on that model. Section V validates the design method by comparing some designs with simulation results, while Section VI reports measurement results for one of those designs, where average and chip to chip dispersion results are presented. Section VII presents a comparison against state-of-the-art. Finally, we draw some conclusions in Section VIII.

II. Circuit Analysis

This section follows [11] in describing the constant inversion level bias current generator while defining notation. The circuit analysis is based on the "Advanced Compact Model" (ACM) [17], [18] for the long channel MOSFET, accurate through all inversion levels.

ACM [17] expresses the drain current of a MOSFET as the difference between forward and reverse currents:

$$I_D = S\, I_{SQ}\, (i_f - i_r)\,, \quad S = W/L\,, \tag{1}$$

where $\mathrm{i_f}$ and $\mathrm{i_r}$ are the forward and reverse inversion coefficients and W, L are the effective width and length of the MOS transistor. The sheet normalization current is defined as

$$I_{SQ} \;=\; \frac{1}{2}\, n\, \mu C'_{ox}\, {U_T}^2 \tag{2}$$

where n is the subthreshold slope factor, μ is the mobility of carriers in the MOS channel, $\mathrm{C'_{ox}}$ is the gate capacitance per unit area and the thermal voltage will be denoted as

$$U_T = \frac{kT}{q}\,, \tag{3}$$

where T is the absolute temperature, k is Boltzmann's constant and q is the electron charge.

The relationship between the terminal voltages $\mathrm{V_G}$, $\mathrm{V_S}$, $\mathrm{V_D}$ (all referred to the bulk) and the inversion coefficients is

$$\frac{V_P \;-\; V_{S(D)}}{U_T} \;=\; \mathcal{F}\left(i_{f(r)}\right) \;\equiv\; \sqrt{1+i_{f(r)}} \;-\; 2 \;+\; \ln\left(\sqrt{1+i_{f(r)}}-1\right). \tag{4}$$

The pinchoff voltage $\mathrm{V_P}$ depends on $\mathrm{V_G}$ through a rather complex expression [17], but is very well approximated by

$$V_P = \frac{(V_G - V_T)}{n} \tag{5}$$

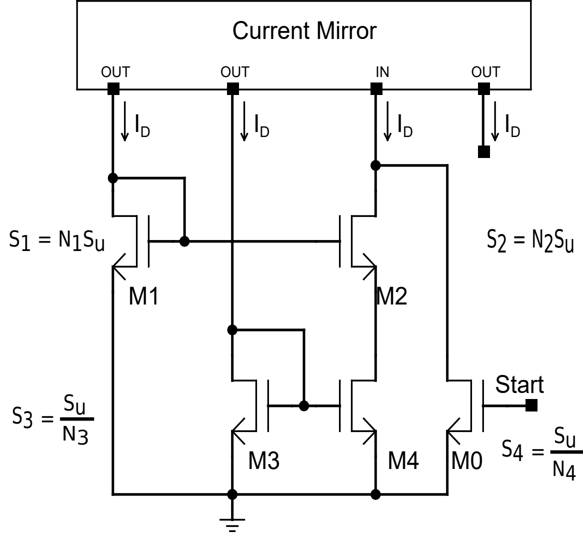


Fig. 1. MOS-only constant inversion level bias generator

where $\mathrm{V_T}$ is the threshold voltage. When terminal voltages $V_{DS} > V_{DSSAT}$ the transistors are in saturation and the current follows:

$$I_D = S\, I_{SQ}\, i_f\,. \tag{6}$$

The circuit in Fig. 1 is a constant inversion level bias current generator. It was first proposed in [9], [10] and later extended in [12]. It was fully modelled in [11] where it is shown that it produces a particular temperature dependence on the bias current which yields a constant inversion coefficient (i_f), independent of temperature. Moreover, it depends only on ratios of the aspect ratios S_1 to S_4 of MOSFETs M_1 to M_4 (Fig. 1), as well as on the copy ratios of the mirrors. For simplicity and lowest consumption, these are considered to be 1:1 mirrors. It must be noted that M_1 to M_3 are saturated, while M_4 is not. From (6), the generated bias current depends on I_{SQ} , S and i_f of any of the saturated MOSFETs, e.g.:

$$I = I_{sq} i_{f2} S_2. \tag{7}$$

Among the many possible sets of ratios involving S_1 to S_4, the following have been chosen for circuit analysis:

$$B = \frac{S_2}{S_1},\; M = \frac{S_2}{S_3},\; D = \frac{S_4}{S_4 - S_3}\;. \tag{8}$$

As already noted [11], choosing B, D and M determines the inversion levels of M_1 to M_4: i_{f1}, i_{f2}, $i_{f3} = i_{f4}$, i_{r4}. Their value must be computed numerically as shown in [11], by solving $\mathcal{F}(i_{f1}) - \mathcal{F}(i_{f2}) = \mathcal{F}(i_{f4}) - \mathcal{F}(i_{r4})$.

Usually, for ultra low power applications, $S_1 > 1$, $S_2 > 1$, $S_3 < 1$ and $S_4 < 1$. Also, in order to minimize mismatch effects the transistors are designed as parallel (M_1,M_2) or series (M_3,M_4) associations of a unit MOSFET M_u with aspect ratio $S_u = W_u/L_u$. Thus, we define N_1, N_2, N_3, N_4 such that $S_1 = N_1 Su$, $S_2 = N_2 S_u$, $S_3 = S_u/N_3$, $S_4 = S_u/N_4$. Therefore, N_2, N_3, N_4 are obtained from N_1, B, D, M as:

$$N_2 = N_1 B,\; N_3 = \frac{M}{N_2},\; N_4 = N_3 \frac{D-1}{D}\;. \tag{9}$$

III. Modelling the Variability of the bias generator

Mismatch in both the multiple output current mirror and among the active transistors M_1 to M_4 affect the temperature independent inversion coefficients (i_{fj}). The absolute dispersion in the threshold voltage V_T and the relative dispersion in $S\, I_{SQ}$, which is that of $\beta = S\mu C'_{ox}$, were modelled following [19]. In the latter, we include the effect of channel width variation through A_{CWV} [20]. For each M_j, $j = 1, 2, 3, 4$:

$$\sigma^2_{V_{Tj}} = \frac{A^2_{VT}}{2W_u L_u}\frac{1}{N_j};\quad \frac{\sigma^2_{\beta_j}}{\beta^2_j} = \frac{A^2_{\beta}}{2W_u L_u}\frac{1}{N_j} + \frac{A^2_{CWV}}{2W^2_u L_u}\frac{1}{N_j}\,, \tag{10}$$

where A_{VT} $[V\mu m]$, A_β $[\mu m]$ and A_{CWV} $[\mu m^{3/2}]$ are technology parameters and the dispersions are those of each transistor against a mean transistor [21].

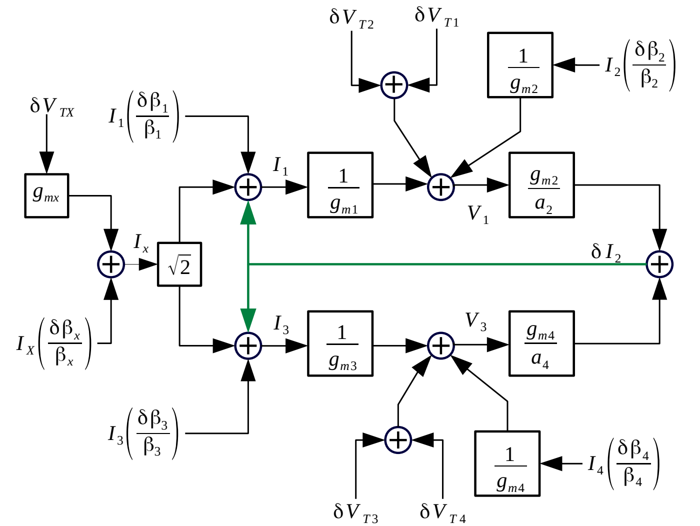


Fig. 2. Closed loop diagram for the constant inversion level bias current generator, showing dispersion in I_2 as a function of small signal and mismatch parameters. Notation is defined in Appendix A.

Fig. 2 shows how each transistor contributes to the dispersion in I_2, the branch current through M_2 and M_4, by considering dispersion as a small DC signal [22]. Due to the self biased topology, the signal diagram in Fig. 2 has the shape of a closed loop. Further details on Fig. 2 can be found in Appendix A.

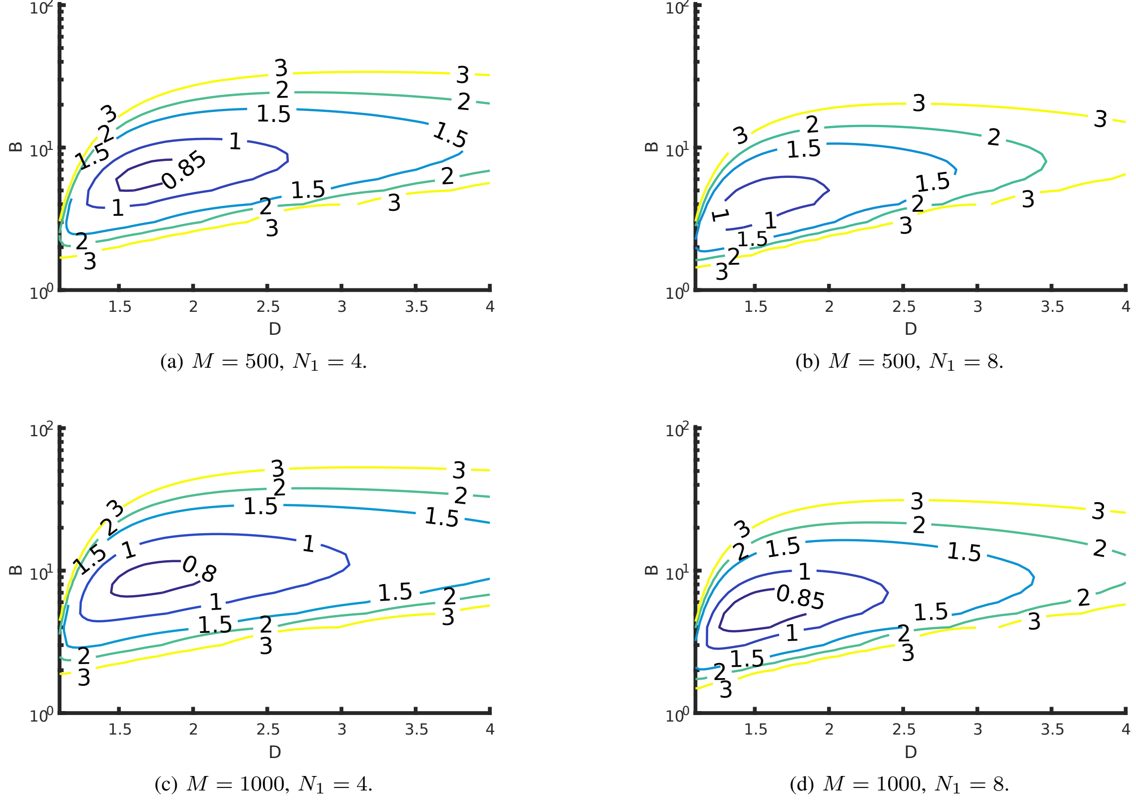
The rest of this paper focuses on the dispersion introduced by M_1 to M_4. The multiple output current mirror can be designed separately with proven techniques.

The dispersion in I_2 will be computed with the help of sensitivity coefficients, S_{VTj} and S_{β_j} defined as:

$$S_{V_{Tj}} = \frac{\partial\,(\delta I_2/I_2)}{\partial V_{Tj}},\quad S_{\beta_j} = \frac{\partial\,(\delta I_2/I_2)}{\partial\,(\delta\beta_j/\beta_j)}. \tag{11}$$

The sensitivities are determined from the transfer functions corresponding to the diagram in Fig. 2. Expressions for S_{VTj} and S_{β_j} are shown in Appendix A.

Appendix A shows that sensitivity coefficients S_{β_1} to S_{β_4} depend only on B, D, M, thus they are independent of temperature and process. On the other hand, S_{VT1} to S_{VT4}



(a) $M = 500$, $N_1 = 4$.

(b) $M = 500$, $N_1 = 8$.

(c) $M = 1000$, $N_1 = 4$.

(d) $M = 1000$, $N_1 = 8$.

Fig. 3. Dispersion multiplied by the root of total area ($\sqrt{\mathcal{G}\mathcal{A}}$) for different sets of M and N_1.

depend on process through the subthreshold slope (n), and on temperature through n and the thermal voltage ($U_T = kT/q$).

Once the sensitivity coefficients are known, the relative dispersion in I_2 can be expressed as:

$$\sigma^2_{\frac{\delta I}{I}} = \sum_{j=1}^{4}\left(\sigma^2_{V_{Tj}}.S^2_{VTj} + \frac{\sigma^2_{\beta_j}}{\beta_j^2}.S^2_{\beta j}\right) = \sum_{j=1}^{4}\frac{f^2_{Mj}}{W_u L_u}\frac{1}{N_j}\ , \tag{12}$$

where, considering (10), f_{Mj} can be written as:

$$f^2_{M_j} = \frac{A^2_{V_T}S^2_{V_{Tj}} + A^2_\beta S^2_{\beta_j}}{2} + \frac{A^2_{CWV}}{2W_u}S^2_{\beta_j},\ j = 1, 2, 3, 4\ . \tag{13}$$

We define $\mathcal{G} \equiv \sigma^2_{(\frac{\delta I}{I})}W_u L_u$ which is the squared relative dispersion multiplied by the gate area of a unit transistor ($A_u = L_u W_u$). $\mathcal{G}$ represents dispersion normalized to the unit transistor gate area. Using (12) and (9), it can be written as

$$\mathcal{G} = \frac{f^2_{M_1}}{N_1} + \frac{f^2_{M_2}}{N_1 B} + \frac{f^2_{M_3}}{M}N_1 B + \frac{f^2_{M_4}}{M}N_1 B\frac{D}{D-1}\ . \tag{14}$$

This expression does not depend on W_u or L_u. So, it is a function of the geometrical parameters N_1, B, D, M but independent of the absolute dimensions of the active transistors. This is a very strong result and the basis for the design method described in Sec. IV. It also depends through f_{M_j} on Pelgrom's mismatch coefficients for the given technology and on sensitivity coefficients. Those related to β only depend on B, D, M, while those related to V_T depend also on n and temperature. Thus we can express:

$$\mathcal{G} \equiv f(B, D, M, N_1, A_{VT}, A_\beta, A_{CWV}, n, T) \tag{15}$$

which can be split in two terms as:

$$\mathcal{G} = \mathcal{G}_\beta + \mathcal{G}_{VT}, \tag{16}$$

where the first term is:

$$\mathcal{G}_\beta = f_\beta(B, D, M, N_1, A_{VT}, A_\beta, A_{CWV}), \tag{17}$$

and, using the results in Appendix A,

$$\mathcal{G}_{VT} = \frac{f_{VT}(B, D, M, N_1, A_{VT}, A_\beta, A_{CWV})}{n^2T^2}. \tag{18}$$

Although $\mathcal{G}_{VT}$ depends on temperature, it is later shown that its effect is only marginal.

We also define the normalized area:

$$\mathcal{A} \equiv N_1 + N_2 + N_3 + N_4 \tag{19}$$

which is the total number of unit transistors in M_1 to M_4. When $\mathcal{A}$ is multiplied by Au it becomes the total gate area (A_T) for M_1 to M_4. Using (9),

$$\mathcal{A} = N_1(1 + B) + \frac{M}{BN_1}\left(1 + \frac{D-1}{D}\right)\ . \tag{20}$$

The design method to be introduced in the following section is based on the normalized functions $\mathcal{G}$ and $\mathcal{A}$.

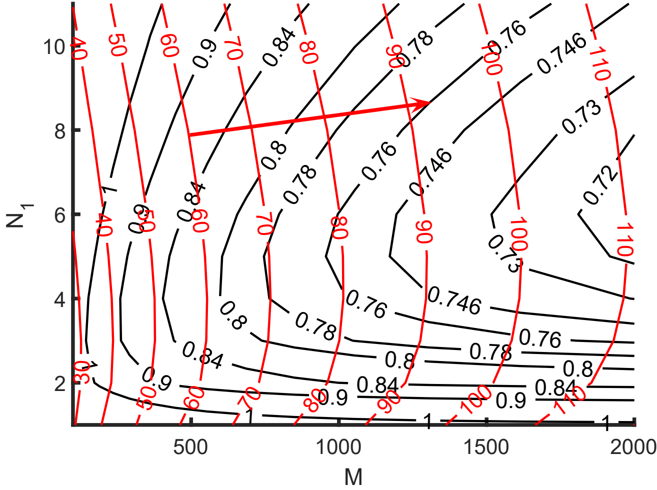


Fig. 4. Contours for $\mathcal{A}$ in red and minimal $\sqrt{\mathcal{GA}}(B,D)$ in black.

IV. Current Source Design

Combining (14) and (20), it is possible to express the square of relative dispersion times the total area as:

$$\sigma^2_{(\frac{\delta I}{I})} A_T = \mathcal{GA}(B,D,M,N_1) \tag{21}$$

which also depends on temperature and technology. $\mathcal{GA}$, still independent of W_u and L_u, indicates how efficient the spent area is in reducing dispersion. Of course, increasing the area is a brute force method to limit dispersion. The proposed method, based on optimizing $\mathcal{GA}$, intends to spend the area in a smart way by choosing the optimal distribution of area among M_1 to M_4. A lower value of $\mathcal{GA}$ corresponds to a lower dispersion for a given area.

Anyway, as will become evident, increasing the total number of unit transistors ($\mathcal{A}$) also helps to decrease dispersion but leads to a complex layout. The proposed design method attempts to minimize $\mathcal{GA}$ while keeping a reasonable number of unit transistors ($\mathcal{A}$) for a feasible layout.

The four-variable minimization problem is split in two steps for dimension reduction. For each point in the plane (M,N_1), the minimum of $\sqrt{\mathcal{GA}}(B,D)|_{M,N_1}$ is found. Fig. 3 shows $\sqrt{\mathcal{GA}}$ contours in (B,D) planes for different sets of M and N_1.

These minima define a surface in the (M,N_1) plane. Fig. 4 shows contours of minimum $\sqrt{\mathcal{GA}}(B,D)$ in the (M,N_1) plane, together with plots of the constant normalized area $\mathcal{A}$. It is clear that increasing the normalized area (layout complexity) decreases the dispersion. This combined plot helps the designer to manage the trade-off between dispersion and layout complexity.

The plots depend mainly on technology mismatch parameters and only slightly on temperature as will be shown later. The designer can start by defining all the geometry ratios without the need of choosing W_u and L_u until later on.

Up to this point in the design method, the designer chooses a design complexity, expressed as the number of unit transistors ($\mathcal{A}$) and the contours in Fig. 4 allow to define the optimal combination of those transistors (N_1, N_2, N_3, N_4) to minimize dispersion. The contours also indicate the dispersion efficiency of the spent area ($\sqrt{\mathcal{GA}}$) for the chosen complexity. Note that this result is completely independent of the unit transistor width and length and the plots depend on technology only through the mismatch parameters A_{VT} and A_β.

After choosing the layout complexity, the optimal assignment of the total number of transistors to each of them is fixed by the contours. In turn, this also fixes the inversion level of each transistor even though the width (W_u) and length (L_u) of the unit transistor are still free parameters.

In order to determine W_u and L_u, we previously calculate the needed area A_u and aspect ratio S_u. The area $A_u = W_u \times L_u$ depends on the specification for dispersion through (21) while the aspect ratio ($S_u = W_u/L_u$) determines the current through (7).

V. Model Results vs Simulation

The design method was validated through seven different designs on a 130 nm CMOS technology. The active transistors are PMOS instead of NMOS as used in [11] and shown in Fig. 1, which is of course still valid considering adequate signs for voltages and currents. Using PMOS transistors is preferred for ultra low power applications due to the lower mobility which results in a smaller current for the same unit transistor geometry. Also, in the chosen technology, the reverse current (leakage) of source / drain to substrate diodes is smaller for PMOS transistors.

All of the designs but one are based on series and parallel associations of a unit transistor with $W_u = 1\ \mu m$ and $L_u = 50\ \mu m$, chosen to produce bias currents compatible with ultra low power applications. For reference, extracted mismatch parameters for the technology are shown in Table I. For a given unit transistor, the mismatch parameters are smaller for a PMOS than those for an NMOS.

TABLE I
Extracted mismatch parameters.

Device	PMOS	PMOS	NMOS
W_u $[\mu m]$	1	40	1
L_u $[\mu m]$	50	25	50
A_{VT} $[V\mu m]$	3.8×10^{-3}	4.5×10^{-4}	5.78×10^{-3}
A_β $[\mu m]$	7.8×10^{-3}	1.28×10^{-2}	1.10×10^{-2}
A_{CWV} $[\mu m^{3/2}]$	5.89×10^{-3}	8.1×10^{-2}	1.20×10^{-1}

Fig. 5 shows designs #1 to #7 as points overlaid on the contours in Fig. 4. A preexistent, non-optimal, design (#1) was leveraged for evaluation of the dispersion model through simulations and measurements. For comparison purposes, an optimal design (#2) was obtained with the proposed method using the same D and N_1 parameters. In the latter, M is not far from that of #1 while, naturally enough, B is quite different, thus leading to a quite different output current, since the size of the unit transistor is the same in both designs. The predicted dispersion of the optimized, similar, design is 78 % of that of the initial design.

Four nearby optimal designs were also considered. Designs #3 and #4 lie on the same constant $\sqrt{\mathcal{GA}}$ curve in order to obtain a similar dispersion level with different layout complexities. Designs #5 and #6 explore dispersions levels

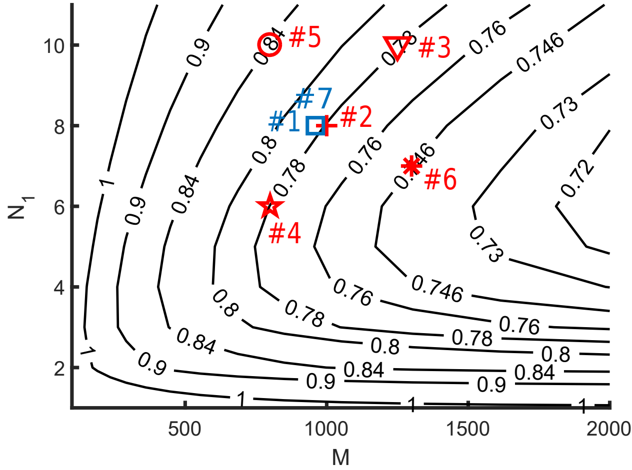


Fig. 5. Selected design points overlaid on the plot in Fig. 4.

above and below that of designs #1 to #4. Design #7 reuses the same N_1, B, D, M parameters as design #1, but in this case the unit transistor is $W_u = 40\,\mu m$, $L_u = 25\,\mu m$, such that the generated bias current is $0.98\,\mu A$. This way we will show how the same design point on the plot of Fig. 5 results in two designs generating different bias currents and displaying different dispersions obtained through adequate choice of the unit transistor. Note that, in this case, the unit transistor, and thus the total area, is increased by a factor of twenty.

The rest of this section presents simulation results for all of the designs while the next section does so with measurement results for design #1.

A. Proposed model compared to simulations

Table II presents the results obtained with Cadence Spectre DCmatch simulations at 300 K, considering only dispersion in M_1 to M_4. Note that the worst dispersion (1σ) among the optimal designs (#2 to #6) is $1.36\,\%$ (predicted), $1.54\,\%$ (simulated). The table shows better than $15\,\%$ of relative difference between the dispersion predicted by the model used throughout the design and the simulated dispersion results. This is close enough and validates the design method.

B. Test circuit

The complete schematic of current source #1 is shown in Fig. 6. The corresponding layout is displayed in Fig. 7. The core block containing the active transistors M_1 to M_4 (gate area: $A_{gate} = \mathcal{A}W_uL_u = 5200\ \mu m^2$) spends $11400\ \mu m^2$. Including the biasing current mirrors, the total area is $31550\,\mu m^2$.

A Monte Carlo simulation across 2000 cases was performed, varying parameters only for M_1 to M_4, in order to fairly compare the results to the dispersion model. Fig. 8 shows the corresponding histogram for the bias current output I_{out} at $25\ °C$. The mean is $11.8\ nA$ and the standard deviation is $191.4\ pA$, resulting in $\sigma_{\frac{\delta I}{I}MC}(\%) = 1.62\,\%$, which is very close to $1.57\,\%$, the value yielded by the model.

Table III shows a summary of predictions results across a wide range from $233\ K$ ($\approx -40\ °C$) to $398\ K$ ($\approx 125\ °C$). The variation of dispersion across temperature is quite narrow. The reason lies on that the dispersion due to β, independent of temperature (see Appendix A), dominates compared to that of V_T.

DCmatch simulations covering the variability of all the circuit components were performed at $-20\ °C$, $25\ °C$, $37\ °C$ and $100\ °C$. The results are shown in Table IV. The excess dispersion is explained by the components in the biasing mirrors.

VI. Simulation and measurement results for the test chip

This section reports measurement results for 8 samples of design #1 across the 310 K to 370 K temperature range. Each measurement is repeated 1024 times and averaged in order to minimize the effect of noise in the circuit and the measurement setup.

A. Measured bias current compared to simulations

Fig. 9 shows the averages of bias currents measured in samples A to H together with simulations for typical and worst case corners across temperature.

The variation with temperature stems from that of mobility and is intended to compensate for the mobility dependence with temperature in the biased circuits. Thanks to this temperature dependence, the biased circuits operate in a constant inversion level regardless of temperature.

Measurement results for all samples lie within the range defined by the simulations of the worst case corners. The eight points at each temperature are lumped together evidencing the achieved limited dispersion.

B. Measured bias current dispersion

Table V shows the averages of bias currents, measured at 310 K, in samples A to H.

In order to evaluate the chip to chip dispersion of the bias current, the standard deviation σ_I is usually reported, but a large amount of measurement samples is required. The available eight samples are not enough for a meaningful calculation of σ_I [23]. However, it is possible to estimate the median $\mathcal{M}$, which indicates the center value of an ordered data set.

Considering the average current values listed in Table V, the statistical method in [23] results in the median $\mathcal{M}$ lying within the range $11.13\ nA$ to $11.61\ nA$, with a $95\,\%$ probability. Also, 8 samples are enough to determine that the interval of percentiles $15.87\,\%$ to $84.13\,\%$ (akin to $\pm 1\sigma$ for a normal distribution) centered around the median is $11.13\ nA$ to $11.61\,nA$ with a $75\,\%$ probability. This interval spans $480\,pA$.

This can be compared to the $\pm 1\sigma$ dispersion of the DCmatch simulation which spans $520\,pA$ (Table IV). In conclusion, for 310 K, the dispersion obtained from measurement results and DCmatch simulations, are in reasonable agreement. The comparison between the latter and the theoretical model was addressed in Section V.

TABLE II
MODEL RESULTS VERSUS SIMULATION RESULTS FOR DISPERSION AT 300 K.

#	***Unit Trans.*** $[\mu m]$		***Geometric Parameters***			***Design Dimensions***				***Area*** $[\mu m^2]$	I $[nA]$	$\frac{\sigma(I)}{I}(\%)$		
	W_u	L_u	B	D	M	N_1	N_2	N_3	N_4	*M1 ... M4*		*Model*	*Simulation*	*Relative Difference* [%]
1	1	50	10	1.5	960	8	80	12	4	5200	11.79	1.57	1.69	7.1
2	1	50	5.25	1.50	1008	8	42	24	8	4100	2.49	1.22	1.36	10.5
3	1	50	4.8	1.44	1248	10	48	26	8	4600	2.43	1.15	1.29	11.0
4	1	50	5.83	1.53	805	6	35	23	8	3600	2.76	1.30	1.44	9.9
5	1	50	4	1.43	800	10	40	20	6	3800	2.62	1.36	1.54	11.9
6	1	50	6.14	1.58	1290	7	43	30	11	4550	4.17	1.11	1.24	10.9
7	40	25	10	1.5	960	8	80	12	4	104000	980	0.08	0.12	15

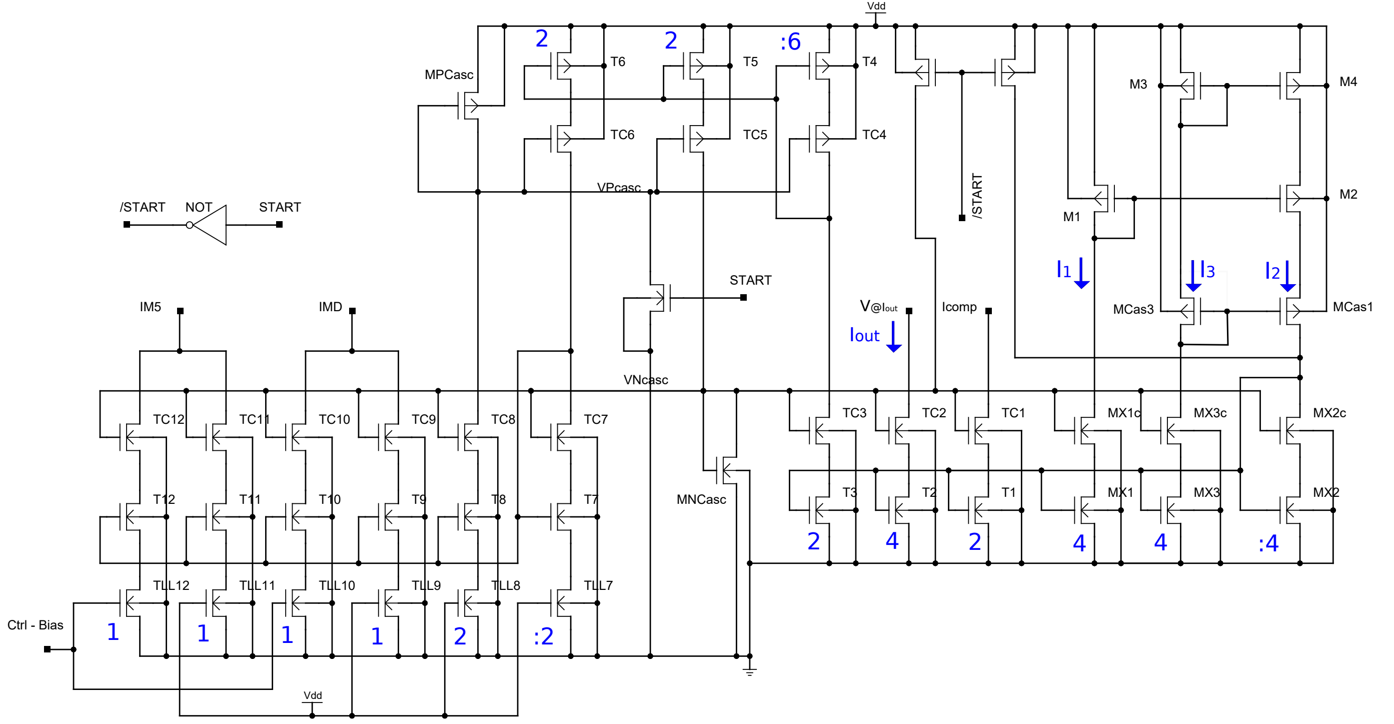


Fig. 6. Constant inversion level bias current source schematic.

TABLE III
MODEL RESULTS FOR THE VARIATION OF DISPERSION ACROSS TEMPERATURE (DESIGN #1).

$\sigma_{\frac{\delta I}{I}}(\%)@233\ K$	$\sigma_{\frac{\delta I}{I}}(\%)@300\ K$	$\sigma_{\frac{\delta I}{I}}(\%)@398\ K$
1.62	1.57	1.54

TABLE IV
DCMATCH SIMULATION RESULTS FOR THE BIAS CURRENT (DESIGN #1).

Temperature $[^\circ C]$	I_{mean} $[nA]$	σ_I $[pA]$	$\sigma_{\frac{\delta I}{I}}(\%)$
−20	10.47	237	2.26
25	11.79	255	2.17
37	12.13	260	2.14
100	14.05	285	2.03

TABLE V
BIAS CURRENT MEAN VALUES IN SAMPLES A TO H (DESIGN #1).

CHIP	$I_{avg}@310\ K\ [nA]$
A	11.15
B	11.34
C	11.53
D	11.13 (min)
E	11.42
F	11.30
G	11.61 (max)
H	11.48

C. Other simulation and measurement results

The dependence of the current on the DC voltage at the bias current output node is shown in Fig. 10. It can be seen that only 200 mV are required across the output transistors T_{C2} and T_2 (Fig. 6) to keep the current in the plateau.

Simulation results for an extended temperature range show that leakage current is no longer negligible for temperatures above 100 $^\circ C$, as shown in Fig. 11. Fig. 11 shows that the leakage in protection structure in PADs is partly responsible but most of the effect comes from leakage of S/D to substrate diodes of the circuit.

The consumption of the current source (I_{dd}) was indirectly measured as a multiple of the output current. Considering all the current mirrors involved in the circuit, $I_{dd} = 4 \times I_{out}$, so, from DCmatch simulations, the consumption of the circuit

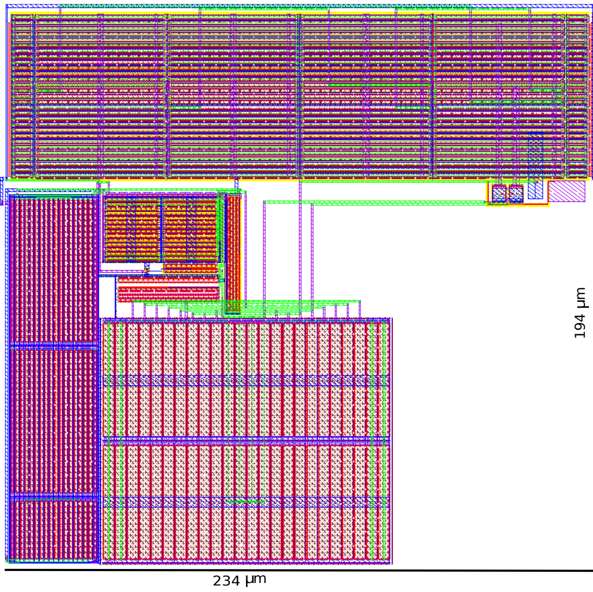


Fig. 7. Constant inversion level current source circuit layout.

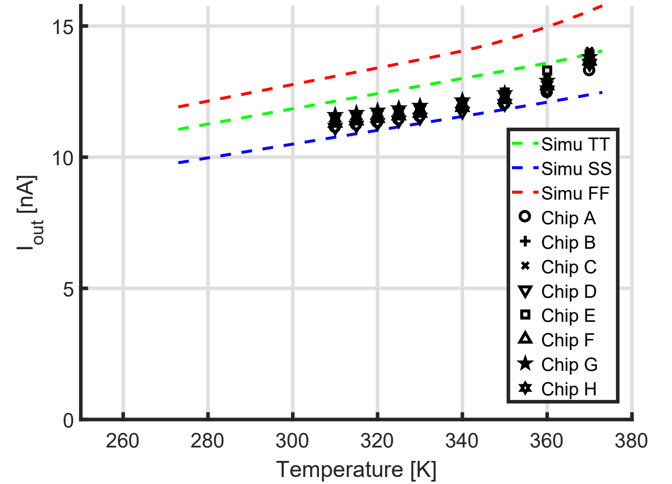


Fig. 9. Measured bias current across temperature for chips A to H compared to typical and worst case simulations (design #1).

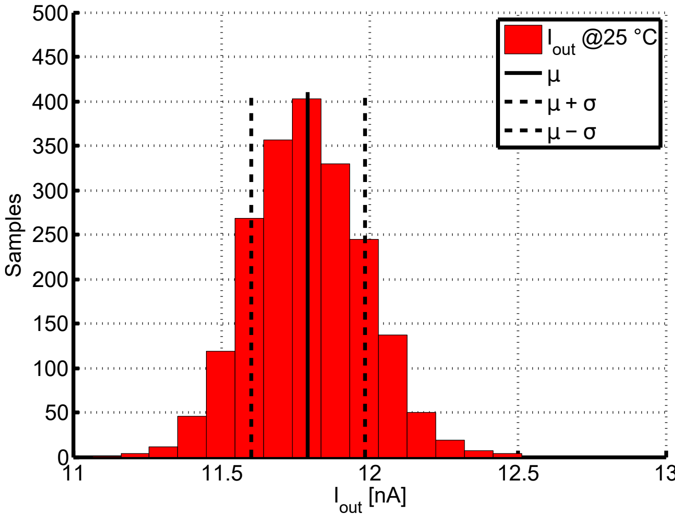


Fig. 8. Bias current dispersion at 25 $^{\circ}C$ (Monte Carlo 2000 cases, design #1). μ = 11.8 nA, σ = 191.4 pA

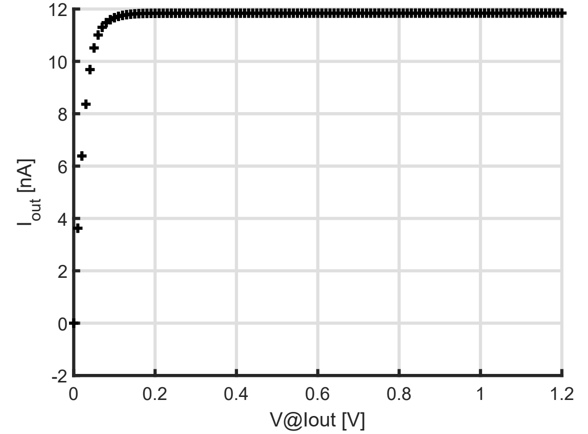


Fig. 10. Simulated bias current vs. voltage at the output node (design #1, 300 K).

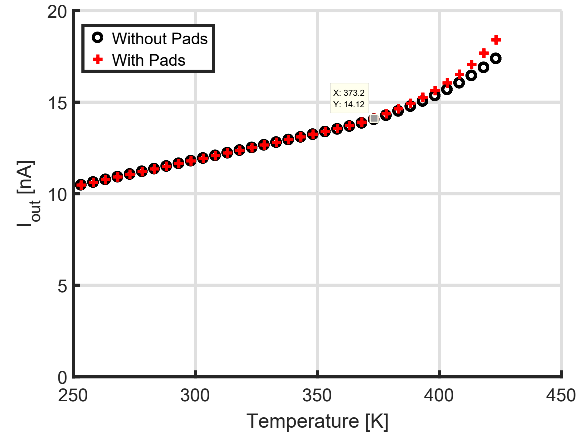


Fig. 11. Simulated leakage current effect on the bias current (design #1).

is expected to vary from 42 nA to 56 nA in the range from 253 $K(\approx -20\,^{\circ}C)$ to 373 $K(\approx 100\,^{\circ}C)$. In particular, from measurements, it is 45.5 nA in average at 310 K.

A transient simulation was performed to verify the starting method of the circuit, triggered by a pulse on the external signal *START* as shown in Fig. 12. After the pulse, the bias current decays to its steady state value.

VII. Comparison against state-of-the-art

The performance of the fabricated constant inversion level current source, in particular regarding the optimized dispersion performance, is compared against state-of-the-art in Table VI.

As explained in Section VI, the interval of percentiles 15.87 % to 84.13 % of the measured bias current spans 480 pA. For comparison purposes, this span is expressed as a

TABLE VI
COMPARISON OF REPORTED CMOS CONSTANT INVERSION LEVEL CURRENT SOURCES.

	This work	[12]	[15]	[10]	[14]
CMOS process	$0.13\,\mu m$	$1.5\,\mu m$	$90\,nm$	$2\,\mu m$	$0.18\,\mu m$
Results from:	measurements	measurements	measurements	measurements	simulations
Current average	$11.4\,nA$	$0.4\,nA$	$68\,nA$ at $1.6\,V$ $173\,nA$ at $3.6\,V$	$1\,nA$ to $100\,nA$	$50\,nA$
Dispersion	$\pm 2.11\,\%$	$\pm 10\,\%$	N/A	$\pm 30\,\%$	N/A
Number of samples	8	10	N/A	8	N/A
Temperature coefficient	$2200\,ppm/^{\circ}C$	$2500\,ppm/^{\circ}C$	$43.5\,ppm/^{\circ}C$ at $1.6\,V$ $15\,ppm/^{\circ}C$ at $3.6\,V$	N/A	$600\,ppm/^{\circ}C$
Temperature range $[^{\circ}C]$	-20 to 100	-20 to 70	-40 to 125	-60 to 80	-40 to 60
$V_{DD}\,[V]$	1.2	≥ 1.1	1.6 to 3.6	≥ 1.2	≥ 0.71
Chip area $[mm^2]$	0.032	0.046	0.03	0.06	N/A

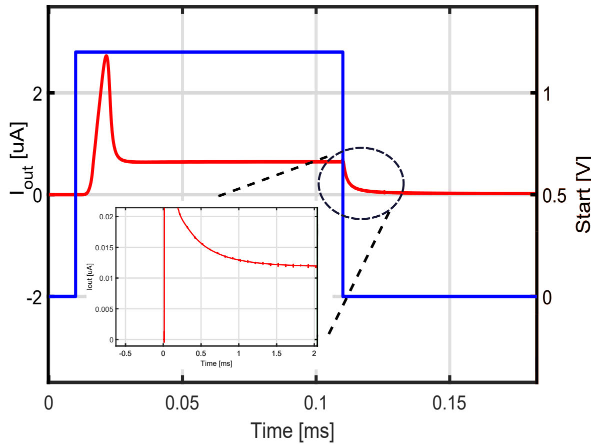


Fig. 12. Simulated current transient plot at 300 K (design #1).

percentage of the average bias current, yielding $\pm 2.11\,\%$. This result is remarkable compared to those reported [10], [12].

Since a constant inversion level bias current source is temperature dependent by definition, its temperature coefficient, that is the variation of current with temperature, is expected to be significant and depends mainly on technology.

The chip area is comparable to the other designs.

VIII. CONCLUSIONS

A constant inversion level bias current source was presented along with a thorough model of mismatch effects. The design problem was addressed and a design method was proposed that considers the trade-off between dispersion and layout complexity. The method was validated by comparing the predicted dispersion with simulation results and measurements of a test circuit fabricated on CMOS 130 nm. The results are very similar to those predicted by the model, validating the proposed design method for this kind of current source. The fabricated design outputs an average current of $11.4\,nA$ with an expected simulated dispersion of $\pm 2.17\,\%$. All measured devices were within $\pm 2,11\,\%$ of the average.

APPENDIX A
SENSITIVITY COEFFICIENTS

The sensitivity coefficients S_{β_1} to S_{β_4} and $S_{V_{T1}}$ to $S_{V_{T4}}$ are found by solving the transfer functions implied in the diagram on Fig. 2. They allow to obtain the dispersion in the current I_2 as a function of the mismatch parameters of β and V_T.

In the aforementioned diagram, g_{m1}, g_{m2} and g_{m4} are the gate transconductances of transistors M_1, M_2 and M_4, respectively, while a_2 and a_4 are auxiliary parameters that will be defined. M_X represents the transistors of the 1:1 current mirror (M_{X1} to M_{X3} in Fig. 6) with associated parameters g_{mx}, I_X, V_{TX} and β_X.

TABLE VII
SENSITIVITY COEFFICIENTS.

Transistor	Sensitivities - β	Sensitivities - V_T
M_1	$S_{\beta_1} = \frac{\alpha_1}{1-A}$	$S_{V_{T1}} = \frac{1/a_2}{1-A}\frac{g_{m2}}{I_2}$
M_2	$S_{\beta_2} = \frac{1/a_2}{1-A}$	$S_{V_{T2}} = \frac{1/a_2}{1-A}\frac{g_{m2}}{I_2}$
M_3	$S_{\beta_3} = \frac{\alpha_2}{1-A}$	$S_{V_{T3}} = \frac{g_{m4}/a_4}{1-A}\frac{1}{I_2}$
M_4	$S_{\beta_4} = \frac{1/a_4}{1-A}$	$S_{V_{T4}} = \frac{g_{m4}/a_4}{1-A}\frac{1}{I_2}$

Table VII shows all the sensitivities as a function of the expressions defined in equations (22) through (28).These depend on geometrical ratios B, D and M (Eq. 8) and on the normalized charge densities q_{S1}, q_{S2}, q_{S4}, q_{D4}. These are functions of, respectively, i_{f1}, i_{f2}, i_{f4} and i_{r4} [17], which are in turn defined by B, D and M as shown in Section II.

The parameter A is defined as:

$$A \equiv \alpha_1 + \alpha_2, \tag{22}$$

where α_1 is expressed as a function of B, q_{S2}, q_{S1} and a new parameter a_2 as:

$$\alpha_1 = \left(\frac{1}{g_{m1}}.\frac{g_{m2}}{a2}\right) = B\frac{q_{S2}}{q_{S1}}\frac{1}{2a_2}. \tag{23}$$

The parameter a_2 can be computed with good approximation as:

$$a_2 \approx 1 + \frac{n g_{m2}}{g_{md4}} = 1 + \frac{S_2}{S_4}\frac{q_{S2}}{q_{D4}}, \; \frac{S_2}{S_4} = \frac{D-1}{D}M, \tag{24}$$

thus, α_1 only depends on B, D and M. α_2 can be written as:

$$\alpha_2 = \left(\frac{1}{g_{m3}}.\frac{g_{m4}}{a_4}\right) = \frac{S_4}{S_3}\frac{1}{2a_4}\left(1-\frac{q_{D4}}{q_{S4}}\right),\ \frac{S_4}{S_3} = \frac{D}{D-1}, \tag{25}$$

which depends on a_4, approximately computed as:

$$a_4 \approx 1 + \frac{g_{md4}}{ng_{m2}} = 1 + \frac{S_4}{S_2}\frac{q_{D4}}{q_{S2}}. \tag{26}$$

So, α_2 depends only on B, D and M. Also, A depends only on those geometrical parameters, and because the sensitivities $S_{\beta 1}$ to $S_{\beta 4}$ are computed through α_1, α_2, A, a_2 and a_4, they are defined by the chosen geometry. As a consequence, these sensitivities are independent of both temperature and process.

For the sensitivities $S_{V_{T1}}$ through $S_{V_{T4}}$, as shown in Table VII, $\frac{g_{m2}}{I_2}$ and $\frac{g_{m4}}{I_2}$ are also needed. They can be computed as:

$$\frac{g_{m2}}{I_2} = \frac{1}{nU_T}\frac{2}{(q_{S2}+2)}, \tag{27}$$

and:

$$\frac{g_{m4}}{I_2} = \frac{2}{nU_T}\frac{S_4}{S_2}\frac{q_{S4}}{q_{S2}}\frac{1-\frac{q_{D4}}{q_{S4}}}{q_{S2}+2}. \tag{28}$$

Both equations (27) and (28), depend on the subthreshold slope n and on U_T. So, this set of parameters depends on temperature through n and (mainly) U_T while it depends on process through n.

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