Variability-aware Design Method for a Constant Inversion Level Bias Current Generator

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***Abstract*—A model for estimating the dispersion in the output of a MOS-only, constant inversion level, current reference is presented. Based on such model, a design method is introduced that allows to minimize dispersion for a given layout complexity. The method was applied to five different designs producing currents from 2.4 nA to 4.2 nA (@ 300 K) and simulated dispersions ranging from 1.3% to 1.5% (1 σ) while the model predicted dispersions from 1.2% to 1.4%.**

***Keywords*—Current References, MOS transistors, mismatch, ACM, temperature effects.**

I. Introduction

Current references are used in every kind of analog circuit for biasing purposes. Although constant or PTAT current references are mostly used, some circuits benefit from current references working at a constant inversion level as shown in several recent publications [1]–[8]. A MOS-only simple circuit [9]–[11] generates a constant inversion level current. Although insights on the design of these current reference circuits have been previously published [11]–[13], the dispersion of the bias current due to mismatch among the involved transistors has received so far little consideration. Moreover, in the past, the authors have come across designs with both excellent and very poor dispersion. Thus, there is a need to introduce a dispersion model in the design methodology for these circuits, which is the main purpose of this paper.

Section II reviews known results about the constant inversion level current generator. Section III introduces a mismatch based variability model for the current while Section IV presents a design method based on that model. Section V validates the design method by comparing some designs with simulation results. Finally, we draw some conclusions in section VI.

II. Circuit Analysis

This section follows [11] in describing the constant inversion level current bias generator while defining notation. The circuit analysis is based on the ACM model [14], [15] for the long channel MOSFET, accurate through all inversion levels. In ACM, the drain current of a long channel MOSFET is expressed as:

$$I_D = S\, I_{SQ}\,(i_f - i_r)\ , \tag{1}$$

where i_f and i_r are the forward and reverse inversion coefficients and $S = W/L$, W and L being respectively the effective width and length of the MOSFET. The sheet normalization current I_{SQ} is a technology parameter proportional to $\mu C'_{ox}$. The inversion coefficients are related to the normalized surface charge densities at source and drain $q_{S(D)} = -Q'_{S(D)}/nC'_{ox}U_T$, by [14]:

$$i_{f(r)} = q_{S(D)}(q_{S(D)} + 2) \Longleftrightarrow q_{S(D)} = \sqrt{1 + i_{f(r)}} - 1\ . \tag{2}$$

The circuit in Fig. 1 is a constant inversion level bias current generator. It was first proposed in [9], [10], and later extended in [12]. It was fully modelled in [11] where it is shown that it produces a particular temperature dependence on the bias current which yields a constant inversion coefficient (i_f) independent of temperature. Moreover, it depends only on ratios of the aspect ratios $S_1..S_4$ of MOSFETs $M_1..M_4$ (Fig. 1), as well as on the copy ratios of the mirrors. For simplicity and lowest consumption, these are considered to be 1:1 mirrors. It must be noted that $M_1..M_3$ are saturated, while M_4 is not. From Eq. 1, the generated bias current depends on I_{SQ}, S and i_f of any of the saturated MOSFETs, e.g: $I = I_{sq} i_{f2} S_2$. Among the many possible sets of ratios involving $S_1..S_4$, the following have been chosen for circuit analysis:

$$B = \frac{S_2}{S_1},\ M = \frac{S_2}{S_3},\ D = \frac{S_4}{S_4 - S_3}\ . \tag{3}$$

As already noted [11], choosing B, D and M determines the inversion levels of $M_1..M_4$: i_{f1}, i_{f2}, $i_{f3} = i_{f4}$, i_{r4}. Their value must be computed numerically as shown in [11]. Usually, for ultra low power applications, $S_1 > 1$, $S_2 > 1$, $S_3 < 1$ and $S_4 < 1$. Also, in order to minimize mismatch effects the transistors are designed as parallel (M_1,M_2) or series (M_3,M_4) associations of a unit MOSFET M_u with aspect ratio $S_u = W_u/L_u$. Thus, we define N_1, N_2, N_3, N_4 such that $S_1 = N_1 Su$, $S_2 = N_2 S_u$, $S_3 = S_u/N_3$, $S_4 = S_u/N_4$. Therefore, N_2, N_3, N_4 are obtained from N_1, B, D, M as:

$$N_2 = N_1 B,\ N_3 = \frac{M}{N_2},\ N_4 = N_3 \frac{D-1}{D}\ . \tag{4}$$

III. Modelling the Variability of the Bias Generator

Mismatch in both the multiple output current mirror and among the active transistors $M_1..M_4$ affect the temperature independent inversion coefficients (i_{fj}). The absolute dispersion in the threshold voltage V_T and the relative dispersion in I_{SQ}, which is that of $\mu C'_{ox}$, were modelled following [16].

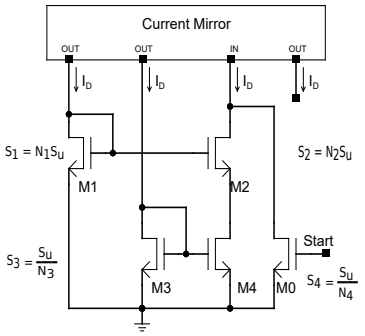


Fig. 1: MOS-only constant inversion level bias generator

We also consider the effect of channel width variation through A_{CWV} [17]. For each M_j, $j = 1, 2, 3, 4$:

$$\delta V_{Tj}^2 = \frac{A_{VT}^2}{2W_u L_u}\frac{1}{N_j}; \quad \left(\frac{\delta\beta_j}{\beta_j}\right)^2 = \frac{A_\beta^2}{2W_u L_u}\frac{1}{N_j} + \frac{A_{CWV}^2}{2W_u^2 L_u}\frac{1}{N_j}\ , \tag{5}$$

where A_{VT} $[V\mu m]$, A_β $[\mu m]$ and A_{CWV} $[\mu m^{3/2}]$ are technology parameters and the dispersions are expressed relative to a mean transistor [18].

Fig. 2 shows how each transistor contributes to the dispersion in I_2, the branch current through M_2 and M_4, by considering dispersion as a small DC signal [19]. Due to the self biased topology, the signal diagram in Fig. 2 has the shape of a closed loop.

The rest of this paper focuses on the dispersion introduced by $M_1..M_4$. The multiple output current mirror can be designed separately with proven techniques.

The dispersion in I_2 will be computed with the help of sensitivity coefficients, S_{VTj} and S_{β_j} defined as:

$$S_{V_{Tj}} = \frac{\partial\left(\delta I_2/I_2\right)}{\partial V_{Tj}}, \quad S_{\beta_j} = \frac{\partial\left(\delta I_2/I_2\right)}{\partial\left(\delta\beta_j/\beta_j\right)}. \tag{6}$$

Expressions for S_{VTj} and S_{β_j} are shown in Appendix A. The sensitivities are determined from the transfer function corresponding to the diagram in Fig. 2. They can be expressed in terms of g_m/I_D and g_{md}/I_D ratios. As these ratios are functions of i_f and i_r which are in turn determined by B, D and M [11], then the sensitivities depend only on these geometrical ratios, the subthreshold slope (n) and U_T.

Once the sensitivity coefficients are known, the relative dispersion in I_2 can be expressed as:

$$\sigma^2_{\frac{\delta I}{I}} = \sum_{j=1}^{4}\left(\delta V_{Tj}^2 . S_{VTj}^2 + \left(\frac{\delta\beta_j}{\beta_j}\right)^2 . S_{\beta j}^2\right) = \sum_{j=1}^{4}\frac{f_{Mj}^2}{W_u L_u}\frac{1}{N_j}\ , \tag{7}$$

where, considering Eq. 5, f_{Mj} can be expressed as:

$$f_{M_j}^2 = \frac{A_{V_T}^2 S_{V_{Tj}}^2 + A_\beta^2 S_{\beta_j}^2}{2} + \frac{A_{CWV}^2}{2W_u} S_{\beta_j}^2,\ j = 1, 2, 3, 4\ . \tag{8}$$

From Eq. 7, and expressing the total area of each transistor in terms of B, D, M and N_1 (introduced in Section II), we define $\mathcal{G} \equiv \sigma^2_{(\frac{\delta I}{I})} W_u L_u$. Thus,

$$\mathcal{G} = \frac{f_{M_1}^2}{N_1} + \frac{f_{M_2}^2}{N_1 B} + \frac{f_{M_3}^2}{M} N_1 B + \frac{f_{M_4}^2}{M} N_1 B \frac{D}{D-1}\ , \tag{9}$$

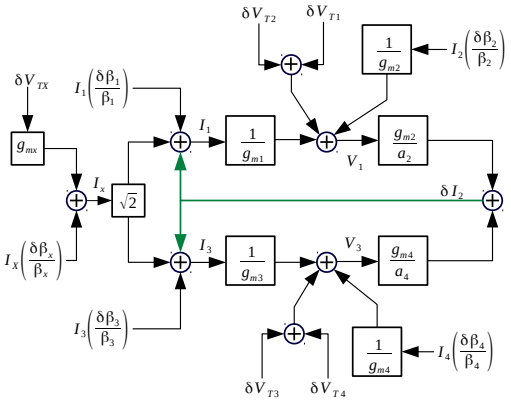


Fig. 2: Closed loop diagram for the constant inversion level bias current generator, showing dispersion in I_2 as a function of small signal and mismatch parameters.

which is the squared relative dispersion multiplied by the gate area of a unit transistor ($A_u = L_u W_u$). $\mathcal{G}$ represents dispersion normalized to the unit transistor gate area and it does not depend on W_u or L_u. This is a very strong result and the basis for the design method described in Sec. IV.

We also define the normalized area:

$$\mathcal{A} = N_1(1+B) + \frac{M}{BN_1}\left(1 + \frac{D-1}{D}\right)\ , \tag{10}$$

which is the total number of unit transistors in $M_1..M_4$. When $\mathcal{A}$ is multiplied by Au it becomes the total gate area (A_T) for $M_1..M_4$.

IV. Current Source Design

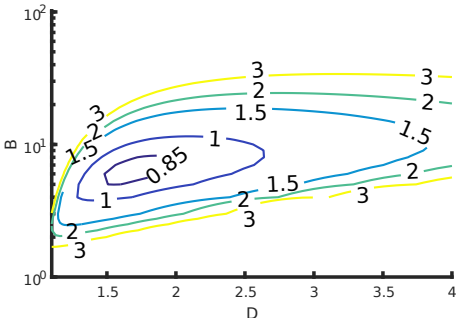
Combining Eq. 9 and Eq. 10, it is possible to express the square of relative dispersion times the total area as:

$$\sigma^2_{(\frac{\delta I}{I})} A_T = \mathcal{G}\mathcal{A}(B, D, M, N_1)\ . \tag{11}$$

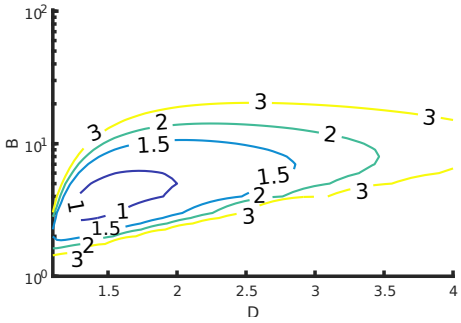
This expression is the dispersion introduced by $M_1..M_4$ normalized to the total gate area, which is still independent of W_u and L_u. A lower value of $\mathcal{GA}$ corresponds to a lower dispersion for a given area.

The proposed design method attempts to minimize $\mathcal{GA}$ while keeping a reasonable number of unit transistors ($\mathcal{A}$) for a feasible layout. The four variable minimization problem is split in two steps for dimension reduction. For each point in the plane (M, N_1), the minimum of $\sqrt{\mathcal{GA}(B,D)}|_{M,N_1}$ is found. These minima define a surface in the (M, N_1) plane. Fig. 3 shows $\sqrt{\mathcal{GA}}$ contours in (B, D) planes for different sets of M and N_1. Fig. 4 shows contours in the (M, N_1) plane together with plots of the constant normalized area $\mathcal{A}$. It is clear that increasing the normalized area (layout complexity) decreases the dispersion. This plot helps the designer to manage the trade-off between dispersion and layout complexity.

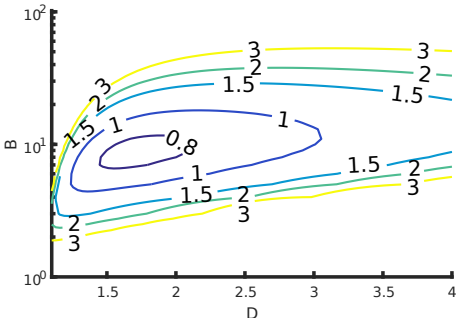
The plots depend only on technology mismatch parameters. So, the plot holds for any current source to be designed in a given technology thanks to the normalized approach, which is an outstanding result. The designer can start defining all



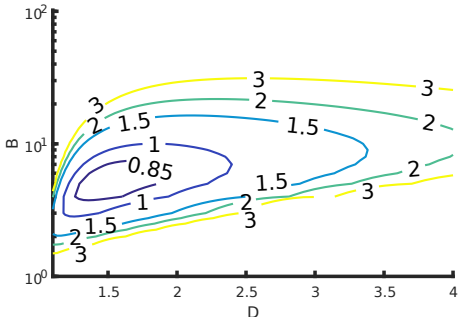
(a) $M = 500$, $N_1 = 4$.



(b) $M = 500$, $N_1 = 8$.



(c) $M = 1000$, $N_1 = 4$.



(d) $M = 1000$, $N_1 = 8$.

Fig. 3: Dispersion multiplied by the root of total area ($\sqrt{\mathcal{GA}}$) for different sets of M and N_1.

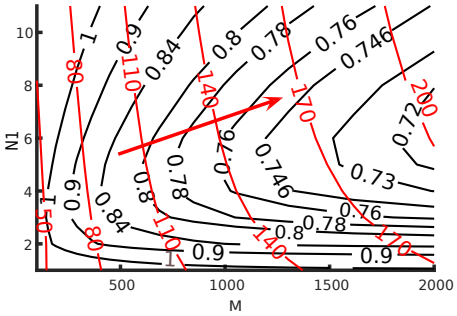


Fig. 4: Contours for $\mathcal{A}$ in red and minimal $\sqrt{\mathcal{GA}}$ in black.

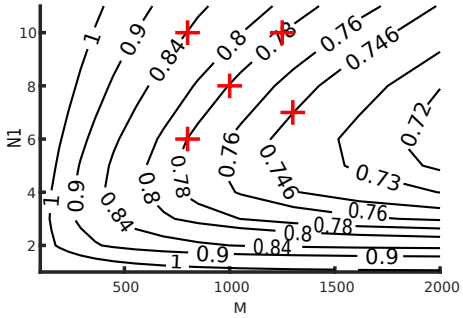


Fig. 5: Selected design points overlaid on the plot in Fig. 4.

the geometries without the need of choosing W_u and L_u until later on. The design method determines the relative size of transistors for optimum dispersion given a layout complexity. The size of the unit transistor controls the current value through $\frac{W_u}{L_u}$ and the dispersion through $W_u L_u$.

V. Model Results vs Simulation

The design method was validated through five different designs on a 130 nm CMOS technology. Fig. 5 shows them as points overlaid on the contours in Fig. 4. In order to compare them to simulation results it was necessary to select W_u and L_u, arbitrarily chosen as $W_u = 1\ \mu m$ and $L_u = 50\ \mu m$. This also determines the actual bias current. Table I presents the results which show approximately 12 % of relative difference between the model used throughout the design and the simulation results. This is close enough and validates the design method.

VI. Conclusions

A constant inversion level bias current source was presented along with a thorough model of mismatch effects. The design problem was addressed and a design method was proposed that considers the trade-off between dispersion and layout complexity. The method was validated by comparing the predicted dispersion with simulation results which were just

Design Dimensions				$I\ [nA]$	$\frac{\sigma(I)}{I}(\%)$		
N_1	N_2	N_3	N_4		*Model*	*Simulation*	*Relative Difference* [%]
10	40	20	6	2.62	1.36	1.54	11.9
7	43	30	11	4.17	1.11	1.24	10.9
8	42	24	8	2.49	1.22	1.36	10.5
10	48	26	8	2.43	1.15	1.29	11.0
6	35	23	8	2.76	1.30	1.44	9.9

TABLE I: Model results versus simulation results for dispersion.

12 % off. The obtained results define a design methodology for this kind of current source.

APPENDIX A
SENSITIVITY COEFFICIENTS

The sensitivity coefficients are found by solving the transfer functions determined by Fig. 2. The inputs are the β and V_T mismatch parameters in each transistor and the output is the dispersion in I_2.

Transistor	Sensitivities for β	Sensitivities for V_T
M_1	$S_{\beta_1} = \frac{\alpha_1}{1-A}$	$S_{V_{T1}} = \frac{1/a_2}{1-A}\frac{g_{m2}}{I_2}$
M_2	$S_{\beta_2} = \frac{1/a_2}{1-A}$	$S_{V_{T2}} = \frac{1/a_2}{1-A}\frac{g_{m2}}{I_2}$
M_3	$S_{\beta_3} = \frac{\alpha_2}{1-A}$	$S_{V_{T3}} = \frac{g_{m4}/a_4}{1-A}\frac{1}{I_2}$
M_4	$S_{\beta_4} = \frac{1/a_4}{1-A}$	$S_{V_{T4}} = \frac{g_{m4}/a_4}{1-A}\frac{1}{I_2}$

TABLE II: Sensitivity coefficients for each transistor.

Table II shows all sensitivities in terms of the expressions defined in Eq. 12 through Eq. 18. They depend on the geometrical relations B, D, M (Eq. 3) and the normalized charge densities q_{S1}, q_{S2}, q_{S4}, q_{D4}. The latter are related to the inversion coefficients through Eq. 2 which are in turn defined by B, D, M [11].

$$A = \alpha_1 + \alpha_2 \tag{12}$$

$$\alpha_1 = \left(\frac{1}{g_{m1}}.\frac{g_{m2}}{a2}\right) = B\frac{q_{S2}}{q_{S1}}\frac{1}{2a_2} \tag{13}$$

$$\alpha_2 = \left(\frac{1}{g_{m3}}.\frac{g_{m4}}{a_4}\right) = \frac{S_4}{S_3}\frac{1}{2a_4}\left(1-\frac{q_{D4}}{q_{S4}}\right),\ \frac{S_4}{S_3} = \frac{D}{D-1} \tag{14}$$

$$a_4 \approx 1 + \frac{g_{md4}}{ng_{m2}} = 1 + \frac{S_4}{S_2}\frac{q_{D4}}{q_{S2}},\ \frac{S_4}{S_2} = \frac{D}{D-1}\frac{1}{M} \tag{15}$$

$$a_2 \approx 1 + \frac{ng_{m2}}{g_{md4}} = 1 + \frac{S_2}{S_4}\frac{q_{S2}}{q_{D4}} \tag{16}$$

$$\frac{g_{m2}}{I_2} = \frac{2}{nU_T(q_{S2}+2)} \tag{17}$$

$$\frac{g_{m4}}{I_2} = \frac{S_4}{S_2}\frac{2}{nU_T}\frac{q_{S4}}{q_{S2}}\frac{1-\frac{q_{D4}}{q_{S4}}}{q_{S2}+2} \tag{18}$$

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