

SERIES-PARALLEL ASSOCIATION OF TRANSISTORS FOR THE REDUCTION OF RANDOM OFFSET IN NON-UNITY GAIN CURRENT MIRRORS.

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ABSTRACT

In this paper the series-parallel association of transistors applied to current mirrors with a non-unity copy factor is studied with regard to mismatch. This technique has been demonstrated to be a valuable tool in the design of low-offset oriented analog circuits. Some measurements are presented as well as a minimum offset design.

1. INTRODUCTION

The performance fluctuations of MOSFET's are usually modeled considering only threshold voltage V_T and current factor β fluctuations. In the simplest possible approach, V_T and β are random variables, with normal distribution, and standard deviations given by

$$\sigma_{V_T}^2 = \frac{A_{V_T}^2}{2WL}, \quad \sigma_{\beta}^2 = \frac{A_{\beta}^2}{\beta^2 2WL} \quad (1)$$

where W, L are transistor width and length respectively [1,2] and A_{V_T}, A_{β} are two technology parameters with typical values $A_{V_T}=13-35\text{mV}\cdot\mu\text{m}$ and $A_{\beta}=2-4\%\cdot\mu\text{m}$ [2]. For the sake of simplicity, only variations in V_T and β -as in (1)- will be considered in this paper. Nevertheless the analysis can be extended to other models to study the mismatch in CMOS transistors [1-4], or to obtain more accurate expressions for $\sigma_{V_T}^2, \sigma_{\beta}^2$, considering, for example, the mismatch dependence on the distance between transistors [1,2]. In analog design, it is common to express mismatch in terms of $\Delta V_T, \Delta\beta$, the difference between V_T, β , of two matched transistors. With a careful layout, the dependence of V_T and β , on the distance between transistors [1,2] is negligible and thus $\sigma_{\Delta V_T}^2 = 2\sigma_{V_T}^2, \sigma_{\Delta\beta}^2 = 2\sigma_{\beta}^2$ [2].

Offset due to transistor mismatch is a major limitation in analog circuit performance. To reduce it, the designer increases the area of the transistors, and follows some layout rules such as providing the same surroundings for the transistors. Classic current mirrors (Fig.1(a)) with a copy factor $M \gg 1$ are particularly sensitive to mismatch offset because at the output, there is a single transistor with a reduced area which generates spread variations in V_T and β . In a 2-transistor current mirror (M_A, M_B) the copy factor is calculated as the ratio between their aspect ratios:

$$\frac{(W/L)_A}{(W/L)_B} = M \quad (2)$$

Series-parallel association of transistors can aid in the obtention of different transistor geometries [5] by combining a large number of unitary transistors. In Fig.2 measured drain current vs. drain voltage curves for a single transistor, and a 10 by 10 array of the same transistor equivalent to a single one are shown. Both plots are similar, and also note in the upper plot that the drain-source transconductance g_{ds} is much smaller in the case of the composed transistor [5]. This composed transistor can substitute M_b in Fig.1(a), to implement a current mirror with the desired copy factor M (as in Fig.1(c)), but with the same number of unitary transistors at both input and output branches of the mirror. A better matching and a reduction in random offset are expected because a large number of unitary transistors have been matched. In this paper analytical expressions to estimate current offset due to random mismatch in current mirrors using series-parallel association of transistors are obtained. Measurements, examples of use and finally a minimum-offset design are presented

2. CURRENT MIRROR TOPOLOGY AND MISMATCH

In Fig.1 three different topologies for a current mirror to perform a $M:1$ current copy are shown: (a) M unitary transistors in parallel copy to a single one, (b) N -parallel transistors copy to N series-stacked transistors, (c) M unitary transistors in parallel copy to a N -series- N -parallel composed transistor. Circuits in Fig.1(b), (c) perform a $N^2:1, M:1$ copy, and present a lower current offset in comparison to Fig.1(a) because of the larger area of the equivalent transistor M'_B (M''_B). The normalized random current mismatch in the circuit of Fig.1(a) is calculated with small signal analysis, assuming that each unitary transistor M_a, M_b has the same standard deviations $\sigma_{\beta}^2 / \beta^2$ and $\sigma_{V_T}^2$:

$$\left(\frac{\sigma_{I_{out}}^2}{I_{out}^2} \right)_{(a)} = \left(1 + \frac{1}{M} \right) \left(\frac{\sigma_{\beta}^2}{\beta^2} + \frac{g_{mB}^2}{I_{out}^2} \cdot \sigma_{V_T}^2 \right) \quad (3)$$

where g_{mB} is the gate transconductance of M_b . Matching calculation considering case (b) is more complex. ΔI variations in current are produced due to variations $\Delta\beta, \Delta V_T$, in series and parallel transistors. Each contribution is calculated by small signal analysis, then the four terms are added. ΔI variations due to ΔV_{T_i} variations in the series stacked transistors of the current mirror are:

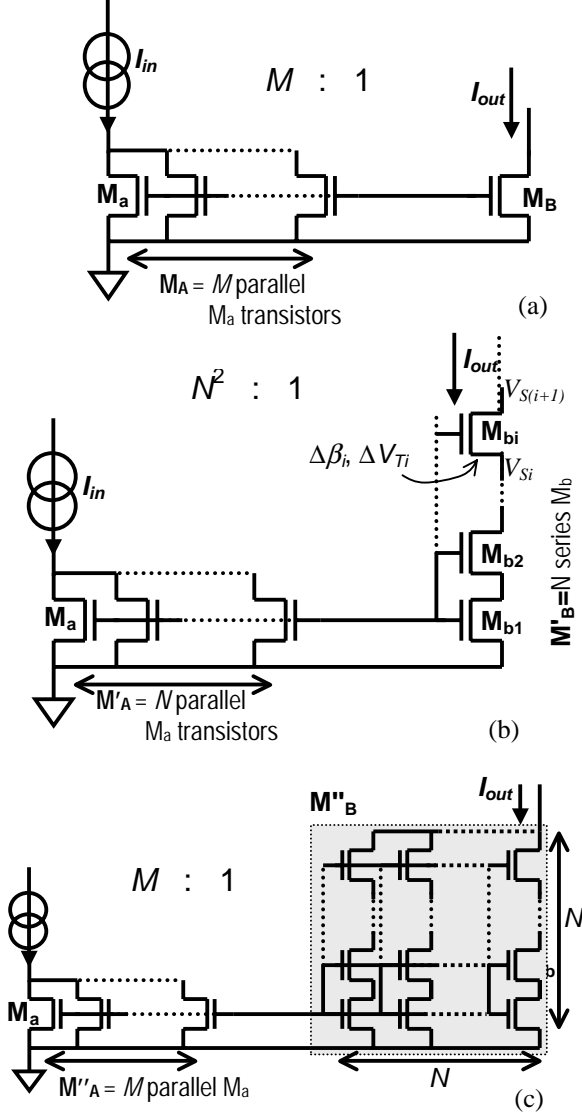


Figure 1. Three $M:1$ current copiers: (a) A M_A transistor composed by M unitary transistors M_a in parallel, copy to single transistor M_B . (b) A M'_A transistor composed by N unitary transistors M_a in parallel copy to M'_B transistor composed of N series-stacked unitary transistors M_b . (c) A M''_A transistor composed by M unitary transistors M_a in parallel, copy to M''_B transistor composed of N -series- N -parallel unitary transistors M_b . All unitary transistors $M_a \equiv M_b$ have the same $(\sigma_\beta/\beta)^2$, $(\sigma_{V_T})^2$.

$$\begin{aligned} \Delta I &= \frac{\partial I}{\partial V_T} \cdot \Delta V_T + \frac{\partial I}{\partial V_{S_i}} \cdot \Delta V_{S_i} + \frac{\partial I}{\partial V_{D_i}} \cdot \Delta V_{S(i-1)} \\ &= -g_{m_i} \Delta V_T - g_{m_{S_i}} \Delta V_{S_i} + g_{m_{D_i}} \Delta V_{S(i-1)} \end{aligned} \quad (4)$$

where g_{m_i} , $g_{m_{S_i}}$, $g_{m_{D_i}}$ are respectively the gate, source, and drain transconductances of a generic transistor M_{b_i} . Equation (4) has been derived for a generic transistor M_{b_i} ; considering that $g_{m_{D_i}} = g_{m_{S(i-1)}}$ [6, 7] and summing (4) for all the series

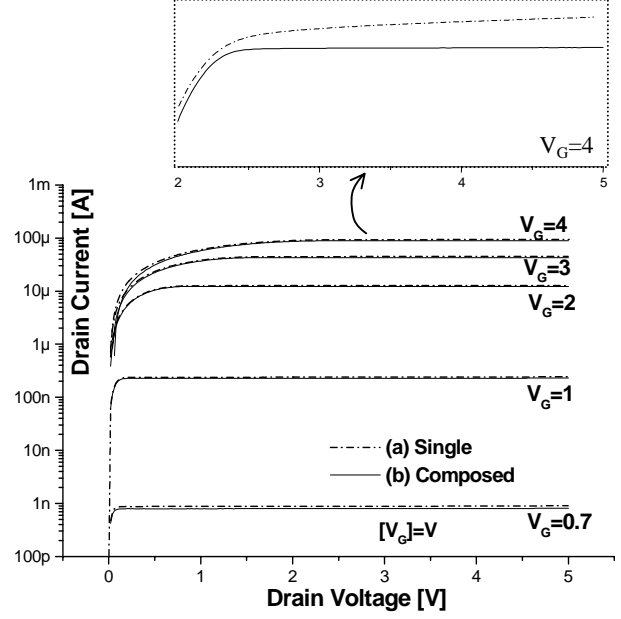


Figure 2. Measured I_D - V_D curves for different gate voltages V_G , of (a) single $W/L=4\mu\text{m}/12\mu\text{m}$ transistor. (b) 10×10 transistor array. At the top, saturation region is magnified for $V_G=4\text{V}$ to observe the change in g_{ds} from (a) to (b).

transistors:

$$N\Delta I = \sum_{i=1}^N g_{m_i} \cdot \Delta V_{T_i} \quad (5)$$

Assuming that ΔV_{T_i} are non correlated:

$$\sigma_{\Delta I}^2 = \frac{\sigma_{V_T}^2}{N^2} \cdot \sum_{i=1}^N g_{m_i}^2 \approx \frac{g_{mB'}^2}{N^2} \cdot \sigma_{V_T}^2 \quad (6)$$

$g_{mB'}$, $g_{mA'}$ are respectively, the gate transconductance of the series/parallel composed-transistor M'_B , M'_A . Note that the result of the sum in (6) is not exact, it has been approximated supposing infinite differential-length series transistors, and the integration procedure and approximations presented in [7]. An equation equivalent to (6) can be derived for $\Delta\beta_i$ variations in series transistors. Variations in β and V_T , in parallel transistors are calculated as in (3). The normalized mismatch current standard deviation is obtained:

$$\left(\frac{\sigma_{I_{out}}}{I_{out}^2} \right)_{(b)} = \frac{2}{N} \left[\frac{\sigma_\beta^2}{\beta^2} + \frac{g_{mB'}^2}{I_{out}^2} \cdot \sigma_{V_T}^2 \right] \quad (7)$$

To derive (7) it has been used that $g_{mA'}/I_{in} = g_{mB'}/I_{out}$ because both M'_A , M'_B have the same specific current [6]. The case of Fig.1(c) is quite similar to (6) but multiple series-composed transistors should be considered.

The analysis can be further extended to the general topology of Fig.3. With this configuration:

$$\frac{I_{in}}{I_{out}} = \frac{Q.R}{P.S} = M \quad (8)$$

where P , R , Q and S are the number of unitary transistors in series and parallel in each branch. The expected normalized current mismatch standard deviation for this circuit is:

$$\left(\frac{\sigma_{I_{out}}^2}{I_{out}^2} \right) = \left(\frac{1}{RS} + \frac{1}{PQ} \right) \left[\frac{\sigma_{\beta}^2}{\beta^2} + \frac{g_{mB}^2}{I_{out}^2} \cdot \sigma_{V_T}^2 \right] \quad (9)$$

$\left(\sigma_{I_{out}}^2 / I_{out}^2 \right)_{(c)}$ is calculated using (9) and $P=1$, $Q=M$, $R=S=N$. Note, from (1,3,7,9) that, for the same gate area, $\sigma_{I_{out}}^2 / I_{out}^2$ has been substantially reduced from Fig.1(a) to (b) or (c). In Fig.4 calculated and measured I_{out} , $\sigma_{I_{out}}^2 / I_{out}^2$ in terms of the input current, for a 100:1 NMOS current mirror with the topologies of Fig.1(a) ($M=100$) and (c) ($N=10$) are shown. $\sigma_{I_{out}}^2$ was calculated from 10 samples of the circuit of the same run. Unitary transistors were sized $W_u/L_u=4\mu/12\mu$, and $A_{VT}=0.03V\mu m$, $A_{\beta}=0.02\mu m$ from [2] were employed for the offset estimation using (1,3,9). The underestimation in $\left(\sigma_{I_{out}}^2 / I_{out}^2 \right)_{(a)}$ is assumed to come from the simplification in (1) of distance-related terms [1,2]. As expected, the measurements confirmed a considerable offset reduction from (c) to (a).

3. APPLICATION EXAMPLES

Current copiers with different copy factors are usual in analog integrated circuits, therefore series-parallel association of transistors is a powerful tool for the designer. For example, by combining several series-parallel unitary transistors as in Fig.5, it is possible to derive a wide range of copies of a single bias current, as usually required in analog design; very efficiently in terms of area and mismatch. The circuit in Fig.5 has been designed to derive 120nA, and 10nA currents to bias analog circuitry from a single 40nA reference. It occupies only 0.015mm² and the expected standard deviation is $\sigma_{I_{out1}}=1.4nA$, $\sigma_{I_{out2}}=0.26nA$, using $W_u/L_u=15\mu m/20\mu m$ unitary transistors.

Another interesting example is the use of series-parallel transistors for current division in standard OTAs to obtain extremely low transconductances with an extended linear range [8]. Using adequate design criteria and layout, a significant improvement in offset is obtained compared to usual current division OTAs or current cancellation techniques where offset is a serious limitation [9,10]. In Table-1 predicted and measured offset of two OTAs of 2.8nS, and 100pS are shown. The OTAs use series-parallel current division as in [8], and linearized differential input pair [11] to achieve $\pm 550mV$ (measured) linear range at the input [8]. The measured standard deviation in Table-1 was calculated using 10 circuit samples. Theoretical estimation of the offset also takes into account the offset introduced by other current mirrors, current sources, and the linearized differential pair in the circuit. But series-parallel current division still is the most significant term contributing to input offset voltage and should be reduced to improve offset.

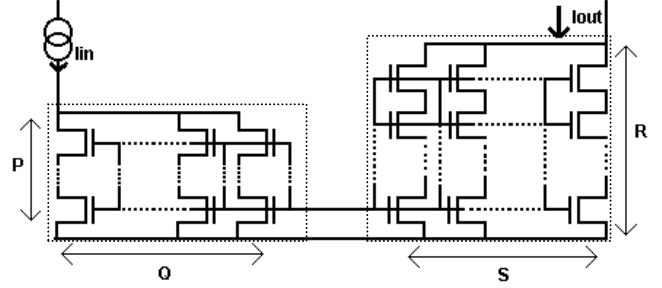


Figure 3. Schematic of a generic series-parallel current mirror with a copy factor $M=(QR)/(PS)$.

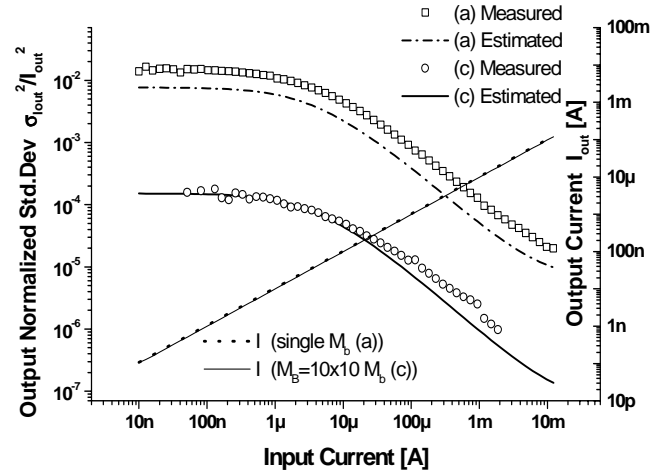


Figure 4. Calculated and measured I_{out} , $\sigma_{I_{out}}^2 / I_{out}^2$ in a 100:1 current copier as in Fig.1(a) and (c).

	$\sigma_{V_{off}} \text{ Calc.}$	$\sigma_{V_{off}} \text{ Meas.}$	$V_{off} \text{ max.}$
OTA-I	9.0mV	7.1mV	12mV
OTA-II	8.8mV	7.7mV	21mV

Table 1. Input referred offset V_{off} calculated and measured ($\sigma_{V_{off}}$ and maximum V_{off}), for (I) 100pS OTA using the current division scheme of Fig.1(b) with $N=28$, (II) 28nS OTA using the current division scheme of Fig.1(c) - $M_A = 28$ parallel, $M_B = 5 \times 5$ series-parallel.

4. DESIGN FOR MINIMUM OFFSET

Suppose a $M:1$ ($M=800$) current mirror which requires minimum offset implemented as in Fig.3. The design problem is to determine P , Q , R , S , and W_u , L_u , the width and length of the unitary transistor. Examining (9), it is assumed that $P.Q = R.S$ (equal area for M_A , M_B) for minimum mismatch offset. Another essential specification is the available area because mismatch is reduced for any topology if the gate area A_{Gate} of transistors is increased (1). Also, matched transistors, particularly with common centroid geometry, require

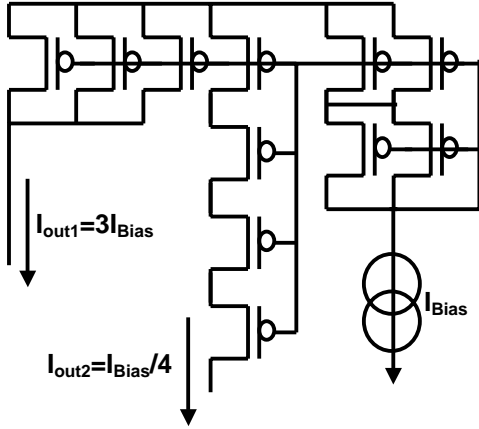


Figure 5. An efficient 4:1, 1:3 current copier.

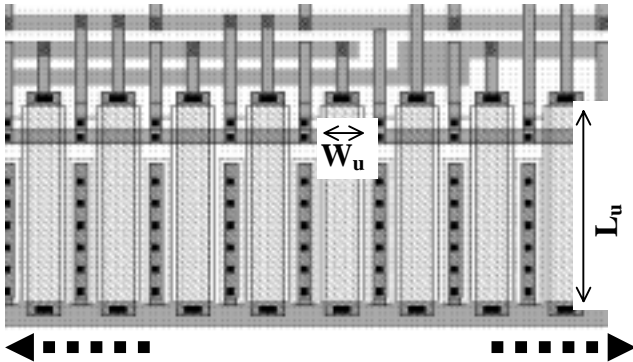


Figure 6. Layout example.

minimum distances between them and connecting wires, which increase the total circuit area A_{Total} . The ratio $\rho = A_{Gate}/A_{Total}$ has usual values from 5-20%. For the circuits presented, the layout was created by connecting row(s) of unitary transistors as in Fig.6. W_u (drawn) was chosen $4\mu\text{m}$ to reduce the effect of effective channel width reduction. A very short L_u will result in a very small ρ ratio because mainly connecting wires (see Fig.6) will compose the area. As L_u increases, ρ does so approximating a constant value. $L_u=40\mu\text{m}$ was selected examining an estimated plot $\rho(L)$ to achieve a ratio $\rho=30\%$. With the available area, and the estimated layout structure, it was possible to draw 120 unitary transistors and the solution selected was $P=1$, $Q=56$, $R=29$, $S=2$. The circuit occupies a total area of 0.05mm^2 in a $0.8\mu\text{m}$ CMOS technology, the expected current mismatch is $\sigma_{I_{out}}/I_{out} = 0.33\%$, and was designed to operate with $I_{in}=20\text{nA}$. Finally note that the composed transistor M'_B would increase the output transconductance of the current mirror due to its small g_{ds} . This can contribute also to reduce systematic offset but in the example presented, and the mirrors of Fig.1, systematic offset is mainly introduced by the drain-source transconductance of the input transistor M_A . Although it will not be discussed in this presentation,

systematic offset should be considered in a minimum offset oriented design

5. CONCLUSIONS

Series-parallel association of transistors applied to the efficient implementation of current mirrors with a wide range of copy factors has been introduced. From both measurements and theoretical estimation, the technique has been demonstrated to be valuable in terms of mismatch offset reduction. In particular, it has been shown that extremely large current multiplication (division) factors can be obtained without a significant penalty in terms of area or offset. Some examples of use, and a minimum offset-oriented design have been presented.

6. ACKNOWLEDGEMENT

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7. REFERENCES

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