ARCHITECTURE AND CELLS

FOR MICROPOWER TEMPERATURE SENSORS

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ABSTRACT

We present a temperature sensor architecture and the design of a cell for systems on a chip (SoCs) incorporating temperature sensing functions for applications in the 240 K to 400 K range. The proposed architecture emphasizes signal processing in the digital domain, thus simplifying analog circuitry and allowing very low consumption.

We perform a theoretical temperature dependence analysis of several simple circuits and apply the results to the design of a cell on a 0.8m technology that generates the basic analog signals for the aforementioned architecture. Simulations for this circuit show that it draws less than 30 nA from a supply in the 1.6V to 5.0V range while exhibiting excellent temperature characteristics.

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1. INTRODUCTION

Over the last years, evolution of electronic system design has shown a strong trend towards the use of systems-on-chip (SoCs). The availability of deep sub-micron technologies allows the integration of an increasing number of circuits in a single chip, making SoCs a reality and allowing them to integrate analog and digital processing, microelectromechanical systems (MEMS), RF circuits, sensing and many more.

The inclusion of sensing functionality in SoCs has become a must for a wide spectrum of applications, resulting in the need to master design techniques for integrated sensors.

Temperature, magnetic and optic sensors can be integrated in standard CMOS fabrication processes, guaranteeing low access cost to SOC design. Particularly, temperature is a key measurement in many SOCs, and as such, temperature sensor cells become a basic building block in state of the art Integrated Circuit (IC) design.

Temperature sensing cells are used in a wide range of applications, biomedical, cold chain monitoring and several industrial applications to name just a few. Many of these applications are intended for use in portable or even implantable systems with very long battery life.

The main goal of our research is to achieve the minimum possible consumption while low voltage is also a desirable characteristic.

Finally, the desired precision is around 0.5K, for a temperature range from 230 K to 400 K, except in the case of biomedical applications where the temperature range is much limited but the precision should be around 0.05K.

The following notation will be used throughout this paper. Variable x is defined as

$$x = \frac{T}{T_R} \qquad (1)$$

and represents the temperature relative to an arbitrary reference (often, T_R = 300 K). The subscript R will be applied to any variable taken at the reference temperature.

In section 2 we comment on the general architecture for these micropower sensors; section 3 performs a review of several options for the basic circuits. In section 4 we present a complete circuit implementing temperature dependent voltage sources and a quite stable current source while in section 5 we show the layout of the designed circuit and some very promising simulation results. Finally, we draw some conclusions and comment on future work

2. SYSTEM ARCHITECTURE

In accordance to the SoC philosophy briefly mentioned in the Introduction, we consider temperature sensors that

are integrated on the same chip to the rest of the system. Thus, it is important to take into account the whole sensing subsystem from the temperature sensitive components, through the signal conditioning, if existent, to the A/D converter. That is, in terms of architecture we will consider a complete sensing system with digital output.

The building blocks usually needed for a digital output Temperature Sensor are: a proportional to absolute temperature (PTAT) generating block, a constant reference (bandgap) block and an A/D converter. (Fig. 1)

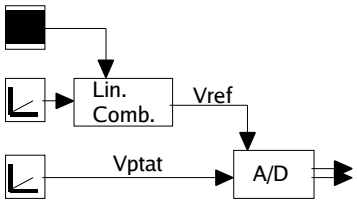


Fig. 1 Block Diagram of classic Temperature Sensor

As shown, the bandgap reference is in general obtained by summing a PTAT voltage with a voltage with negative temperature constant (NTC voltage), thus cancelling out the temperature variation to the first order. The negative temperature dependence is usually implemented with a diode-connected bipolar transistor (BJT).

Generally, a PTAT voltage will be expressed as:

$$V_{ptat} = k_p x \qquad (2)$$

and an NTC voltage can be described to the first order as:

$$V_n = V_0 + k_n x \quad , \quad k_n < 0 \qquad (3)$$

Some of the signal processing implied in Fig. 1 can be done in the digital domain [1]. We propose to represent the temperature information through a digital word (Fig. 2) which is the ratio of a PTAT voltage (Vptat) and an NTC reference (Vn). In the next Section we will comment on using MOSFETS to generate NTC voltages.

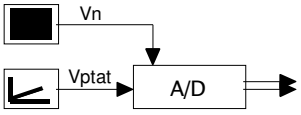


Fig. 2 Block Diagram of proposed architecture

The classical approach of Fig. 1 has two calibration parameters: V_{ref} and k_p and the main errors are caused by imperfect compensation of the NTC voltage with the PTAT signal and non-linearities in the bandgap circuit.

The proposed diagram on Fig. 2 has three calibration parameters: V_0, k_n and k_p. The main error arises from not considering higher order terms in Eq.3. In this case, the correct determination of the extra parameter k_n is equivalent to the perfect compensation inside the bandgap of the former option. So, both of them are equivalent in terms of calibration, but our proposal exhibits the flexibility of digital computation instead of performing compensation of parameters in the analog circuit. This approach takes circuit processing from the analog to the digital domain, probably with advantages in terms of consumption [2]. Curvature compensation can be performed digitally at a system level in both cases.

In practice, this conversion can be done by using an arbitrary (even not fully known) reference (Vref) for the A/D, so obtaining digital words:

$$D_n = \frac{V_n}{V_{ref}} \quad , \quad D_p = \frac{V_{ptat}}{V_{ref}} \qquad (4)$$

We can later compute:

$$\Theta = \frac{D_n}{D_p} = \frac{V_n}{V_{ptat}} \qquad (5)$$

which is independent of Vref.

This way we can simplify the A/D converter, in particular avoiding the need of preprocessing the signals which would imply added errors and consumption. We have chosen a single ramp A/D converter based on a current source and a capacitor, plus counters and a comparator. The details of the A/D converter are out of the scope of this paper, but is important to highlight the need for a high output impedance source, since it will later explain some design decisions. Although the comparator is not considered in detail, a comparison block of some kind is needed anyway to perform the A/D function.

As the system already includes an A/D converter, once the temperature is known, V_n can be used as a reference and employ the A/D to measure quantities from other parts of the SoC and as an aid to calibration by measuring an external reference.

As we will show in this paper, this architecture allows very low consumption.

3. BASIC SUBCIRCUITS

There are several options to generate V_n and V_{ptat}. In this section we will review some of them.

We will use the following notation for the thermal voltage:

$$U_T = \frac{kT}{q} = xU_{TR} \; , \; U_{TR} = \frac{kT_R}{q} \qquad (6)$$

In this section the usual models for MOS transistors are used for the different operating regions. This equations, included here for reference purposes, are expressed in terms of the pinch-off voltage V_p and the form factor S:

$$V_P = \frac{V_G - V_T}{n}\,,\; S = \frac{W_{eff}}{L_{eff}} \qquad (7)$$

For weak inversion (WI):

$$I_D = 2\,n\,S\,\mu\,C_{ox}\,U_T^2\; e^{\frac{V_P}{U_T}}\left[e^{-\frac{V_S}{U_T}} - e^{-\frac{V_D}{U_T}}\right] \qquad (8)$$

For saturated strong inversion (SI,sat):

$$I_D = \frac{1}{2}\,S\,n\,\mu\,C_{ox}\,V_P^2 \quad (\text{sat},\; V_S = 0) \qquad (9)$$

In linear strong inversion (SI,lin):

$$I_D = S\,\mu\,C_{ox}\,n V_D\left(V_P - \frac{V_D}{2}\right) \quad (\text{lin},\; V_S = 0) \qquad (10)$$

Although the classical bandgap circuits are based on bipolar transistors [3], we will concentrate on using MOS transistors operating in WI.[4,5] As in both cases the carrier transport is dominated by difussion phenomena, they obey similar exponential equations.

Fig. 3 Evolution of technology: past and forecasts

There is a potential advantage in using MOS instead of BJT. As technology advances with decreasing channel lengths, the supply voltage also goes down. This makes the fixed junction voltage of BJTs a growing fraction of the available supply. On the other hand, the threshold voltage V_T in MOS transistors will scale down as well (Fig. 3).

The following general case has immediate application in a classical PTAT circuit.

Two MOSFETS in WI

Consider two MOS transistors M1 and M2 operating in WI having their form factors and drain currents related by:

$$I_{D1} = A I_{D2} \quad , \quad S_2 = B S_1 \qquad (11)$$

With those conditions, Eq.8 implies:

$$\ln(AB) = \frac{V_{G1} - V_{G2}}{n U_T} + \ln\left(e^{-\frac{V_{S1}}{U_T}} - e^{-\frac{V_{D1}}{U_T}}\right) - \ln\left(e^{-\frac{V_{S2}}{U_T}} - e^{-\frac{V_{D2}}{U_T}}\right) \qquad (12)$$

Only some particular cases that simplify the equation are interesting:

- Common source and drain terminals for the pair:

$$V_{S1} = V_{S2}\,,\; V_{D1} = V_{D2} \Rightarrow \Delta V_G = V_{G1} - V_{G2} = n U_T \ln(AB) \qquad (13)$$

- When both transistors are saturated ($V_D >> V_S$) Eq.12 simplifies to:

$$\ln(AB) = \frac{\Delta V_G}{n U_T} - \frac{\Delta V_S}{U_T} \qquad (14)$$

which yields the following equations for common source and gate terminals:

$$\Delta V_S = 0 \;\Rightarrow\; \Delta V_G = n\,U_T \ln(AB) \qquad (15)$$

$$\Delta V_G = 0 \;\Rightarrow\; \Delta V_S = -U_T \ln(AB) \qquad (16)$$

Classical PTAT circuit

Applying the last result to the circuit of Fig. 4, we obtain that V_o is PTAT[4,5]:

$$V_o = \alpha_T U_T = x\,\alpha_T U_{TR}\;,\; \alpha_T = \ln(AB) \qquad (17)$$

A similar circuit with bipolar transistors instead of MOSFETs is widely known [3,6,7].

It must be noted that V_o does not depend on I1 and I2 and therefore it does not depend, to some extent, on the nature or value of the element Q.

Eqs. 11 and 17 show a tradeoff among sensitivity, area and consumption. We found that for minimum consumption we must choose A=1, B>1, thus $\alpha_T = \ln(B)$. Due to the logarithmic function, an increase in α_T resuls a high area penalty. Taking this fact into account

and introducing matching considerations for layout [8], a suitable choice is B=8.

Polarization of PTAT circuit.

The element Q determines the branch currents. If Q is a resistance, it must have a high value for micropower applications implying very small currents (e.g. around 10MΩ). Thus it would either spend a huge area or need a special HiRes Poly process. Besides, the temperature dependence of the resistance is in general poorly known [9].

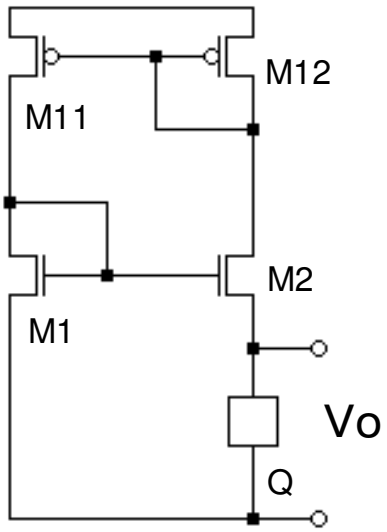


Fig. 4: Classical PTAT circuit implemented with WI MOS

So, other options must be considered for the Q element. We will concentrate on NMOS transistors in order to obtain matching with the rest of the circuit.

Throughout this paper we will assume a first order dependence of V_T with temperature:

$$V_T = V_{TR} + k_{VT}\left(x-1\right)\ ,\ k_{VT} < 0 \qquad (18)$$

Deviations from this equation will result in inaccuracies in the final results. These can be accounted for digitally at a system level.

In the first place, we consider using an NMOS in WI with Vg = Vo (Fig. 5). The branch current has the following temperature dependence:

$$I = I_R\, x^{(k_\mu + 2)}\, e^{\frac{V_{TR}+k_{VT}}{n_R U_{TR}}\frac{x-1}{x}} \qquad (19)$$

where k_μ is the exponent of the temperature variation of mobility as defined by:

$$\mu = \mu_R\, x^{k_\mu}\ ,\ k_\mu < 0 \qquad (20)$$

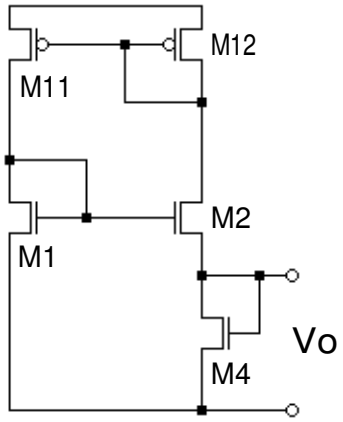


Fig. 5 PTAT biasing through a diode connected MOS in WI

The theoretical value for the mobility exponent is k_μ =-1.5 in the temperature range of interest and for usual dopant concentrations. (k_μ = -1.8 for the technology of the circuits in section 5).

Although, as stated above, k_μ+2 is usualy small, the exponential factor makes the current very dependent with temperature, for instance 10^7 times between 250K and 400K. So, this bias circuit is of limited use, perhaps for biomedical applications which operate at an almost constant body temperature.

Another possibility is shown in Fig. 6, where an NMOS in strong inversion (SI) is used as element Q, with the gate biased by another branch.

Due to the low V_{DS} (around 50 mV at 300K for α_T = L8), in paractice M4 can only be operated in a linear (nonsaturated) regime. This solution was proposed by Oguey *et al.* [9] and presents the following temperature dependence:

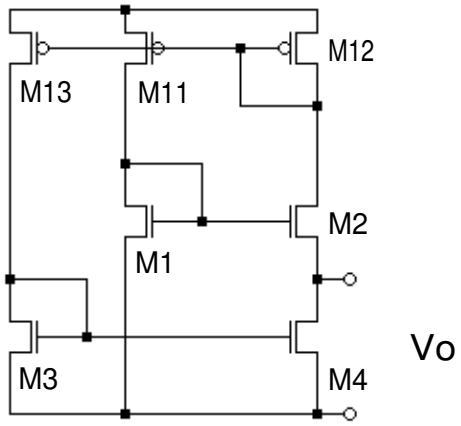


Fig. 6 PTAT biasing through a SI operating MOS

$$I_4 = I_{4R}\, y(x)\, x^{(k_\mu + 2)},\quad y(x) = \frac{n}{n_R} \qquad (21)$$

Now, k_μ is small as above and y(x) varies ± 5% in a 200K to 400K range, so I_4 has a weak dependence on temperature. So, this circuit can be used with advantage to bias not only the embedded PTAT source but other circuits as well with a quasi-constant current.

For design purposes, we need to know I_4 at a reference temperature:

$$I_{4R} = K\, I_{3R} = \frac{S_4\, G^2}{H}\, 2 n_R\, \mu_R\, C_{ox}\, \alpha_T^2\, U_{TR}^2 \qquad (22)$$

where K is the current relationship imposed by mirror M12-M13 and H and G are given by

$$H = \frac{K S_3}{S_4},\quad G = \frac{1+\sqrt{1-H}}{2} \qquad (23)$$

From the above equations, we obtain the following expression for H:

$$H = 2\left(\frac{n_R \alpha_T U_{TR}}{V_{G4R} - V_{TR}}\right) - \left(\frac{n_R \alpha_T U_{TR}}{V_{G4R} - V_{TR}}\right)^2 \qquad (24)$$

Equations 22 - 24 show that we can independently choose I_{4R} and V_{G4R}. A given size relationship H yields a unique gate voltage V_{G4R} but doesn't fix the current I_{4R} until the absolute size S_4 (or S_3 through H) is chosen.

Last, it is worth noticing that the seemingly simpler solution with $V_{G4} = V_{G1}$ is useless. For $\alpha_T \geq \ln(8)$, the existence of a solution with M4 in SI implies that S4~S2 or S4 > S2 and so, being M2 in WI, M4 will be in WI as well. If we consider M4 in WI, as M1 is in WI too, the circuit does not fix V_{G1} (=V_{G4}) and therefore the current is undetermined.

Now, we will review the temperature behaviour of some simple circuits biased with the quasi-constant current generated by the circuit shown in Fig. 6

Diode Connected MOS:

Fig. 7 Diode connected MOS

Considering as before first order variations in V_T (Eq.18), a diode connected MOS (Fig. 7) operating in WI yields a gate voltage with negative temperature dependence when biased with the quasi-constant current of Eq.20:

$$V_G = V_o + x\left[k_{VT} + y(x)\left(V_{GR} - V_{TR}\right)\right] \qquad (25)$$

where:

$$V_0 = V_{TR} - k_{VT} \quad ,\quad y(x) = \frac{n(x)}{n_R} \qquad (26)$$

and:

$$V_{GR} = V_{TR} + n_R\, U_{TR} \ln\left(\frac{I_R}{2 S n_R\, \mu_R\, C_{ox}\, U_{TR}^2}\right) \qquad (27)$$

In the previous equations, y(x) is the relative variation of the subthreshold slope n with temperature. As mentioned above, y(x) is near 1 throughout the temperature range. V_{GR} is the value of V_G at the reference temperature. The choice of V_{GR} fixes the slope of Eq. 25 while design Eq. 27 relates its value to the bias current and transistor size. This approach will be repeated for the other basic crcuits.

If we now consider the same circuit shown in Fig. 7, but biased in SI operating region, it may be shown that it also verifies Eq. 25 but with a different expression for V_{GR}:

$$V_{GR} = V_{TR} + \sqrt{\frac{2 I_R n_R}{S\, \mu_R\, C_{ox}}} \qquad (28)$$

MOS Voltage Divider:

Fig. 8 MOS voltage divider

Fig. 8 shows a MOS voltage divider formed by transistors Ma and Mb. Both transistors have the same width but different lengths. We define the following relationship between the length of transistor Mb (L_b) and the sum of both transistor's lengths ($L = L_a + L_b$):

$$L_b = \alpha L \qquad (29)$$

It can be shown that in SI the drain-source voltage in transistor Mb is:

$$V = \left(1 - \sqrt{1-\alpha}\right)\frac{V_G - V_T}{n} \qquad (30)$$

When biased with the quasi-constant current (Eq. 21), V_G is such that:

$$V = xV_R \qquad (31)$$

with:

$$V_R = \left(1 - \sqrt{1-\alpha}\right)\sqrt{\frac{2I_R}{S n_R \mu_R C_{ox}}} \qquad (32)$$

Eq. 31 also holds when the divider is operating in WI [4], but in this case:

$$V_R = U_{TR} \ln\left(\frac{1}{1-\alpha}\right) \qquad (33)$$

4. COMPLETE CIRCUIT

We combined some of the previous subcircuits in a comprehensive cell which generates all the voltages needed for the sensor temperature architecture proposed in Section 2. This cell was designed for research purposes with the main objective of checking the results presented in Section 3. For this reason the circuit has some extra outputs that would not be needed just for a temperature sensor. Fig. 9 shows a schematic diagram of the cell.

It also implements a current source to be used in a ramp generator, which was also designed but lies outside the scope of this paper.

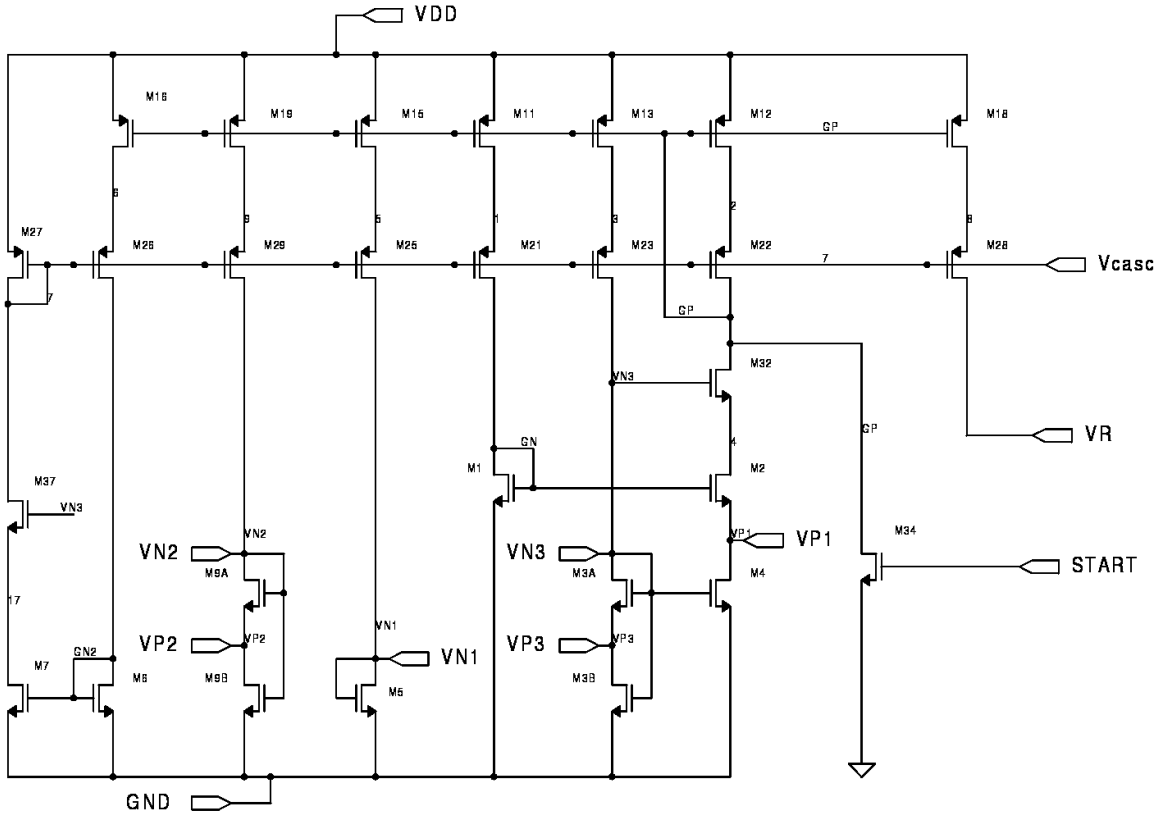
PMOS transistors M11 through M28 implement a cascoded current mirror which fixes the current an all the branches. The mirror input is branch 2 (M12 and M22). We will further comment on the mirror below.

The core of the circuit is formed by M1 to M4 as in Fig. 6. M1 and M2 operate in WI, while M3 and M4 are in SI, M4 is not saturated. The main purpose of the core is to generate the quasi-constant current (Eq. 21) which biases the whole circuit through the current mirror.

There are other outputs directly related to this kernel. Vp1 is a PTAT voltage (see also Fig. 4) which displays a small k_p ($Vp1_R$ = 46mV).

As M3 is in SI and biased by the quasi-constant current its gate voltage is that of Eqs. 25 and 28 (see also Fig. 7). Although the gate voltage of M3 is primarily intended to exhibit NTC (thus the node name Vn3), the temperature slope of Vn3 can have any sign depending on $Vn3_R$ compared to V_0 in Eq.25. For research purposes we chose $Vn3_R = V_0$, so that $Vn3 = V_0$ for any temperature (to the first order).

This way, we achieve a constant voltage reference (uncorrected for curvature effects) in a circuit with no resistances. This is not important for the sensor architecture of Section 2 but is a very useful circuit in many systems. As will be shown below, this can even be done at very low currents which extends its usefulness to micropower systems.



The main disadvantage of this circuit compared to traditional bipolar or BiCMOS bandgap generators is that V_0 is not related to fundamental constants as in the bandgap case. The value of V_0 is instead directly related to process parameters of strong variation, mainly V_T (Eq.26). This choice has the possible added advantage of making the bias point of M3 and M4 independent ot temperature which may in practice add to the stability of the circuit.

Once M3 is a MOS in SI biased with the quasi-constant current, we can split it in two serial transistors M3A and M3B implementing the divider of Fig. 8 which fulfills Eq. 31. This way we generate Vp3 which, being a PTAT voltage with adjustable k_p, can be designed with a slope greater than that of Vp1, thus obtaining higher sensitivity.

The sensor architecture is based on sequentially connecting the outputs to the same input of the A/D converter. This switching activity on Vn3 or Vp3 would disturb the core circuit and thus the current on all branches, particularly that of the ramp generator. As this is not acceptable, we replicated M3 on branch 9 (M9A, M9B, M19, M29), generating Vn2 and Vp2. We still split M3 for better matching with the replica M9.

As Vn2 was devoted to obtaining a constant voltage, we still need to generate an NTC output for our sensor architecture. For this purpose we added branch 5 (M5, M15, M15) with a diode connected MOS (M5) which generates Vn1. Having the PTAT and NTC outputs on different branches adds flexibiity in choosing the respective slopes, which is advantageous for the sensor system, resulting in added sensitivity. While M5 can be operated either in WI or SI, we chose WI for its lesser area. In our design case, the very low biasing current implies a very long transistor for SI, spending much more area than the WI counterpart.

In this circuit, any mismatch has the effect of changing one or more parameters of the output voltages (V_0,k_n,k_p). This is no worse than the parameter uncertainty due to techonology parameters spread. Both effects have to be dealt with by proper calibration performed digitally at a system level.

For this reason we do not expect Vn2 to be useful as a constant voltage reference with the shown circuit topology. Anyway, it could be easily modified by adding some kind of digital device trimming for M9 [1]. This way we could achieve a micropower constant reference voltage with no resistances. The generated reference value would nonetheless depend only on uncontrolled technology parameters.

As the ramp generator needs a current source with very high output impedance we chose to implement it with a cascode output, and for good matching among all the branches, we decided to use cascoded mirrors for the whole circuit [10]. This has the added advantage of minimizing the influence of the power supply (Vdd) on our circuit. We tried to minimize the saturation voltages on the mirror transistors in order to keep the lowest working supply voltage to a minimum. Auxiliary branches 6 and 7 generate the gate voltage of the cascode transistors. We decided to operate this branches with 1/5 the current of the others to keep the overall consumption low. The branch for the ramp generator (M18, M28) also works with a 1/5 current.

The cascodes effectively isolate the lower (NMOS) part of the circuit from variations in Vdd except for branches 2 and 7 (mirror inputs). We added NMOS cascodes (M32 and M37) to these branches in order to obtain a better stability respect to Vdd. We use the constant voltage Vn3 to bias the gates of these cascodes.

Although it should not be necessary [9], we added a start transistor (M34) intended to be digitally controlled.

5. LAYOUT AND SIMULATION RESULTS

We designed a circuit with the topology of Fig. 9 on a 0.8 micron, double poly, double metal technology. The layout of the cell is shown on and has an area of 715 x 225μm^2. This layout also includes the ramp generator and an analog multiplexer intended to output the different signals through the same buffered output pad.

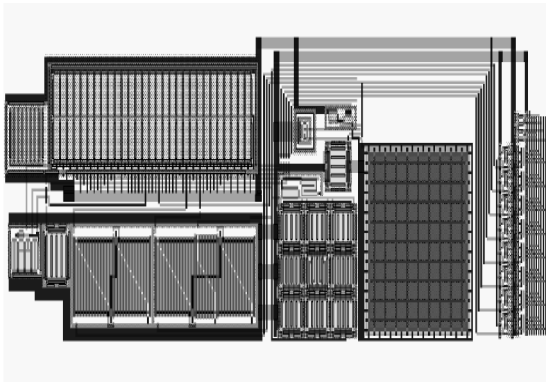


Fig. 10 Layout of the fabricated cell.

We chose a branch current of 5nA (1 nA for the reduced current branches), totalling 28 nA at T_R = 300 K.

As mentioned above, Vn2 and Vn3 were chosen to be equal to V_0 with $V_0 \approx 1.2V$ (nominal) for this technology. We selected the divider coefficient for M3 and M9 close to 1 and so that:

$$\alpha = 0.96 \quad \Rightarrow \quad \left(1 - \sqrt{1-\alpha}\right) = 0.8 \qquad (34)$$

This yields k_p=244mV for Vp2 and Vp3. From system considerations related to the sensor, k_n for Vn1 should be -658 mV which implies $Vn1_R$ = 578 mV.

Although we made the theoretical analisys of section 3 based on the classic equations valid for transistors either in deep SI or deep WI, we made all the sizing of the circuit using the ACM model [11,12] which is valid through all operating regions. We extracted the main ACM parameters by fitting to simulations performed with BSIM 3v3 and parameters provided by the foundry.

The circuit has already been fabricated but the scheduled delivery date is just past the deadline for this paper. We expect to have preliminary measurement results for the workshop.

We performed simulations of the circuit based on the BSIM 3v3 model and foundry supplied parameters in the range 230 K to 400 K (-43 C to 127 C). Fig. 11 shows the main outputs as a function of temperature for a range of supply voltages. Vn3 and Vp3 resulted respectively identical to Vn2 and Vp2 as expected. Due to the use of cascoded mirrors and cascodes M32 and M37, there is no noticeable variation of the outputs with Vdd at this scale.

The minimum operating Vdd was established at Vdd_{min} = 1.6 V for the full temperature range. At Vdd = 1.5V there was a very small difference at the lower end of the temperature range. So, Vdd_{min} can be lowered for limited

Fig. 11 Voltages VP1, VP2, VN1 and VN2 for different VDD voltages

temperature ranges. This limits results from M23 and M29 going out of saturation.

The outputs in Table 1, were obtained at T_R = 300 K, showing excellent correlation to the goals.

Output	Sim.	Specs.
$Vn1_R$ (mV)	578	578
$Vn2_R$ (mV)	1246	1236
$Vp1_R$ (mV)	46.2	53.7
$Vp2_R$ (mV)	250	244

Table 1 Specification and simulated output voltages @ T_R = 300 K

The curvature error of the outputs is shown in Fig. 12. The curves were obtained as the difference between each output and a straight line passing through the output value at T_R and having the same slope as the output at this temperature.

The worst deviation is that of Vn2 at the minimum temperature. It is equivalent to 7.1ppm/K over a 170 K range. For a smaller range from -15 C to 80 C the curvature error of Vn2 is equivalent to 4.2 ppm/K. Although these are promising numbers, it is not reasonable to compare these simulation results to published measured results.

Finally, Fig. 13 shows the total current drawn from Vdd as a function of temperature. At this zoom scale, variations with Vdd are not noticeable. The peak is just over 30 nA exhibiting a weak dependence with temperature as predicted.

Fig. 12 Curvature error in voltages VP1, VP2, VN1 and VN2

Fig. 13 Current consumption as a function of temperature

6. CONCLUSION

We have shown the development of a micropower, low voltage circuit for integrated systems (SoCs) incorporating temperature sensing functions.

The proposed architecture takes most of signal processing to the digital domain, thus simplifying the analog circuitry and allowing very small consumption.

We performed a thorough analysis of first order temperature behaviour of several simple circuits in particular when biased by a current presenting a special temperature dependence. To the best of our knowledge, this systematic analysis has never been presented in such a way and some of the results are either new or impovements over previous results.

The results of this analysis allowed us to design a circuit generating the basic signals for our architecture which draws under 30 nA from a single supply between 1.6 and 5.0V in 0.8 μ technology. It is worth noticing that matching is not an issue since its effect in the circuit will result in added deviations to those due to technology parameter spread which are unavoidable. Thus, mismatching will be compensated anyway during calibration.

Simulation results, presented in section 5, for this circuit are very promising and some immediate work is to compare this results against experimental data from the prototype upon its arrival.

Further future work includes leakage and noise analysis to determine minimum sizes and currents for such kind of circuitry. We would also like to extend the temperature analysis by using the ACM model, which could perhaps lead to removing some conditions imposed on operating regions.

The circuit must be completed with the A/D comparator and digital control. Achieving very low energy for each conversion operation is paramount to keep the micropower advantages presented above. The comparator design is particularly challenging in this respect.

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