

SpectreHDL Model of a Photodiode Cell for Electrical Simulation and its Application in a WTA Based Light Spot Center Location Circuit

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Abstract—This paper presents a photodiode cell model hierarchically implemented in SpectreHDL. A typical photodiode electrical model is used and gaussian distribution of the light spot through the pixels of the cell is implemented to estimate the amount of light power each photodiode receives. Light spot movement is also implemented in the photocell model to allow designers the validation of their signal processing circuitry.

The model introduced here shows how analog hardware description languages can be used to combine different discipline systems in one model.

I. INTRODUCTION

Low-cost CMOS technology is rapidly developing and becoming the mainstay in the IC market. The possibility of implementing photo-electronic conversion devices as photodiodes and phototransistors in CMOS takes designers to leave non-standard technologies and develop their imaging applications in CMOS where they can integrate in one chip photosensors and its signal processing circuitry.

Therefore, there is a need for compact models for this photosensors in the IC designers community. These models should be implemented in the standard CAD applications so that they can be easily used. Several SPICE models have been already presented [1], [2]. But most of them limit themselves to the electrical part of the photodiode model without having the possibility of modelling, for instance, how the light is distributed in an array of photodetectors.

Analog Hardware Description Languages such as SpectreHDL give designer the possibility of integrating different disciplines in one model. In this work, SpectreHDL is used to build a complete photodiode cell model for electrical simulations. The cell consists in an array of photodiodes which is lighted by a moving spot with gaussian power distribution. Each photodiode gets the corresponding amount of light power according to its position in the array and to the parameters defined for the cell instance. The model is used to design a spot center location application based on a winner-take-all (WTA) signal processing circuit.

Although a new electrical photodiode model is also introduced and used in our application, it is not the objective of this paper to show the actual accuracy of this model, but mainly to prove the advantages of an hierarchical modelling approach regarding its tuning and reconfiguration capabilities. The provided photodiode cell model can be configured to use any photodiode electrical model chosen by the designer and also to include other light power distribution functions which better suit the particular application. Moreover, as far as we know, it is the first SpectreHDL photodiode model which integrates electrical photodiode model and dynamics of light movement over the cell.

Section II explains the electrical model for the photodiode used. Section III explains how the model was implemented in SpectreHDL

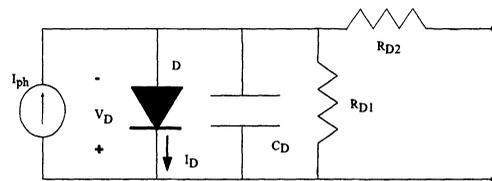


Fig. 1. Electric Model of the Photodiode

and how the photodiode cell was modelled and implemented. In Section IV the application where the cell model was used is explained including the WTA circuit introduction and in Section V the results of the mixed-signal simulation are presented. Section VI summarizes the conclusions of this work.

II. PHOTODIODE ELECTRICAL MODEL

Every diode is also a photodiode. The photoelectric effect appears in every diode which *pn* junction is lighted. The amount of generated photocurrent depends on the quantity of photons arriving to the depletion region. This is a common characteristic among the so called *photon counting devices*. [3]. The relationship between the light power absorbed and the generated photocurrent is a function of the wave length (λ) and can be seen in (1)

$$I_{PH} = \frac{q \cdot \eta \cdot P_{opt}}{h \cdot \nu} = \frac{q \cdot \eta \cdot \lambda \cdot P_{opt}}{h \cdot c} \quad (1)$$

where $\eta = \eta(\lambda)$ is the quantum efficiency, defined as the ration between the number of generated electron-hole pairs and the number of photons that hit the semiconductor surface. h es Planck constant and c is the speed of light in vacuum.

The electric model of the photodiode can be seen in Figure 1. There, I_{PH} is the photocurrent generated by the incident light, calculated with (1), and diode D characteristic is given by (2)

$$I_D = I_S \cdot e^{\frac{qV_D}{kT}} - 1 \quad (2)$$

where I_S represents the leakage currents of the reverse bias diode, that in the case of photodiodes are also called *dark currents* [4] as they are the only currents through the device in the absence of light. This leakage currents are a function of the area and perimeter of the junction, minority carrier concentrations and the minority carrier diffusion length and lifetime.

In the technology process parameters data sheet a expression for I_S is given:

$$I_S = area \cdot J_{SN} + perim \cdot J_{SSWN} \quad (3)$$

where J_{SN} y J_{SSWN} are the leakage currents density per drawn area and per drawn perimeter, respectively.

When operating in reverse bias, the photodiode presents a junction capacitance given by equation (4)

$$C_D = \frac{area.C_{JN}}{1 - \frac{V_D}{\phi}} + \frac{perim.C_{JSWN}}{1 - \frac{V_D}{\phi}} \quad (4)$$

where V_D is the diode reverse voltage, ϕ is the junction potential, C_{JN} and C_{JSWN} are the junction capacitance for $V_D = 0$ per drawn area and per drawn perimeter, respectively, and M_{JN} y M_{JSWN} are the area and sidewall junction grading coefficient, respectively.

Finally resistances R_{D1} and R_{D2} model second order effects. R_{D1} models the dependence of the photocurrents with the reverse bias voltage. R_{D2} models the potential drop in the diode connections. Typical values for these parameters are $10^8\Omega$ for R_{D1} , and a few ohms for R_{D2} .

III. MODEL IMPLEMENTATION WITH SPECTREHDL

SpectreHDL ([5]) lets designers of analog systems and integrated circuits create and use modules that encapsulate high-level behavioral descriptions of systems and components. The behavior of each module is described mathematically in terms of its terminals and external parameters applied to the module. These behavioral descriptions can be used in many disciplines (electrical, mechanical, fluid and so on).

Using this language a photodiode and a photodetector cell are modelled. For the models a hierarchical design is follow, so after the photodiode model, a pixel model is implemented and from there a 256×16 pixel photocell is modelled.

A. Photodiode Model Implementation

The SpectreHDL photodiode model is done with a behavioral description of the device. The input parameters are: area, perimeter, wave length of the incident light beam and quantum efficiency for that wave length. The model has 4 nodes, two for the optic circuit and two for the electric one. The flow into the optic input is defined as the total light power hitting the junction surface, and using (1) we can estimate the generated photocurrent. Equation (2) is then used to calculate the current through the diode and equation (4) is used to calculate the current through the depletion capacitor. Current through R_{D1} and voltage drop in R_{D2} are then calculated completing the electrical circuit.

B. Pixel Model and Implementation

Each pixel is formed by two identical photodiodes, so both generates the same amount of photocurrent. The idea is that one of the pixels connects to the rest of the pixels in its row and the other to rest in its column. Doing so, the cell will have simultaneously the currents through each row and each column of pixels. The assumption that the light power will equally distribute in each photodiode is acceptable as long as it is uniformly distributed in the pixel area. To use this the pixel area should be much smaller than the light power distribution standard deviation. To improve this desired effect, the pixel layout is designed to cancel power gradients in any of the orthogonal directions.

The SpectreHDL implementation of the pixel is done by a structural description, using two photodiode model instances and assigning each one half the total light power received by the pixel. Figure 2 shows a schematic the pixel model. Figure 3 shows a code section where this is implemented. A two optics nodes array is defined and the two photodiode instances are connected to them, so in the *analog* section the power measured through the external optic node is divided in each one of them.

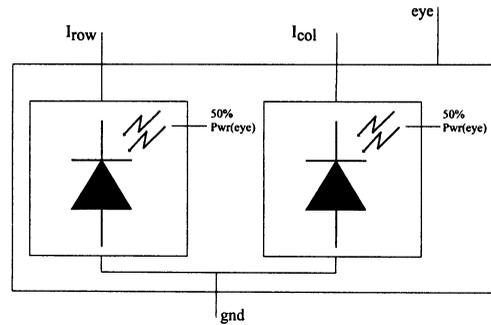


Fig. 2. Pixel model schematic.

```
node [U,Pwr] eyesPhD [2];

PhD Diodo1 (Irow,gnd,eyesPhD [0],gndopt) ();
PhD Diodo2 (Icol,gnd,eyesPhD [1],gndopt) ();

analog{
    pow=Pwr (eye,gndopt);
    Pwr (gndopt,eyesPhD [0]) <- pow/2;
    Pwr (gndopt,eyesPhD [1]) <- pow/2;
}
```

Fig. 3. Part of the SpectreHDL code describing a pixel.

C. 256×16 Pixels Photocell Model and Implementation

Incident light power in the photocell has a gaussian distribution, so in the optic circuit of the model, the light power in each pixel of the cell should be in agreement with the light spot center position and its own position in the cell. We implement this in two steps, first we implement a 16 pixels row (Figure 4), modelling the light power distribution with two parameters: the maximum light power position in the row and its standard deviation. Then a 256 rows block is implemented (Figure 5), modelling the light power distribution through them with the maximum light power position through the rows and its standard deviation. With this scheme each row is assigned a certain amount of light power depending on the y-axis maximum position and the standard deviation through rows (σ_{row}) and passing as arguments to the row cell the x-axis maximum position and the standard deviation through columns (σ_{col}).

Figure 6 shows the SpectreHDL code that implements the 16 pixel row block and how the gaussian distribution of the light power through each pixel is implemented with a function.

D. Light Spot Movement Implementation

When using this model in mixed-signal simulations, results interesting to be able to simulate that the light spot is actually moving through the cell. Therefore, spot movement is implemented by passing the spot center position argument through a function that calculates this position for each simulation time slot. To do so it

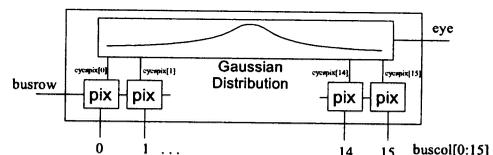


Fig. 4. 16 pixel row model schematic.

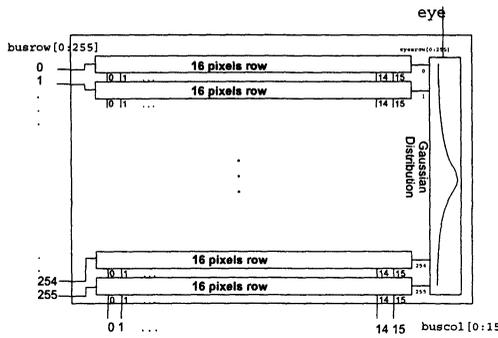


Fig. 5. 256x16 pixels cell model schematic.

```

real gauss(integer c, real mx, real sigma){
    return exp(-0.5*pow((c-mx)/sigma,2))/sqrt(2*PI)/sigma;
}

module pixelarray_1x16 (busrow,buscol,gnd,eye,gndopt)
    (sigma,vel,pos0)
node[V,I] busrow,buscol[ NUMCELL],gnd;
node[U,Pwr] eye,gndopt; parameter real sigma=1;
parameter real vel=1, pos0=3; {
    real pow;
    integer i;

    node [U,Pwr] eyespix[ NUMCELL];

    pixel p00(busrow,buscol[0],gnd,eyespix[0],gndopt)();
    pixel p01(busrow,buscol[1],gnd,eyespix[1],gndopt)();
    pixel p02(busrow,buscol[2],gnd,eyespix[2],gndopt)();
    .
    .
    pixel p15(busrow,buscol[15],gnd,eyespix[15],gndopt)();

    analog{
        pow=Pwr(eye,gndopt);
        generate(i=0:NUMCELL-1:1){
            Pwr(gndopt,eyespix[i])<-
                pow*gauss(i,posLaser(vel,pos0),sigma);
        }
    }
}

```

Fig. 6. SpectreHDL 16 pixel row code, including *gauss* function that calculates the fraction of power that corresponds to each row.

uses two parameters, *pos0* and *vel*, the initial position of the spot and the speed of it (in pix/sec) in the considered direction (rows or columns). However this implementation limits itself to only one kind of movement (constant speed) and the possibility of a one pixel step movement was added. This is done by defining a negative speed, in which case *vel* is considered the time t_0 in which the step occurs.

IV. APPLICATION: SPOT CENTER LOCATION THROUGH WTA CIRCUITS

The usual way to locate a moving spot light is to use the fact that its power distribution over the cell area is gaussian. Therefore we can assure that the row and column of pixels where the center is located will generate the greater photocurrent. Then, to locate the spot center we should measure the currents through the rows and columns of the cells and find the maximums. With this algorithm we can obtain a resolution in the spot location of one pixel.

To locate the maximum row and column with maximum current we use a *winner-take-all* circuit (WTA) presented by Lazzaro *et al.* [6].

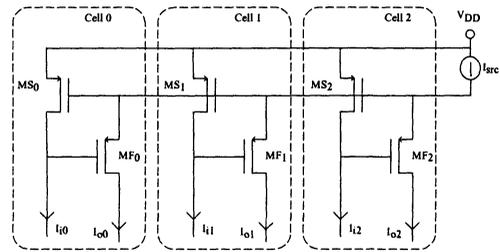


Fig. 7. A pMOS 3 cell WTA Circuit.

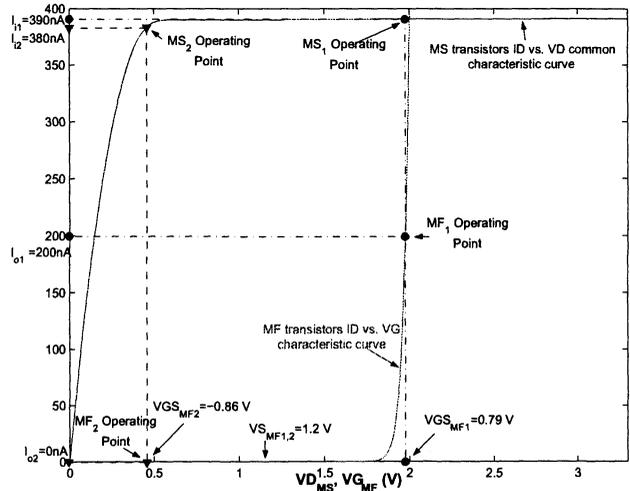


Fig. 8. Operating points of two WTA cells transistors in both their I_D vs V_D and I_D vs V_G characteristic curves.

A. Basic WTA Circuit

Figure 7 presents 3 cells of the basic WTA circuit architecture. This circuit allows to determine the higher of the three input currents ($I_{i0..2}$). Each cell is formed by two transistors MS and MF. MS sense the input current I_i and generates a V_{DS} voltage that fixes the gate voltage of MF. As every MS transistor of the architecture has the same gate voltage, all of them have the same I_D vs V_{DS} characteristic curve, and therefore the one with higher current will generate the higher drain voltage and his cell MF transistor gate voltage will also be the higher. So, most of I_{src} current will flow through the winning cell MF transistor inhibiting the current flow through the rest of the cells MF transistors. This behavior is illustrated in Figure 8 where we can appreciate how a very small difference between cell 1 and cell 2 input currents (10 nA) assures that all I_{src} current flows through MF_1 .

B. Spot Center Location Algorithm

To locate the spot center in the photodetector cell, current maximum through rows and column are searched. It can be easily shown that in a gaussian distribution, the row and column which get more light power effectively mark the spot center.

To find the maximum current in the 256 rows and the 16 columns, the architecture shown in Figure 9 is used. 256 WTA cells are used to sense and find the maximum in the rows and 16 WTA cells are used with the goal in the columns. Therefore, using an adequate circuit, we can obtain two 256 and 16 bits words from the output current levels, each one marking the maximum location with a logic '1'.

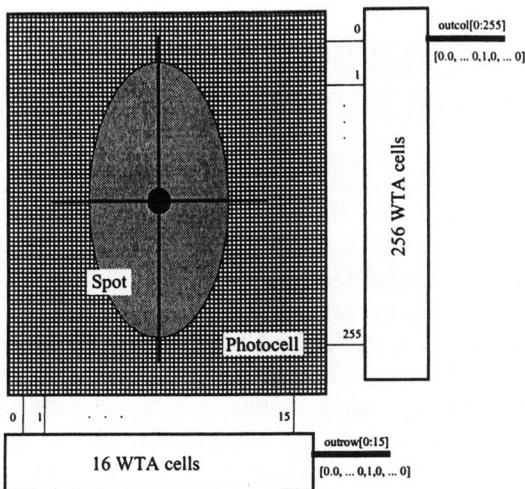


Fig. 9. Schematic view of the complete circuit used to locate the spot center.

From here on any digital circuit can easily take the information for postprocessing.

C. WTA Cell design

From figure 8 we can also get some ideas as for the sizing of transistors MS and MF. Having a large channel length L_{MS} in transistor MS will decrease the early effect in its I_{DvsV_D} curve and, thus, making all other MS transistors work in the triode region even for very small input current differences. In doing so we can obtain a bigger difference in MF transistors VG voltages and therefore assuring that all I_{src} will flow through the winner cell MF transistor. To improve this effect MF should operate in weak inversion where I_{DvsV_G} characteristic curve is exponential opposed to the quadratic one in strong inversion. Since we want to keep the parasitic capacitance at the MF gate node (MS drain node) as small as possible, for reasons that will be seen below, the channel width W_{MS} will be chosen minimum (making MS operate in near-strong inversion). The same applies for W_{MF} and L_{MF} , which will be chosen as small as possible to assure weak inversion for the given I_{src} .

V. SIMULATION RESULTS

Figure 10 shows the results of the mixed-signal simulation of the complete application when the spot center moves from one pixel to its neighbor in the next column. To simulate this case, we use the step movement implemented in our model. When the spot center moves from column 0 to column 1, the input current in WTA cell 1 increase by ΔI and input current in WTA cell 0 decrease by the same amount. This current excess in cell 1 charges the parasitic capacitance at MF gate node. This capacitor is formed by MF gate capacitor, MS source capacitor and the parasitic capacitance the column (or row) of photodiodes presents. This capacitance is usually high enough to dominate the effect in the transient response. When $V_{SD}(MS_1)$ reaches $V_{SD}(MS_0)$ I_{src} starts flowing through cell 1 and $V_{SD}(MS_0)$ starts discharging to its final value. The parasitic capacitance presented by our photocell has values of $1.2pF$ for 16pixel rows and $18pF$ for 256 pixel columns.

VI. CONCLUSIONS

The mixed-signal model of a photodetector cell for electrical simulation has been presented including the complete dynamic model

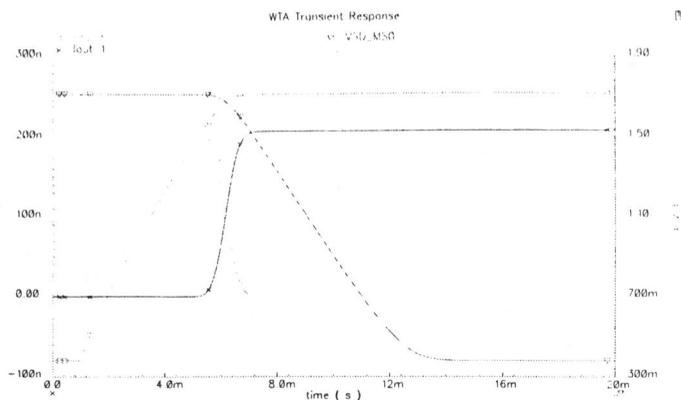


Fig. 10. Mixed-signal simulation: WTA transient response to a change in the light spot position.

for a photodiode. The novelty of the work lies on the integration of both an electrical photodiode model and the dynamics of light movement over the cell. As far as we could see in the references found, all photocells models are limited to the electrical part of the photodiode, which is clearly insufficient for simulating the dynamics of a complete cell.

The implementation of the light spot distribution and movement shows an example of how the designer can use hardware description languages (HDL) to create multidisciplinary simulation blocks to incorporate in the complete simulation of their designs.

In the electrical part of the photodiode model, the use of HDL is, of course, optional. However in this work we chose to do so to show even further the versatility of HDL. The primary objective of the work was not to validate the actual accuracy of the specific photodiode model, but to provide a flexible hierarchical photodetector cell model having advantages in its tuning and reconfiguration capabilities. The photodiode model block can be easily changed by any other model from the literature, and even the light power distribution function can be tuned or completely changed according to the experimental data.

A particular application was chosen and simulated with the implemented photodetector cell model.

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